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Product Specification

XBLW KA7500B

PWM Controllers

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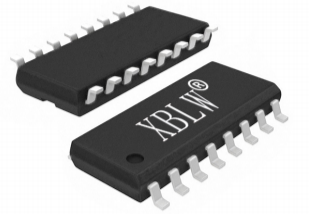
Descriptions

The KA7500B is used for the control circuit of the PWM switching regulator. The KA7500B consists of 5V reference voltage circuit, two error amplifiers, a flip flop, an output control circuit, a PWM comparator, a dead time comparator and an oscillator. This device can be operated in the switching frequency of 1kHz to 200kHz.



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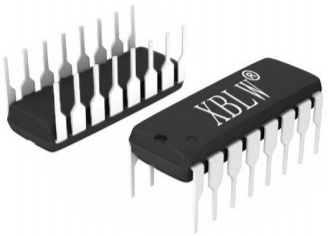

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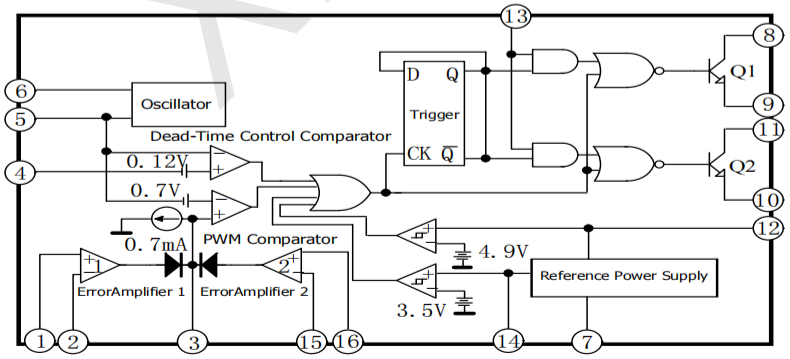
Feature

- Complete PWM Power-Control Circuitry
- On-Chip Oscillator With Master or Slave Operation
- Including Double Error Amplifier
- Internal Regulator Provides a Stable 5-V Reference Supply
- Uncommitted Outputs for 200-mA Sink or Source Current
- Variable Dead Time Provides Control Over Total Range
- Output Control Selects Single-Ended or Push-Pull Operation

Ordering Information

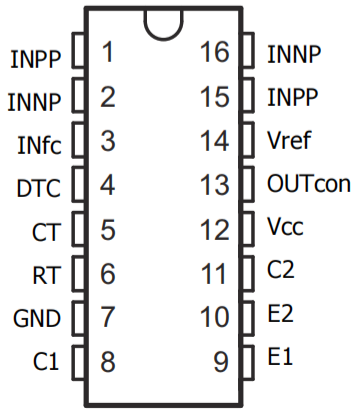
Product Model	Package Type	Marking	Packing	Packing Qty
XBLW KA7500BN	DIP-16	KA7500BN	Tube	1000pcs/Box
XBLW KA7500BDTR	SOP-16	KA7500B	Tape	2500pcs/Reel

Scematic Diagram



Pin Diagram

(TOP VIEW)



Pins Configurations

No.	Description	Symbol	No.	Description	Symbol
1	Noninverting Input 1	INPP	9	Emitter Terminal Of BJT Output 1	E1
2	Inverting Input	INNP	10	Emitter Terminal Of BJT Output 2	E2
3	Input Pin For Feedback	INfc	11	Collector Terminal Of BJT Output 2	C2
4	Dead-Time Control Comparator Input	DTC	12	Positive Supply	Vcc
5	Capacitor Terminal Used To Set Oscillator Frequency	CT	13	Output Control	OUTcon
6	Resistor Terminal Used To Set Oscillator Frequency	RT	14	5-V Reference Regulator Output	Vref
7	Ground	GND	15	Inverting Input To Error Amplifier 2	INPP
8	Collector Terminal of BJT output 1	C1	16	Noninverting Input To Error Amplifier 2	INNP

Extreme Ratings

TA=25℃,unless otherwise noted

Parameter	Symbol	Value		Unit
		Min.	Max.	
Supply Voltage	Vcc	7	40	V
Collector Output Voltage	Vc1;Vc2		40	V
Collector Output Current(Each Transistor)	Ic1;Ic2		200	mA
Amplifier Input Voltage	Vin	-0.3	Vcc-2	V
Power Dissipation(Tamb≤45℃)	PD		500	mW
Ambient Temperature	Tamb	0	70	℃
Storage Temperature Range	Tstg	-55	150	℃

Recommended Operating Conditions

Parameter	SYMBOL	Value			Unit
		Min.	Typ.	Max.	
Supply Voage	Vcc	7.0	15	40	V
Collector Output Voltage	Vc1；Vc2		30	40	V
Collector Output Current (Each Transistor)	Ic1；Ic2			200	mA
Amplifier Input Voltage	Vin	-0.3		Vcc-2.0	V
Current Into Feedback Terminal	Ifb			0.3	mA
Output Current (REF)	Iref			10	mA
Timing Resistor	RT	1.8	30	500	kΩ
Timing Capacitor	CT	0.00047	0.001	10	μF
Oscillator Frequency	fosc	1.0	40	200	kHz

Electrical Characteristics

CHARACTERISTICS	TEST CONDITIONS	SYMBOL	Value			Unit
			Min.	Typ.	Max.	
Reference Section						
Output voltage (REF)	Io=1.0mA	Vref	4.75	5.0	5.25	V
Output voltage change with temperature	ΔTamb=MIN to MAX	ΔVref/ΔT		1.3	2.6	%
Linearity of voltage regulation	Vcc=7.0V~40V	Reg line		2.0	25	mV
load regulation	Io=1.0mA~10mA	Reg load		2.0	15	mV
Short-circuit output current	Vref=0V，Tamb=25℃	Isc		32		mA
Output section						
Collector leakage current	Vcc=40V；Vce=40V	Ic(off)		2.0	100	μA
Emitter leakage current	Vcc=40V；Vc=40V；Ve=0V	Ie(off)			-100	μA
Collector-Emitter Saturation Voltage Fall	Common-emitter：Ve=0V；Ic=200mA	Vc(sat)		1.1	1.3	V
	Emitter-follower：Vc=15V；Ie=-200mA	Ve(sat)		1.5	2.5	V
Output control current	Voc=Vref	IOCH		0.2	3.5	mA
Rise time	Common-emitter configuration see Figure 3	Tr		100	200	ns
	Emitter-follower configuration, See Figure 4			100	200	ns
Fall time	Common-emitter configuration see Figure 3	Tf		25	100	ns
	Emitter-follower configuration, See Figure 4			40	100	ns
Error-Amplifier Section						
Input offset voltage	Vo (pin3)=2.5V	Vio		2.0	10	mV
Input offset current	Vo (pin3)=2.5V	Iio		5.0	250	nA
Input bias current	Vo (pin3)=2.5V	IIB		0.1	1.0	μA
Common-mode input voltage range	Vcc=7.0V~40V	VICR	-0.3		Vcc-2.0	V
Open-loop voltage amplification	Vo=0.5V~3.5V；RL=2.0kΩ; ΔVo=3.0V	GVOL	70	95		dB
Unity-gain bandwidth	Vo=0.5V~3.5V；RL=2.0kΩ	fc		800		kHz
Common-mode rejection ratio	Vcc=40V	CMR R	65	90		dB
Output sink current	Vo (pin3)=0.7V	Io-	0.3	0.7		mA
Output source current	Vo (pin3)=3.5V	Io+	-2.0	-4.0		mA
PWM Comparator Section (See Figure 2)						
Input threshold voltage	Zero Duty Cycle	VTH		4	4.5	V
Input sink current	V (pin3)=0.7V	II-	0.3	0.7		mA
Input sink current (See Figure 2)						

Input bias current	Vin=0V~5.25V	IIB(DT)		-2.0	-10	μA
Maximum duty cycle, each output	Vin=0V； RT=12kΩ;CT=0.1μF	DCmax		45		%
Input threshold voltage (pin4)	Zero Duty Cycle	V_{TH}		3	3.3	V
	Maximum Duty Cycle		0			
Oscillator Section						
Frequency	RT=12kΩ;CT=0.01μF	fosc		10		kHz
Standard deviation of frequency	RT=30kΩ;CT=0.001μF	Δfosc		3.0		%
Frequency change with voltage	Vcc=7.0V~40V	Δfosc/ΔV		0.1		%
Frequency change with temperature	RT=12kΩ;CT=0.01μF；Tamb=Tlow~Thigh	Δfosc/ΔT			12	%
Start time Control						
Low current input	V (pin3)=0.4V	I_{STL}		-25	-200	μA
High current input	V (pin13)=2.4V	I_{STH}		25	200	μA
	V (pin13)=Vref			75		
Total Device						
Standby supply current (Pin6 is Vref,All other inputs and outputs open)	Vcc=15V	Icc		6	10	mA
	Vcc=40V			9	15	
Average supply current (see Figure 2)	Vcc=15V；RT=12kΩ;CT=0.01μF； V (pin14)=2.0V			7.5		mA

Test Diagrams

Figure 1 Error Amplifier Characteristics Test Circuit

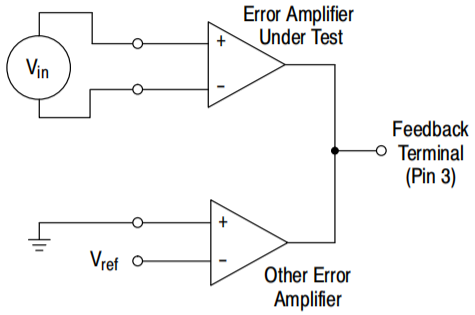


Figure 2 Deadtime and Feedback Control

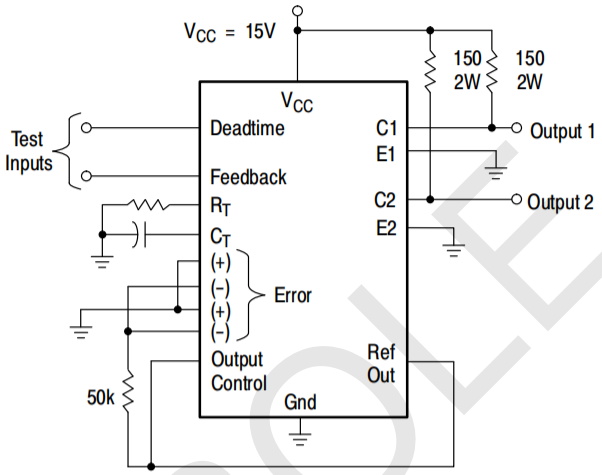


Figure 3 Common-Emitter Test Circuit

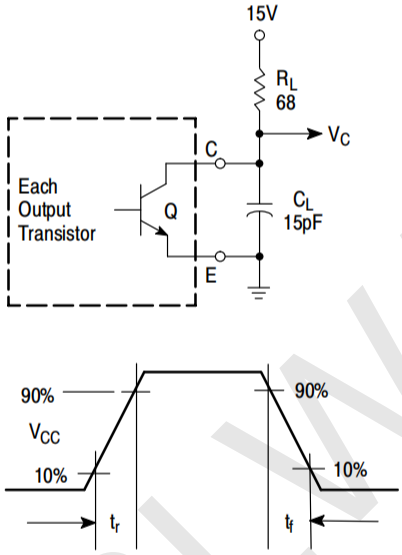


Figure 4 Emitter-Follower Test Circuit

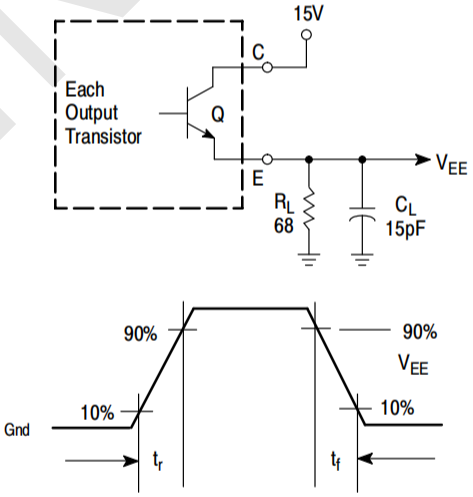
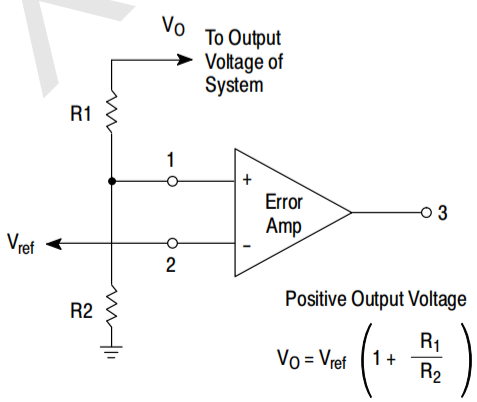


Figure 5 Error Amplifier Sensing Technology



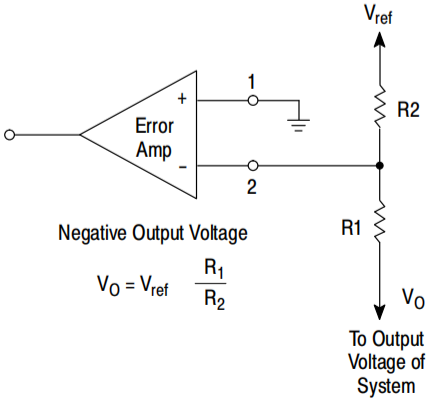
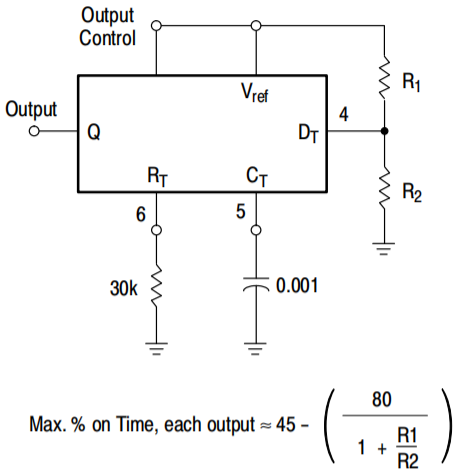


Figure 6. Deadtime Control Circuit



$$\text{Max. \% on Time, each output} \approx 45 - \left(\frac{80}{1 + \frac{R1}{R2}} \right)$$

Figure 7. Soft−Start Circuit

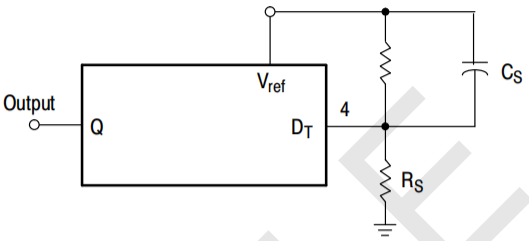


Figure 8. Output Connections for Single−Ended and Push−Pull Configurations

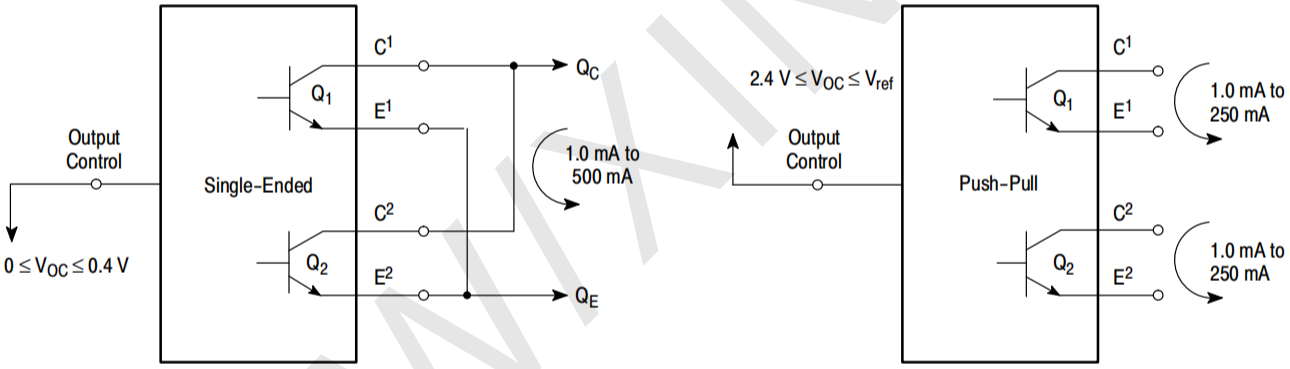


Figure 9. Slaving Two or More Control Circuits

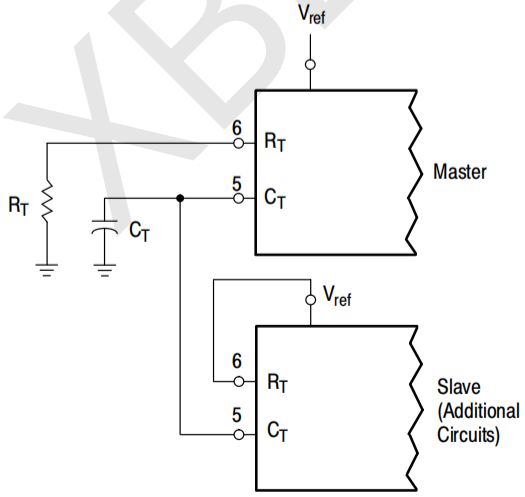
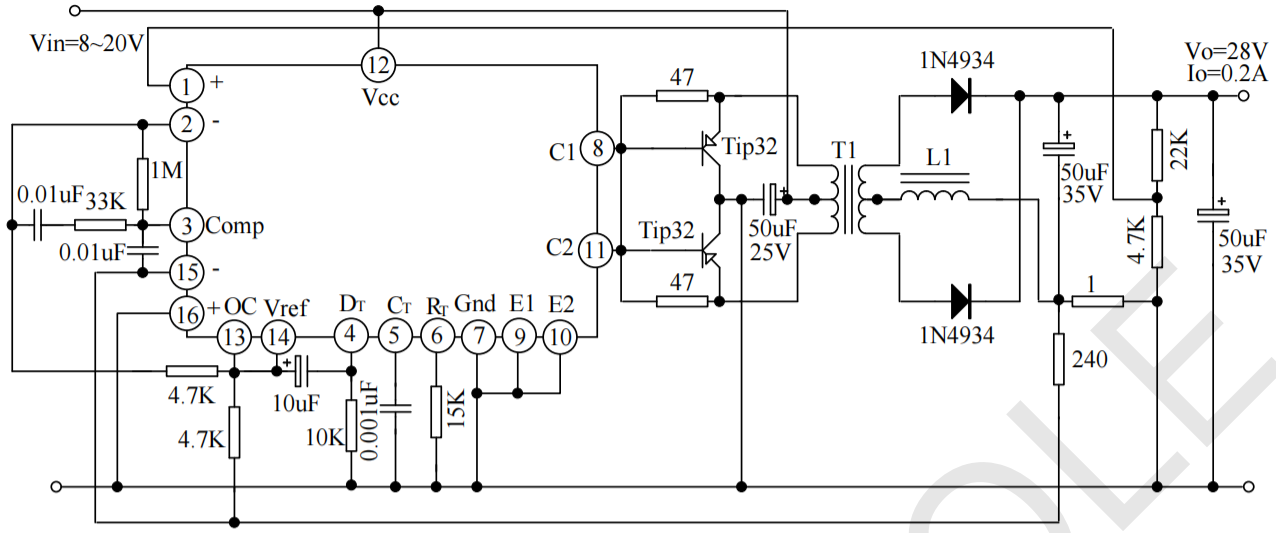
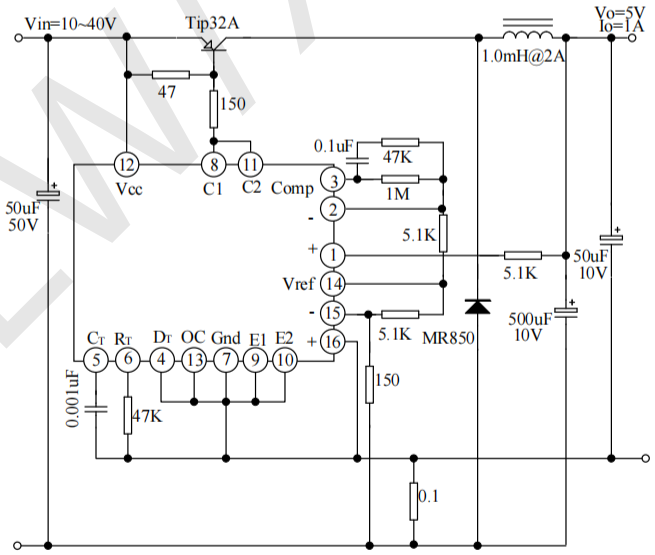


Figure 10. Pulse Width Modulated Push –Pull Converter



Test Item	Test Conditions	Result
Power Voltage	Vin=10V~40V	14mV0.28%
Load Regulation	Vin=28V；Io=1.0mA~1.0A	3.0mV0.06%
Output Voltage Ripple	Vin=28V；Io=1.0A	65mVppP.A.R.D
Short-Circuit Current	Vin=28V；RL=0.1Ω	1.6A
Efficiency	Vin=28V；Io=1.0A	71%

Figure 11. Pulse Width Modulated Step-Down Converter

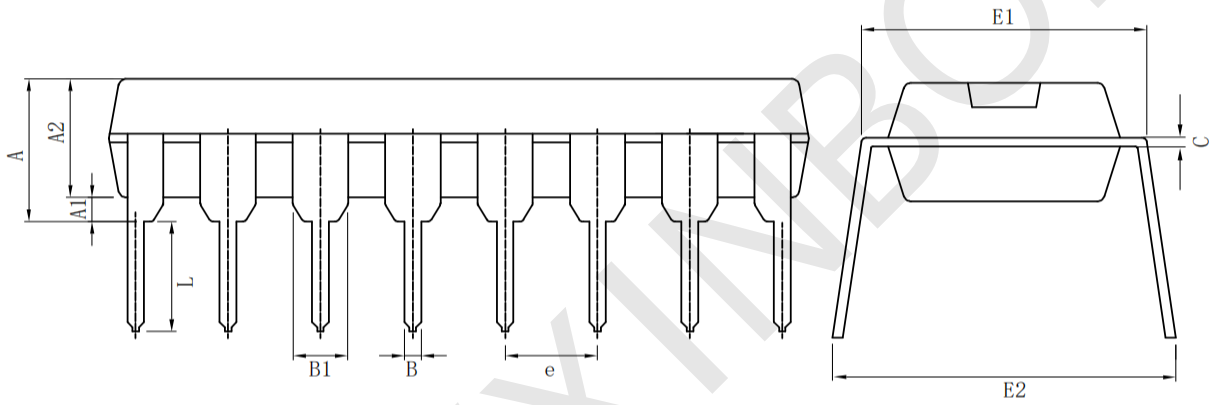


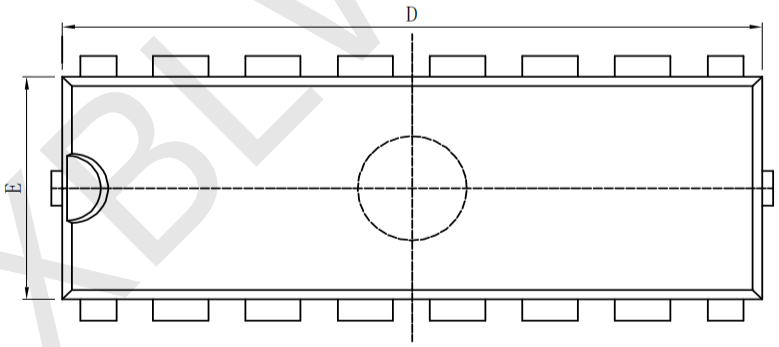
Test Item	Test Conditions	Result
Power Voltage	Vin=8V~40V	3.0mV0.01%
Load Regulation	Vin=12.6V；Io=0.2mA~200mA	5.0mV0.02%
Output Voltage Ripple	Vin=12.6V； Io=200mA	40mVppP.A.R.D
Short-Circuit Current	Vin=12.6V；RL=0.1Ω	250mA
Efficiency	Vin=12.6V；Io=200mA	71%

Package Information

· DIP-16

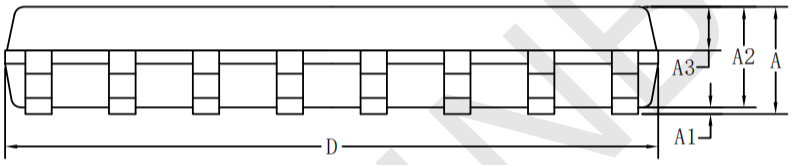
Size / Symbol	Dimensions In Millimeters Min(mm)	Max(mm)	Size / Symbol	Dimensions In Inches Min(in)	Max(in)
A	3.710	4.310	A	0.146	0.170
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.380	0.570	B	0.015	0.022
B1	1.524(BSC)		B1	0.060(BSC)	
C	0.204	0.360	C	0.008	0.014
D	18.80	19.20	D	0.740	0.756
E	6.200	6.600	E	0.244	0.260
E1	7.320	7.920	E1	0.288	0.312
e	2.540(BSC)		e	0.100(BSC)	
L	3.000	3.600	L	0.118	0.142
E2	8.400	9.000	E2	0.331	0.354

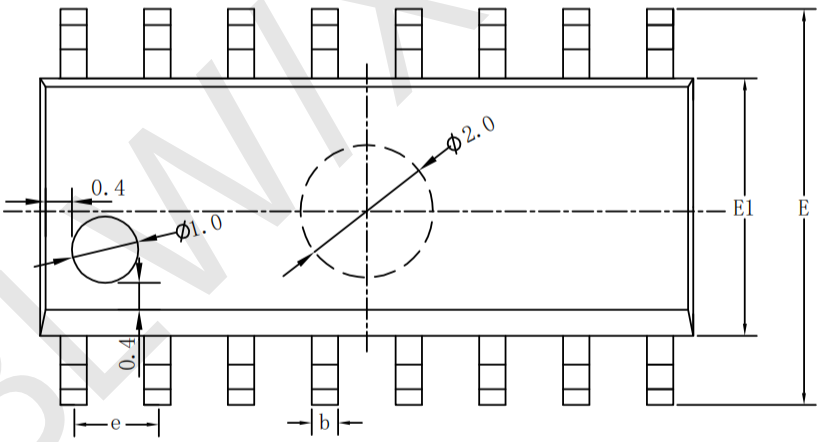


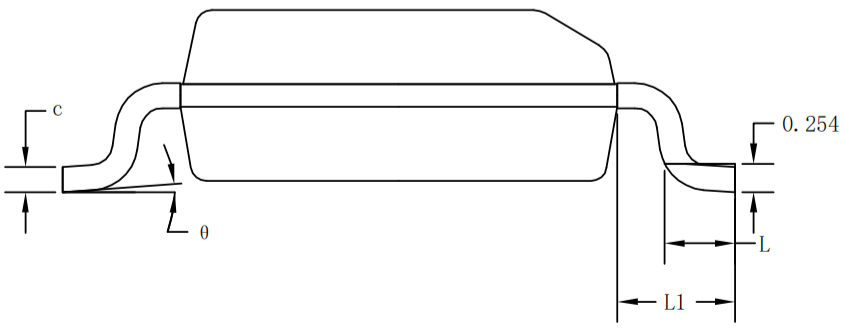


· SOP-16

Size / Symbol	Dimensions In Millimeters			Size / Symbol	Dimensions In Inches		
	Min(mm)	Nom(mm)	Max(mm)		Min(in)	Nom(in)	Max(in)
A	1.500	1.600	1.700	A	0.059	0.063	0.067
A1	0.100	0.150	0.250	A1	0.004	0.006	0.010
A2	1.400	1.450	1.500	A2	0.055	0.057	0.059
A3	0.600	0.650	0.700	A3	0.024	0.026	0.028
b	0.300	0.400	0.500	b	0.012	0.016	0.020
c	0.150	0.200	0.250	c	0.006	0.008	0.010
D	9.800	9.900	10.00	D	0.386	0.390	0.394
E	5.800	6.000	6.200	E	0.228	0.236	0.244
E1	3.850	3.900	3.950	E1	0.152	0.154	0.156
e	1.27(BSC)			e	0.050(BSC)		
L	0.500	0.600	0.700	L	0.020	0.024	0.028
L1	1.05(BSC)			L1	0.041(BSC)		
θ	0°	4°	8°	θ	0°	4°	8°







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