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Circuits from the Lab® Reference Designs for Instrumentation

INTRODUCTION

This instrumentation anthology of circuit notes contains more than 48 Circuits from the Lab designs specifically for analog, mixed-signal, and radio frequency (RF) design challenges within test and measurement applications. Instrumentation engineers can use these circuit notes as standalone solutions, or as foundations for more complex circuits and subsystems.

Built and verified for function and performance by applications experts at Analog Devices, Inc., these circuit designs include

- Comprehensive documentation for easier use with a variety of applications
- Complete design and integration files to minimize system integration issues
- Factory tested evaluation hardware for rapid prototyping with several development platforms

These designs help save time, lower design risk, and improve time to market.

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TABLE OF CONTENTS

REVISION HISTORY

2/2017—Revision 0: Initial Version

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Devices Connected/Referenced	
AD5764	Complete Quad, 16-Bit, High Accuracy DAC
ADR02	Precision 5.0 V Voltage Reference

High Accuracy, Bipolar Voltage Output Digital-to-Analog Conversion Using the AD5764 DAC

CIRCUIT FUNCTION AND BENEFITS

This circuit provides high accuracy, bipolar data conversion using the AD5764, a quad, 16-bit, serial input, bipolar voltage output DAC. This circuit utilizes the ADR02 precision reference to achieve optimal DAC performance over full operating temperature range. The only external components needed for this precision 16-bit DAC are a reference voltage source, decoupling capacitors on the supply pins and reference inputs, and an optional short-circuit current setting resistor leading to savings in cost and board space. This circuit is well suited for both closed-loop servo control and open-loop control applications.

CIRCUIT DESCRIPTION

The AD5764 is a high performance digital-to-analog converter that offers guaranteed monotonicity, integral nonlinearity (INL) of ±1 LSB (C-grade device), low noise, and 10 µs settling time. Performance is guaranteed over wide operating supply voltage ranges. The AV_{DD} supply range is +11.4 V to +16.5 V, and the AV_{SS} operating range is from −11.4 V to −16.5 V. The nominal full-scale output range is ±10 V.

A precision voltage reference must be used in order for the DAC to achieve the optimum performance over its full operating temperature range. The AD5764 incorporates reference buffers, which eliminate the need for both a positive and negative external reference and associated buffers. This leads to further savings in both cost and board space. Because the voltages applied to the reference inputs (REFAB, REFCD) are used to generate the buffered positive and negative internal references for the DAC cores, any error in the external voltage reference is reflected in the outputs of the device.

There are four possible sources of error to consider when choosing a voltage reference for high accuracy applications: initial accuracy, temperature coefficient of the output voltage, long term drift, and output voltage noise. Table 1 lists other 5 V precision reference candidates from Analog Devices and their respective attributes.

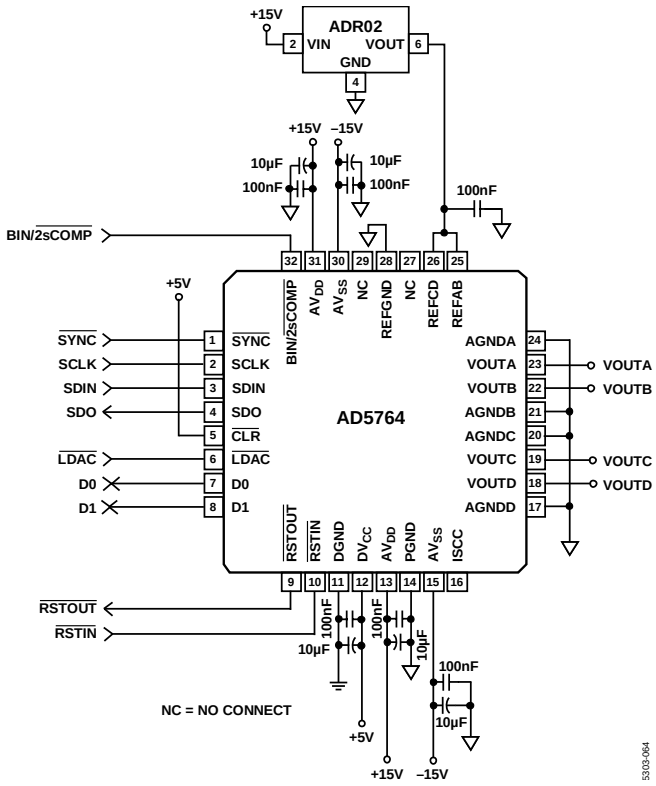

Figure 1. High Accuracy, Bipolar Configuration of the AD5764 DAC Using a Precision Reference

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which the AD5764 is mounted must be designed so that the analog and digital sections are physically separated and confined to certain areas of the board. If the AD5764 is in a system where multiple devices require an AGND-to-DGND connection, the connection is to be made at one point only. The star ground point is established as close as possible to the device. The AD5764 must have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the

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Table 1. Precision 5.0 V References

Part Number	Initial Accuracy Max (mV)	Long-Term Drift Typ (ppm)	Temp Drift Max (ppm/°C)	0.1 Hz to 10 Hz Noise Typ (µV p-p)
ADR435B	±2	40	3	8
ADR425B	±1	50	3	3.4
ADR02B	±3	50	3	10
ADR395B	±5	50	9	8
AD586T	±2.5	15	10	4

tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESL), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply traces of the AD5764 must be as wide as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, must be shielded with digital ground to avoid radiating noise to other parts of the board, and must never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (not required on a multilayer board, which has a separate ground plane; however, it is helpful to separate the lines). It is essential to minimize noise on the reference inputs because it couples through to the DAC output. Avoid crossover of digital and analog signals. Traces on opposite sides of the board must run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is recommended, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the solder side. Best layout and performance are achieved with at least a 4-layer multilayer board, where there is a ground plane layer, a power supply layer, and two signal layers.

LEARN MORE

Kester, Walt. 2005. *The Data Conversion Handbook.* Analog Devices. Chapters 3 and 7.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs.* Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND.* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques.* Analog Devices.

Voltage Reference Wizard Design Tool.

Data Sheets and Evaluation Boards

AD5764 Data Sheet.

AD5764 Evaluation Board.

ADR02 Data Sheet.

REVISION HISTORY

5/09—Rev. 0 to Rev. A

Updated Format.....Universal

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Devices Connected/Referenced	
AD9779A	Dual 16-Bit, 1 GSPS DAC
ADL5370	300 MHz to 1000 MHz I/Q Modulator

Interfacing the ADL5370 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC

CIRCUIT FUNCTION AND BENEFITS

This circuit provides a simple, elegant interface between the ADL5370 I/Q modulator and the AD9779A high speed DAC. The ADL5370 and the AD9779A are well-matched devices because they have the same bias levels and similarly high signal-to-noise ratios (SNR). The matched bias levels of 500 mV allow for a "glueless" interface—there is no requirement for a level shifting network that would add noise and insertion loss along with extra components. The addition of the swing-limiting resistors (RSLI, RSLQ) allows the DAC swing to be scaled appropriately without loss of resolution or of the 0.5 V bias level. The high SNR of each device preserves a high SNR through the circuit.

CIRCUIT DESCRIPTION

The ADL5370 is designed to interface with minimal components to members of Analog Devices family of TxDAC® converters (AD97xx). The baseband inputs of the ADL5370 require a dc common-mode bias voltage of 500 mV. With each AD9779A output swinging from 0 mA to 20 mA, a single 50 Ω resistor to ground from each of the DAC outputs provides the desired 500 mV dc bias. With just the four 50 Ω resistors in place, the voltage swing on each pin is 1 V p-p. This results in a differential voltage swing of 2 V p-p on each input pair.

By adding resistors RSLI and RSLQ to the interface, the output swing of the DAC can be reduced without any loss of DAC resolution. The resistor is placed as a shunt between each side of the differential pair, as shown in Figure 1. It has the effect of reducing the ac swing without changing the dc bias already established by the 50 Ω resistors and the DAC output current.

The value of this ac swing-limiting resistor is chosen based on the desired ac voltage swing. Figure 2 shows the relationship between the swing-limiting resistor and the peak-to-peak ac swing that it produces when 50 Ω bias-setting resistors are used. Note that all Analog Devices I/Q modulators present a relatively high input impedance on their baseband inputs (typically >1 kΩ). As a result, the input impedance of the I/Q modulator will have no effect on the scaling of the DAC output signal.

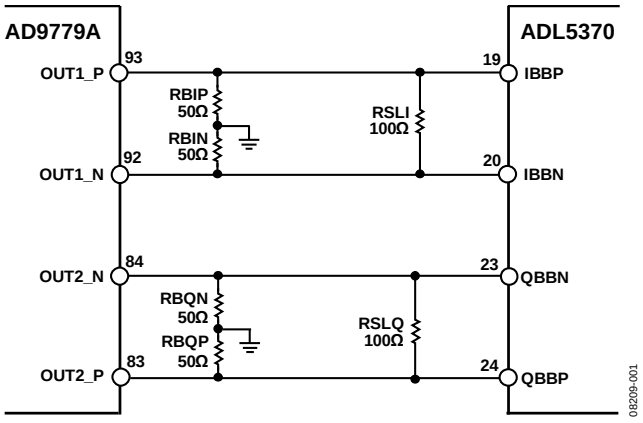

Figure 1. Interface Between the AD9779A and ADL5370 with 50 Ω Resistors to Ground to Establish the 500 mV DC Bias for the ADL5370 Baseband Inputs (Simplified Schematic)

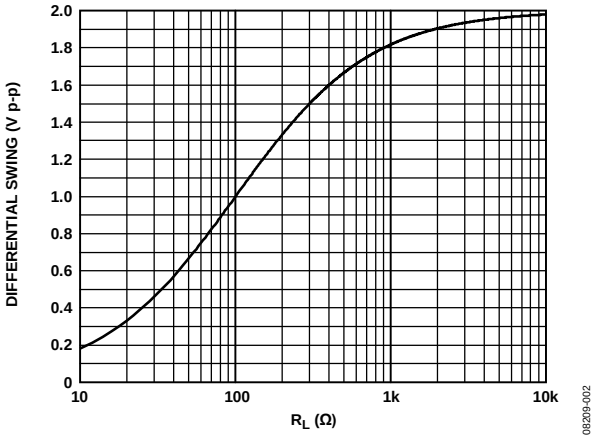

Figure 2. Relationship Between the AC Swing-Limiting Resistor and the Peak-to-Peak Voltage Swing with 50 Ω Bias-Setting Resistors

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It is generally necessary to low-pass filter the DAC outputs to remove image frequencies when driving a modulator. The above interface lends itself well to the introduction of such a filter. The filter can be inserted between the dc bias setting resistors and the ac swing-limiting resistor. Doing so establishes the input and output impedances for the filter.

A simulated filter example is shown in Figure 3 with a third-order elliptical filter with a 3 dB frequency of 3 MHz. Matching input and output impedances makes the filter design easier, so the shunt resistor chosen is 100 Ω, producing an ac swing of 1 V p-p differential for a 0 mA to 20 mA DAC full-scale output current. In a practical application, the use of standard value components, along with the input impedance of the I/Q modulator (2900 kΩ in parallel with a few picofarads of input capacitance), will slightly change the frequency response of this circuit.

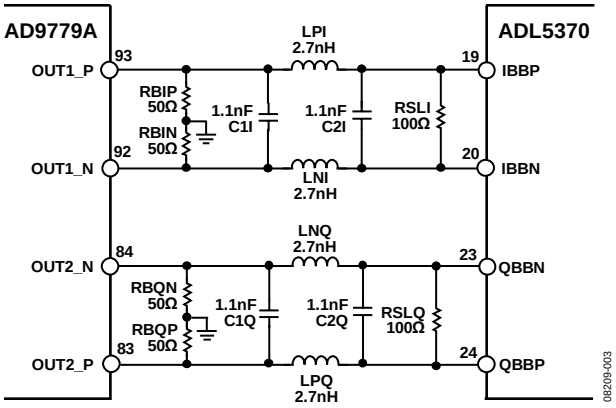

Figure 3. DAC Modulator Interface with 3 MHz Third-Order, Low-Pass Filter (Calculated Component Values)

All the power supply pins of the ADL5370 must be connected to the same 5 V source. Adjacent pins of the same name can be tied together and decoupled to a large area ground plane with a 0.1 µF capacitor. These capacitors should be located as close as possible to the device. The power supply can range between 4.75 V and 5.25 V.

The COM1 pin, COM2 pin, COM3 pin, and COM4 pin should be tied to the same ground plane through low impedance paths. The exposed paddle on the underside of the package should also be soldered to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, they should be stitched together with nine vias under the exposed paddle. The AN-772 application note discusses the thermal and electrical grounding of the LFCSP_VQ in greater detail.

COMMON VARIATIONS

The interface described here can be used to interface any TxDAC converter with ground referenced 0 mA to 20 mA output currents to any I/Q modulator with a 0.5 V input bias level. For zero-IF applications, the AD9783 dual DAC provides an LVDS interface, while the CMOS-driven AD9788 dual DAC can generate a fine resolution complex IF input to the I/Q modulator. The ADL5370/ADL5371/ADL5372/ADL5373/ADL5374 family of I/Q modulators provides narrow-band operation with high output 1 dB compression point and OIP3, whereas the ADL5375 provides broadband high performance operation from 400 MHz to 6 GHz. The ADL5385 I/Q modulator uses a 2 × LO and operates from 50 MHz to 2.2 GHz.

LEARN MORE

AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*. Analog Devices.

MT-016 Tutorial, *Basic DAC Architectures III: Segmented DACs*. Analog Devices.

MT-017 Tutorial, *Oversampling Interpolating DACs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of 'AGND' and 'DGND'*. Analog Devices.

MT-080 Tutorial, *Mixers and Modulators*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Zumbahlen, Hank. 2006. *Basic Linear Design*. Analog Devices. ISBN 0915550281. Chapters 4 and 11. Also available as *Linear Circuit Design Handbook*. Elsevier-Newnes, 2008, ISBN 0750687037, Chapters 4 and 11.

Data Sheets

AD9779A Data Sheet.

ADL5370 Data Sheet.

REVISION HISTORY

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Devices Connected/Referenced	
AD9779A	Dual 16-Bit, 1 GSPS DAC
ADL5375-05	400 MHz to 6000 MHz I/Q Modulator

Interfacing the ADL5375 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC

CIRCUIT FUNCTION AND BENEFITS

This circuit provides a simple, elegant interface between the ADL5375 I/Q modulator and the AD9779A high speed DAC. The ADL5375 and the AD9779A are well-matched devices because they have the same bias levels and similarly high signal-to-noise ratios (SNR). The matched bias levels of 500 mV allow for a "glueless" interface—there is no requirement for a level shifting network that would add noise and insertion loss along with extra components. The addition of the swing-limiting resistors (RSLI, RSLQ) allows the DAC swing to be scaled appropriately without loss of resolution or of the 0.5 V bias level. The high SNR of each device preserves a high SNR through the circuit.

CIRCUIT DESCRIPTION

The ADL5375 is designed to interface with minimal components to members of Analog Devices family of TxDAC® converters (AD97xx). The baseband inputs of the ADL5375 require a dc common-mode bias voltage of 500 mV. With each AD9779A output swinging from 0 mA to 20 mA, a single 50 Ω resistor to ground from each of the DAC outputs provides the desired 500 mV dc bias. With just the four 50 Ω resistors in place, the voltage swing on each pin is 1 V p-p. This results in a differential voltage swing of 2 V p-p on each input pair.

By adding resistors RSLI and RSLQ to the interface, the output swing of the DAC can be reduced without any loss of DAC resolution. The resistor is placed as a shunt between each side of

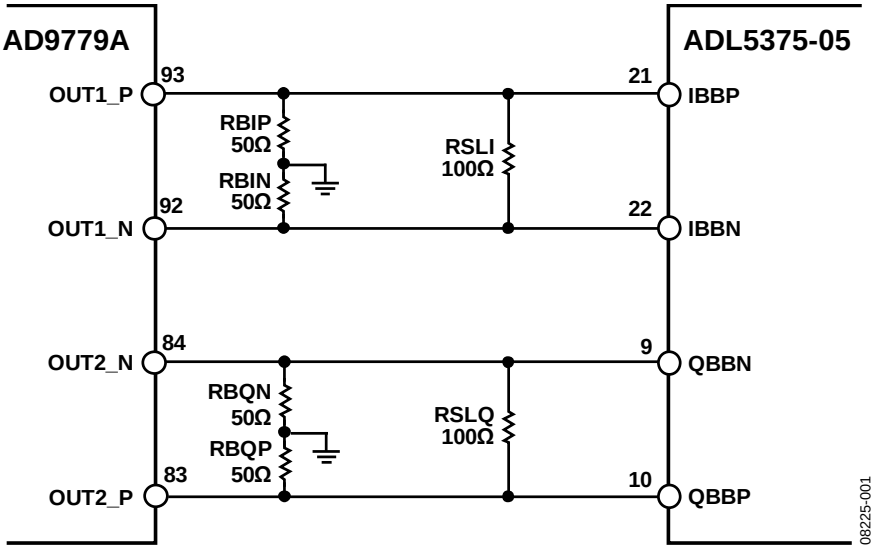

Figure 1. Interface Between the AD9779A and ADL5375 with 50 Ω Resistors to Ground to Establish the 500 mV DC Bias for the ADL5375-05 Baseband Inputs (Simplified Schematic)

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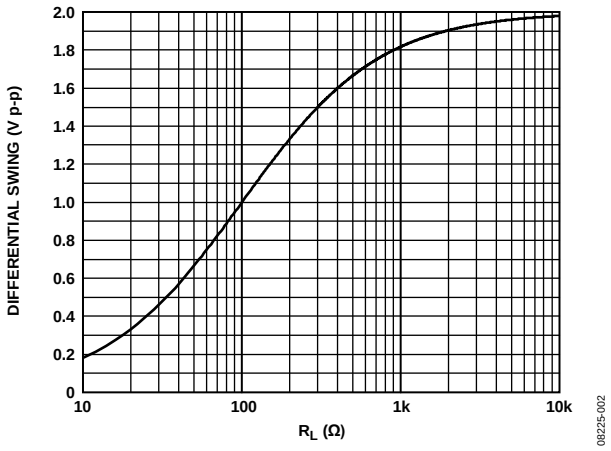

Figure 2. Relationship Between the AC Swing-Limiting Resistor and the Peak-to-Peak Voltage Swing with 50 Ω Bias-Setting Resistors

the differential pair, as shown in Figure 1. It has the effect of reducing the ac swing without changing the dc bias already established by the 50 Ω resistors.

The value of this ac swing-limiting resistor is chosen based on the desired ac voltage swing. Figure 2 shows the relationship between the swing-limiting resistor and the peak-to-peak ac swing that it produces when 50 Ω bias-setting resistors are used. Note that all Analog Devices I/Q modulators present a relatively high input impedance on their baseband inputs (typically >1 kΩ). As a result, the input impedance of the I/Q modulator will have no effect on the scaling of the DAC output signal.

It is generally necessary to low-pass filter the DAC outputs to remove image frequencies when driving a modulator. The above interface lends itself well to the introduction of such a filter. The filter can be inserted between the dc bias setting resistors and the ac swing-limiting resistor. Doing so establishes the input and output impedances for the filter.

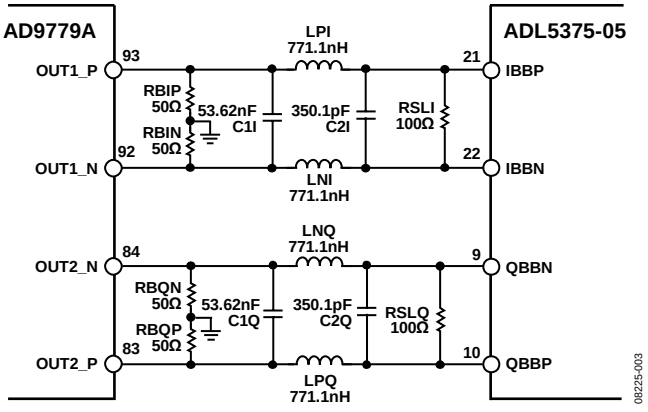

Figure 3. DAC Modulator Interface with 10 MHz Third-Order, Low-Pass Filter (Calculated Component Values)

A simulated filter example is shown in Figure 3 with a third-order elliptical filter with a 3 dB frequency of 10 MHz. Matching input and output impedances makes the filter design easier, so the shunt resistor chosen is 100 Ω, producing an ac swing of 1 V p-p differential for a 0 mA to 20 mA DAC full-scale output current. The simulated frequency response of this filter is shown in Figure 4. In a practical application, the use of standard value components along with the input impedance of the I/Q modulator (2900 kΩ in parallel with a few picofarads of input capacitance), will slightly change the frequency response.

All the power supply pins of the ADL5375 must be connected to the same 5 V source. Adjacent pins of the same name can be tied together and decoupled to a large area ground plane with a 0.1 µF capacitor. These capacitors should be located as close as possible to the device. The power supply can range between 4.75 V and 5.25 V.

The COM1 pin, COM2 pin, COM3 pin, and COM4 pin should be tied to the same ground plane through low impedance paths. The exposed paddle on the underside of the package should also be soldered to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, they should be stitched together with nine vias under the exposed paddle. The AN-772 application note discusses the thermal and electrical grounding of the LFCSP_VQ in greater detail.

COMMON VARIATIONS

The interface described here can be used to interface any TxDAC converter with ground referenced 0 mA to 20 mA output currents to any I/Q modulator with a 0.5 V input bias level. For zero-IF applications, the AD9783 dual DAC provides an LVDS interface, while the CMOS-driven AD9788 dual DAC can generate a fine resolution complex IF input to the I/Q modulator. The ADL5370/ADL5371/ADL5372/ADL5373/

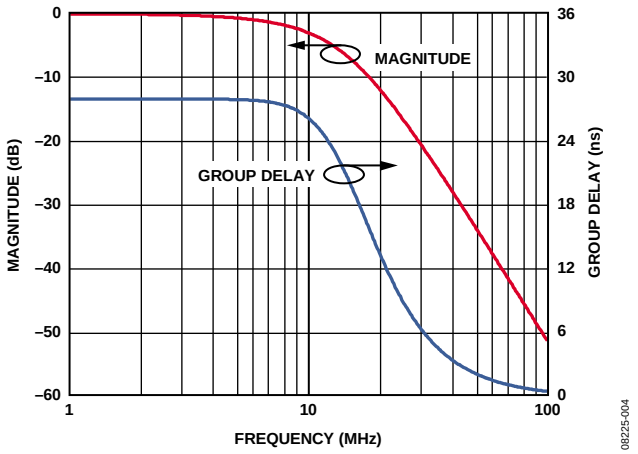

Figure 4. Simulated Frequency Response for DAC Modulator Interface with 10 MHz Third-Order Bessel Filter

ADL5374 family of I/Q modulators provides narrow-band operation with high output 1 dB compression point and OIP3, whereas the ADL5375 provides broadband high performance operation from 400 MHz to 6 GHz. The ADL5385 I/Q modulator uses a 2 × LO and operates from 50 MHz to 2.2 GHz.

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AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*. Analog Devices.

MT-016 Tutorial, *Basic DAC Architectures III: Segmented DACs*. Analog Devices.

MT-017 Tutorial, *Oversampling Interpolating DACs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of 'AGND' and 'DGND'*. Analog Devices.

MT-080 Tutorial, *Mixers and Modulators*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Zumbahlen, Hank. 2006. *Basic Linear Design*. Analog Devices. ISBN 0915550281. Chapters 4 and 11. Also available as *Linear Circuit Design Handbook*. Elsevier-Newnes, 2008, ISBN 0750687037, Chapters 4 and 11.

Data Sheets

AD9779A Data Sheet.

ADL5375 Data Sheet.

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Devices Connected/Referenced	
AD5547/ AD5557	Dual, Current Output, Parallel Input, 16-/14-Bit DAC
ADR03	Precision 2.5 V Voltage Reference
AD8628	Rail-to-Rail Input/Output Operational Amplifier

Precision, Unipolar, Inverting Conversion Using the AD5547/AD5557 DAC

CIRCUIT FUNCTION AND BENEFITS

This circuit provides precision, unipolar, inverting data conversion using the AD5547/AD5557 current output DAC with the ADR03 precision reference and AD8628 operational amplifier (op amp). This circuit provides accurate, low noise, high speed output voltage capability and is well suited for process control, automatic test equipment, and digital calibration applications.

CIRCUIT DESCRIPTION

The AD5547/AD5557 are dual-channel, precision 16-/14-bit, multiplying, low power, current output, parallel input digital-to-analog converters. They operate from a single 2.7 V to 5.5 V supply with ±15 V multiplying references for 4-quadrant outputs. Built-in 4-quadrant resistors facilitate the resistance matching and temperature tracking that minimize the number of components needed for multiquadrant applications.

This circuit uses the ADR03, which is a highly accuracy, high stability, 2.5 V precision voltage reference. As voltage reference temperature coefficient and long-term drift are primary considerations for applications requiring high precision conversion, this device is an ideal candidate.

An op amp is used in the current-to-voltage (I-V) stage of this circuit. An op amp's bias current and offset voltage are both important selection criteria for use with precision current output DACs. Therefore, this circuit employs the AD8628 auto-zero op amp, which has ultralow offset voltage (1 µV typical) and bias current (30 pA typical). The compensation capacitor, C7, is optimized to compensate for the external output capacitance of the DAC.

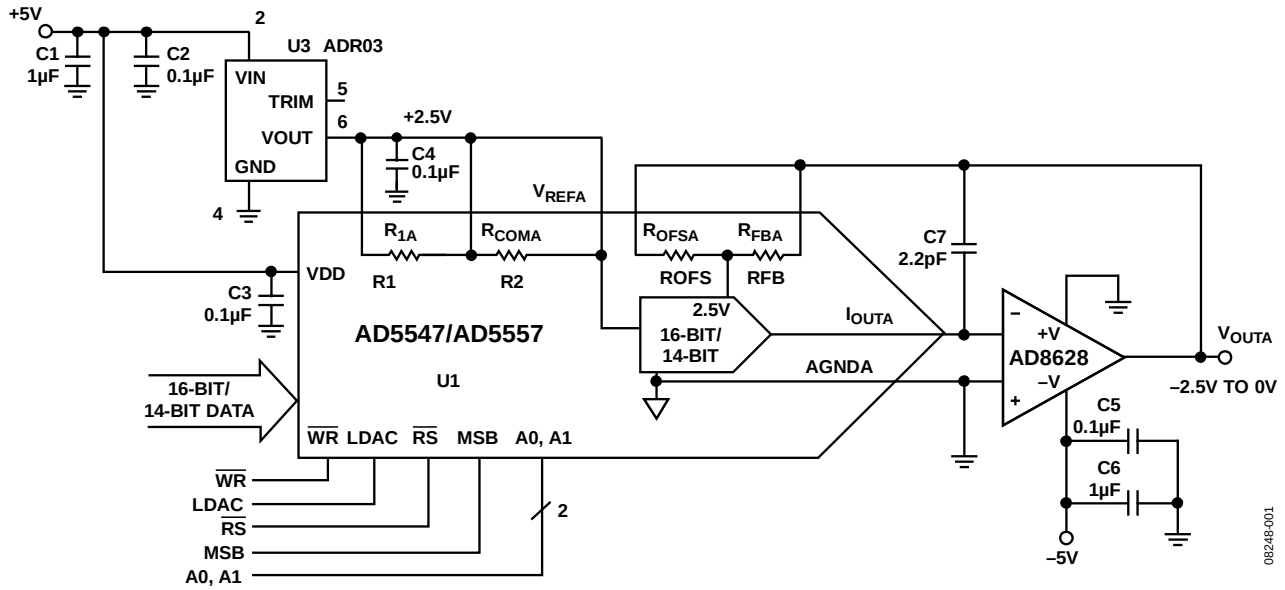

Figure 1. Unipolar 2-Quadrant Multiplying Mode, VOUT = 0 V to –VREF (Simplified Schematic)

Rev. A

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Note that the AD8628 has rail-to-rail input and output stages, but the output can only come within a few millivolts of either rail depending on load current. For the circuit shown, the output can swing from –2.5 V to approximately –1 mV.

The input offset voltage of the op amp is multiplied by the variable noise gain (due to the code-dependent output resistance of the DAC) of the circuit. A change in this noise gain between two adjacent digital codes produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, could cause the DAC to be nonmonotonic. In general, the input offset voltage should be a fraction of an LSB to ensure monotonic behavior when stepping through codes. For the ADR03 and the AD5547, the LSB size is

$$\frac{2.5\ \text{V}}{2^{16}} = 38\ \mu\text{V} \quad (1)$$

The input offset voltage of the AD8628 auto-zero op amp is typically 1 µV, which is negligible compared to the LSB size.

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing through the feedback resistor, RFB. In the case of the AD8628, the input bias current is only 30 pA typical, which flowing through the RFB resistor (10 kΩ typical), produces an error of only 0.3 µV.

The AD5547/AD5557 DAC architecture uses a current-steering R-2R ladder design that requires an external reference and op-amp to convert to an output voltage. VOUT can be calculated for the AD5547 using the equation

$$VOUT = \frac{-VREF \times D}{2^{16}} \quad (2)$$

where D is the decimal equivalent of the input code. VOUT can be calculated for the AD5557 using the equation

$$VOUT = \frac{-VREF \times D}{2^{14}} \quad (3)$$

where D is the decimal equivalent of the input code.

COMMON VARIATIONS

For multichannel applications, the AD8629 is a dual version of the AD8628. The AD8605 is another excellent op amp candidate for the I-V conversion circuit. It also has a low offset voltage and low bias current. The ADR01 and ADR02 are other low noise references available from the same reference family as the ADR03. Other low noise references that would be suitable are the ADR441 and ADR445 products. The size of the reference input voltage is restricted by the rail-to-rail voltage of the op amp selected.

These circuits can also be used as a variable gain element by utilizing the multiplying bandwidth nature of the R-2R structure of the AD5547/AD5557 DAC. In this configuration, remove the external precision reference and apply the signal to be multiplied to the reference input pins of the DAC.

LEARN MORE

ADIsimPower Design Tool.

Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. See chapters 3 and 7.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-033 Tutorial, *Voltage Feedback Op Amp Gain and Bandwidth*. Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*. Analog Devices.

MT-055 Tutorial, *Chopper Stabilized (Auto-Zero) Precision Op Amps*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Data Sheets

AD5547 Data Sheet.

AD5557 Data Sheet.

AD8628 Data Sheet.

ADR03 Data Sheet.

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ADR03	Precision Voltage Reference
AD8628	Rail-to-Rail Input/Output Operational Amplifier

Precision, Unipolar, Noninverting Configuration for the AD5547/AD5557 DAC

CIRCUIT FUNCTION AND BENEFITS

This circuit provides precision, unipolar, noninverting data conversion using the AD5547/AD5557 current output DAC with the ADR03 precision reference and AD8628 operational amplifier (op amp). This circuit provides accurate, low noise, high speed output voltage capability and is well suited for process control, automatic test equipment, and digital calibration applications.

CIRCUIT DESCRIPTION

The AD5547/AD5557 are dual-channel precision 16-/14-bit, multiplying, low power, current output, parallel input digital-to-analog converters. They operate from a single 2.7 V to 5.5 V supply with ±15 V multiplying references for 4-quadrant outputs. Built-in 4-quadrant resistors facilitate the resistance matching and temperature tracking that minimize the number of components needed for multiquadrant applications.

This circuit uses the ADR03, which is a highly accuracy, high stability, 2.5 V precision voltage reference. As voltage reference temperature coefficient and long-term drift are primary considerations for applications requiring high precision conversion, this device is an ideal candidate.

An op amp is used in the current-to-voltage (I-V) stage of this circuit. An op amp's bias current and offset voltage are both important selection criteria for use with precision current output DACs. Therefore, this circuit employs the AD8628 auto-zero op amp, which has ultralow offset voltage (1 µV typical) and bias current (30 pA typical). C7 is a compensation capacitor. The value of C7 for this application is 2.2 pF, which is optimized to compensate for the external output capacitance of the DAC.

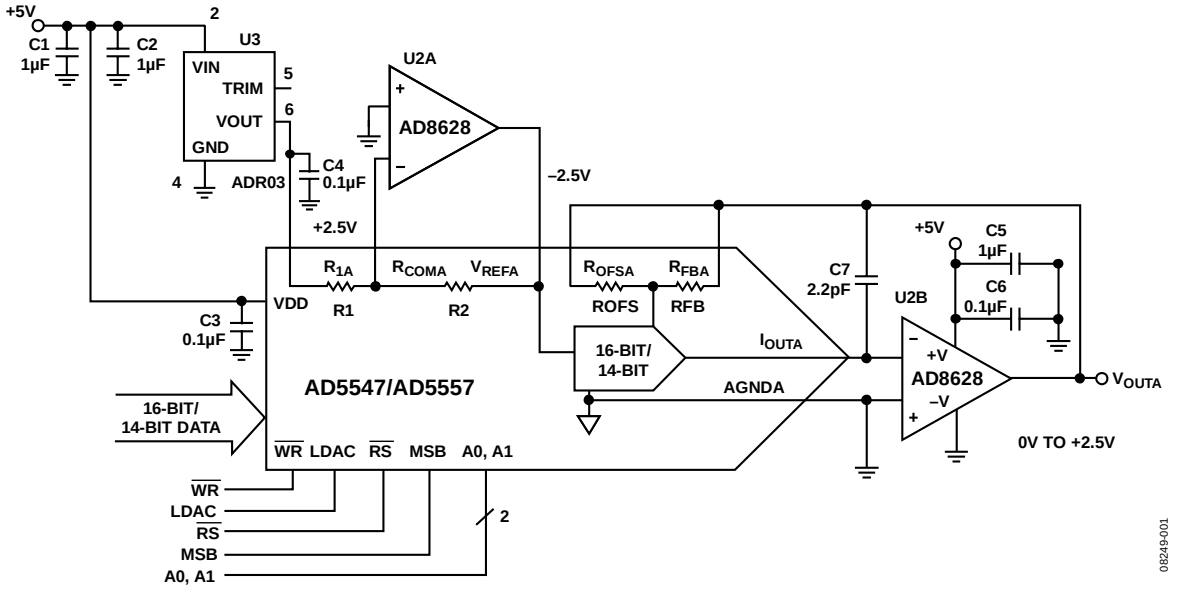

Figure 1. Unipolar 2-Quadrant Multiplying Mode, VOUT = 0 V to +VREF (Simplified Schematic)

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Note that the AD8628 has rail-to-rail input and output stages, but the output can only come within a few millivolts of either rail depending on load current. For the circuit shown, the output can swing from approximately +1 mV to +2.5 V.

The input offset voltage of the op amp is multiplied by the variable noise gain (due to the code-dependent output resistance of the DAC) of the circuit. A change in this noise gain between two adjacent digital codes produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, could cause the DAC to be nonmonotonic. In general, the input offset voltage should be a fraction of an LSB to ensure monotonic behavior when stepping through codes. For the ADR03 and the AD5547, the LSB size is

$$\frac{2.5\ \text{V}}{2^{16}} = 38\ \mu\text{V} \quad (1)$$

The input offset voltage of the AD8628 auto-zero op amp is typically 1 µV, which is negligible compared to the LSB size.

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing through the feedback resistor, RFB. In the case of the AD8628, the input bias current is only 30 pA typical, which flowing through the RFB resistor (10 kΩ typical) produces an error of only 0.3 µV.

The AD5547/AD5557 DAC architecture uses a current-steering R-2R ladder design that requires an external reference and op-amp to convert to an output voltage. VOUT can be calculated for the AD5547 using the equation

$$VOUT = \frac{+VREF \times D}{2^{16}} \quad (2)$$

where D is the decimal equivalent of the input code. VOUT can be calculated for the AD5557 using the equation

$$VOUT = \frac{+VREF \times D}{2^{14}} \quad (3)$$

where D is the decimal equivalent of the input code.

COMMON VARIATIONS

The AD8629 is a dual version of the AD8628. The AD8605 is another excellent op amp candidate for the I-V conversion circuit. It also has a low offset voltage and low bias current. The ADR01 and ADR02 are other low noise references available from the same reference family as the ADR03. Other low noise references that would be suitable are the ADR441 and ADR445 products. The size of the reference input voltage is restricted by the rail-to-rail voltage of the op amp selected.

These circuits can also be used as a variable gain element by utilizing the multiplying bandwidth nature of the R-2R structure of the AD5547/AD5557 DAC. In this configuration, remove the external precision reference and apply the signal to be multiplied to the reference input pins of the DAC.

LEARN MORE

ADIsimPower Design Tool.

Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. See chapters 3 and 7.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-033 Tutorial, *Voltage Feedback Op Amp Gain and Bandwidth*. Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*. Analog Devices.

MT-055 Tutorial, *Chopper Stabilized (Auto-Zero) Precision Op Amps*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Data Sheets

AD5547 Data Sheet.

AD5557 Data Sheet.

AD8628 Data Sheet.

ADR03 Data Sheet.

REVISION HISTORY

5/09—Rev. 0 to Rev. A

Updated Format.....Universal

10/08—Revision 0: Initial Version

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Devices Connected/Referenced	
AD5547/ AD5557	Dual, Current Output, Parallel Input, 16-/14-Bit DAC
AD8512	Low Noise, Low Input Bias, JFET Operational Amplifier
ADR01	Ultracompact, Precision 10.0 V Voltage Reference

Precision, Bipolar, Configuration for the AD5547/AD5557 DAC

CIRCUIT FUNCTION AND BENEFITS

This circuit provides precision, bipolar data conversion using the AD5547/AD5557 current output DAC with the ADR01 precision reference and AD8512 operational amplifier (op amp). This circuit provides accurate, low noise, high speed output voltage capability and is well suited for process control, automatic test equipment, and digital calibration applications.

CIRCUIT DESCRIPTION

The AD5547/AD5557 are dual-channel, precision 16-/14-bit, multiplying, low power, current output, parallel input digital-to-analog converters. They operate from a single 2.7 V to 5.5 V supply with ±15 V multiplying references for 4-quadrant outputs. Built-in 4-quadrant resistors facilitate the resistance matching and temperature tracking that minimize the number of components needed for multiquadrant applications.

This circuit uses the ADR01, which is a highly accuracy, high stability, 10 V precision voltage reference. As voltage reference temperature coefficient and long-term drift are primary considerations for applications requiring high precision conversion, this device is an ideal candidate.

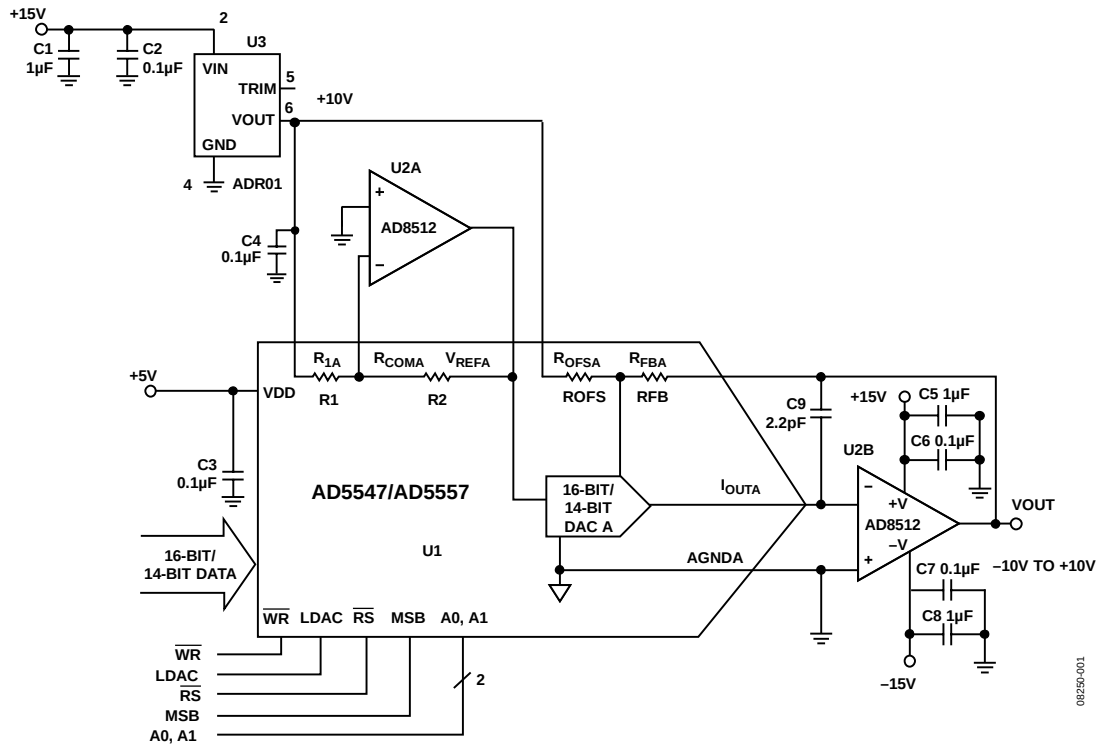

Figure 1. 4-Quadrant Multiplying Mode, VOUT = –VREF to +VREF (Simplified Schematic)

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An op amp is used in the current-to-voltage (I-V) stage of this circuit. An op amp's bias current and offset voltage are both important selection criteria for use with precision current output DACs. Therefore, this circuit employs the AD8512 op amp, which has ultralow offset voltage (80 µV typical for B-grade device) and bias current (25 pA typical). C9 is a compensation capacitor. The value of C9 for this application is 2.2 pF, which is optimized to compensate for the external output capacitance of the DAC.

The input offset voltage of the op amp is multiplied by the variable noise gain (due to the code-dependent output resistance of the DAC) of the circuit. A change in this noise gain between two adjacent digital codes produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, could cause the DAC to be nonmonotonic. In general, the input offset voltage should be a fraction of an LSB to ensure monotonic behavior when stepping through codes. For the ADR01 and the AD5547, the LSB size is

$$\frac{10\ \text{V}}{2^{16}} = 153\ \mu\text{V} \quad (1)$$

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing through the feedback resistor, RFB. In the case of the AD8512, the input bias current is only 25 pA typical, which flowing through the RFB resistor (10 kΩ typical) produces an error of only 0.25 µV.

The AD5547/AD5557 DAC architecture uses a current-steering R-2R ladder design that requires an external reference and op-amp to convert to an output voltage. VOUT can be calculated for the AD5547 using the equation

$$VOUT = \left[\frac{VREF \times D}{2^{16-1}}\right] - VREF \quad (2)$$

where D = 0 to 65535 for 16-bit DAC (D is the decimal equivalent of the input code). VOUT can be calculated for the AD5557 using the equation

$$VOUT = \left[\frac{VREF \times D}{2^{14-1}}\right] - VREF \quad (3)$$

where D = 0 to 16383 for 14-bit DAC (D is the decimal equivalent of the input code).

COMMON VARIATIONS

The AD8605 is another excellent op amp candidate for the I-V conversion circuit. It also has a low offset voltage and low bias current. The ADR02 and ADR03 are other low noise references available from the same reference family as the ADR01. Other low noise references that would be suitable are the ADR441 and ADR445 products. The size of the reference input voltage is restricted by the rail-to-rail voltage of the op amp selected.

These circuits can also be used as a variable gain element by utilizing the multiplying bandwidth nature of the R-2R structure of the AD5547/AD5557 DAC. In this configuration, remove the external precision reference and apply the signal to be multiplied to the reference input pins of the DAC.

LEARN MORE

ADIsimPower Design Tool.

Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. See chapters 3 and 7.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-033 Tutorial, *Voltage Feedback Op Amp Gain and Bandwidth*. Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*. Analog Devices.

MT-055 Tutorial, *Chopper Stabilized (Auto-Zero) Precision Op Amps*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Data Sheets

AD5547 Data Sheet.

AD5557 Data Sheet.

AD8512 Data Sheet.

ADR01 Data Sheet.

REVISION HISTORY

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10/08—Revision 0: Initial Version

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Devices Connected/Referenced	
AD5390/ AD5391/ AD5392	3 V/5 V, 16-/14-/12-Bit Digital-to-Analog Converter
AD7476	1 MSPS, 12-Bit ADC
AD780	Precision 2.5 V/3.0 V Voltage Reference
ADR431	Precision 2.5 V Voltage Reference

AD5390/AD5391/AD5392 Channel Monitor Function

CIRCUIT FUNCTION AND BENEFITS

In a multichannel DAC system, the ability to monitor all outputs at a single point is a significant advantage for troubleshooting and diagnostic analysis. This circuit provides multichannel DAC output channel monitoring using a single-channel SAR ADC.

CIRCUIT DESCRIPTION

This circuit utilizes the internal multiplexer on the AD5390/ AD5391/AD5392 to route any of the DAC output channels to a single output pin (MON_OUT) for monitoring by the external ADC (AD7476). This approach utilizes much less circuitry than would be required if each channel were monitored individually.

The AD5390/AD5391 are complete, single-supply, 16-channel, 14-bit and 12-bit DACs, respectively. The AD5392 is a complete single-supply, 8-channel, 14-bit DAC. Devices are available both in 64-lead LFCSP and 52-lead LQFP packages. All channels have an on-chip output amplifier with rail-to-rail operation. The AD5390/AD5391/AD5392 contain a channel monitor function that consists of a multiplexer addressed via the serial interface, allowing any channel output to be routed to the monitor output (MON_OUT) pin for monitoring using an external ADC. The channel monitor function must be enabled in the control register before any channels are routed to MON_OUT. The AD5390/AD5391/AD5392 also include two uncommitted inputs (MON_IN1 and MON_IN2) to the internal multiplexer that allow the user the facility to monitor inputs from external sources such as references or power supplies. In Figure 1, the MON_IN1 pin on the AD5390 monitors the reference voltage from the AD780/ADR431.

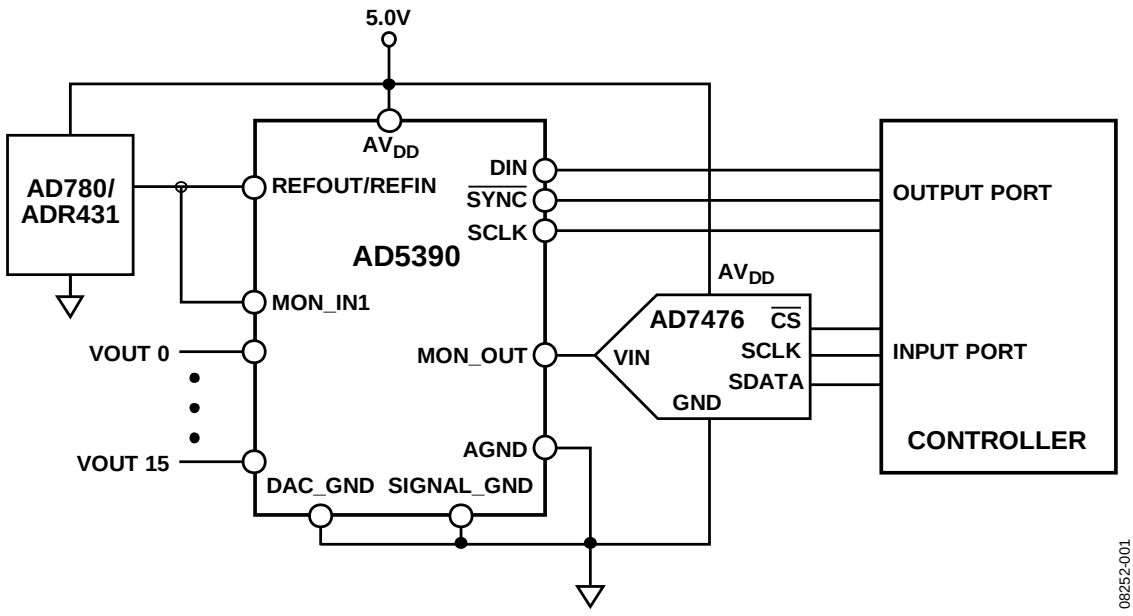

Figure 1. Efficient Channel Monitoring Circuit (Simplified Schematic)

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The AD7476 ADC is a SAR ADC that offers 12-bit resolution, single 2.35 V to 5.25 V power supply, integrated reference, low power operation, small form factor, and serial interface, with throughput rates up to 1 MSPS in a 6-lead SOT-23 package. The reference for the part is taken internally from VDD, allowing the widest dynamic input range to the ADC. Thus, the analog input range for the part is 0 V to VDD. The conversion rate is determined by the SCLK, allowing throughput rates up to 1 MSPS.

The combination of the AD5390/AD5391/AD5392 and AD7476 provides a complete 8- or 16-channel analog output control solution with an efficient monitor function for system debug and fault and diagnostic analysis.

The AD5390/AD5391/AD5392 and the AD7476 must have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply pin, located as close to the packages as possible, ideally right up against the devices (this is not shown on the simplified diagram). The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESL), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply traces should be as wide as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, must be shielded with ground runs to avoid radiating noise to other parts of the board and must never be run near the analog signals. A ground line routed between the SDATA and SCLK lines helps reduce crosstalk between them (not required on a multilayer board, which has a separate ground plane; however, it is helpful to separate the lines). Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is recommended but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the solder side. Best layout and performance is achieved with at least a 4-layer multilayer board, where there is a ground plane layer, a power supply layer, and two signal layers.

COMMON VARIATIONS

Pin-compatible versions of the AD7476 are available for use in applications where lower resolution conversion is acceptable in the monitoring function. The AD7477 provides 10-bit resolution, and the AD7478 provides 8-bit resolution. The ADR431 reference can be substituted for the AD780.

LEARN MORE

ADIsimPower Design Tool.

Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. See chapters 3 and 7.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Voltage Reference Wizard Design Tool

Data Sheets and Evaluation Boards

AD5390 Data Sheet.

AD5391 Data Sheet.

AD5392 Data Sheet.

AD7476 Data Sheet.

AD780 Data Sheet.

ADR431 Data Sheet.

AD5390/AD5391/AD5392 Evaluation Board.

REVISION HISTORY

6/09—Rev. 0 to Rev. A

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11/08—Revision 0: Initial Version

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Devices Connected/Referenced	
AD7982	18-Bit, 1 MSPS PulSAR® 7.0 mW ADC
ADR435	Ultralow Noise XFET® 5.0 V Voltage Reference
ADA4941-1	Single-Supply, Differential 18-Bit ADC Driver

Converting a Single-Ended Signal with the AD7982 Differential PulSAR ADC

CIRCUIT FUNCTION AND BENEFITS

There are many applications that require a single-ended analog signal, either bipolar or unipolar, to be converted by a high resolution, differential input ADC. This dc-coupled circuit converts a single-ended input signal to a differential signal suitable for driving the AD7982, an 18-bit, 1 MSPS member of the PulSAR family of ADCs. This circuit uses the ADA4941-1 single-ended-to-differential driver and the ADR435 ultralow noise 5.0 V voltage reference. The circuit can accept many types of single-ended input signals, including bipolar or unipolar, ranging from high voltage to low voltage. Direct coupling is maintained throughout. If board space is at a premium, all the ICs shown in Figure 1 come in small packages, either 3 mm × 3 mm LFCSP or 3 mm × 5 mm MSOP.

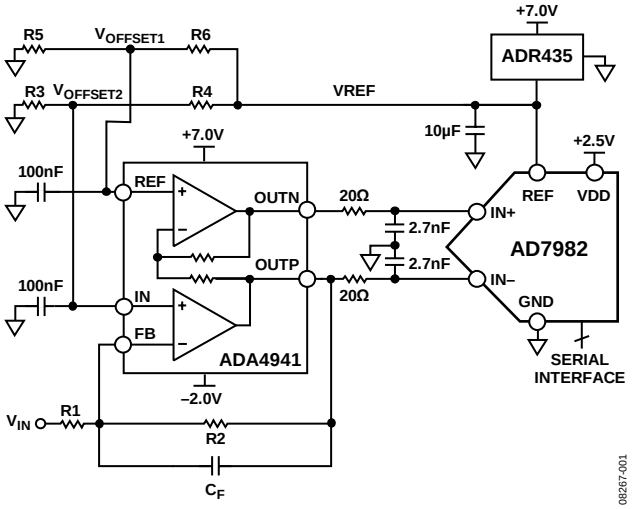

Figure 1. Single-Ended–to- Differential DC-Coupled Driver Circuit (Simplified Schematic)

CIRCUIT DESCRIPTION

The differential input voltage range of the AD7982 is set by the voltage on the REF pin. For V_{REF} = 5 V, the differential input voltage range is $\pm V_{REF}$ = ±5 V. The voltage gain (or attenuation) from the single-ended source, V_{IN}, to OUTP of the ADA4941-1 is set by the ratio of R2 to R1. The ratio of R2 to R1 should be equal to the ratio of V_{REF} to the peak-to-peak input voltage at V_{IN}. For a peak-to-peak, single-ended input voltage of 10 V and V_{REF} = 5 V, the ratio of R2 to R1 should be 0.5. The signal at OUTP is inverted (gain = −1) by the upper half of the ADA4941-1, which supplies the opposite phase output signal at OUTN. The absolute value of R1 determines the input impedance of the circuit. Feedback capacitor C_F is chosen based on the desired signal bandwidth, which is approximately $1/(2\pi R2C_F)$. The 20 Ω resistors and the 2.7 nF capacitors act as a 3 MHz single-pole low-pass noise filter.

Resistors R3 and R4 set the common-mode voltage on the IN− input of the AD7982. The value of this common-mode voltage is $V_{OFFSET2} \times (1 + R2/R1)$, where $V_{OFFSET2} = V_{REF} \times R3/(R3 + R4)$. Resistors R5 and R6 set the common-mode voltage on the IN+ input of the ADC. This voltage is equal to$V_{OFFSET1} = V_{REF} \times R5/(R5 + R6)$. The ADC's common-mode voltage, which is equal to $V_{OFFSET1}$, should be close to $V_{REF}/2$. This implies that R5 = R6. Table 1 shows some possible standard 1% values for the resistors for popular input voltage ranges.

Note that the ADA4941-1 operates on supply voltages of +7 V and −2 V. Since each output must swing from 0 V to +5 V, the positive supply voltage should be a few hundred millivolts greater than +5 V and the negative supply should be a few hundred millivolts more negative than 0 V. For this circuit, supply voltages of +7 V and −2 V were chosen. The +7 V supply

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Table 1. Circuit Values and Voltages for Popular Input Voltage Ranges

V_{IN} (V)	$V_{OFFSET1}$ (V)	$V_{OFFSET2}$ (V)	OUTP (V)	OUTN (V)	R1 (kΩ)	R2 (kΩ)	R4(kΩ)	R3, R5, R6 (kΩ)
+20, −20	2.5	2.203	−0.01, 4.96	5.0, 0.04	8.06	1.00	12.70	10.00
+10, −10	2.5	2.000	0.01, 4.99	4.99, 0.01	4.02	1.00	15.0	10.00
+5, −5	2.5	1.667	0.00, 5.00	5.00, 0.00	2.00	1.00	20.0	10.00

also provides sufficient headroom to power the ADR435. Other voltages are possible, provided the absolute maximum total supply voltage on the AD4941-1 does not exceed 12 V and the headroom requirement of the ADR435 is observed.

The AD7982 requires a +2.5 V supply for V_{DD} as well as a V_{IO} supply (not shown in Figure 1), which can range between 1.8 V and 5 V, depending upon the I/O logic interface levels.

This circuit is not sensitive to power supply sequencing. The AD7982 inputs can withstand up to ±130 mA maximum during momentary overvoltage conditions.

The AD7982 SPI-compatible serial interface (not shown in Figure 1) features the ability, using the SDI input, to daisy-chain several ADCs on a single 3-wire bus and provides an optional busy indicator. It is compatible with 1.8 V, 2.5 V, 3 V, and 5 V logic, using the separate V_{IO} supply.

Excellent layout, grounding, and decoupling techniques must be utilized in order to achieve the desired performance from the circuits discussed in this note. As a minimum, a 4-layer PCB should be used with one ground plane layer, one power plane layer, and two signal layers.

All IC power pins must be decoupled to the ground plane with low inductance, multilayer ceramic capacitors (MLCC) of 0.01 µF to 0.1 µF (this is not shown in Figure 1 for simplicity). Follow the recommendations on the individual data sheets for the ICs referenced in the Learn More section.

The product evaluation boards should be consulted for recommended layout and critical component placement. These can be accessed through the main product pages for the devices (see the Learn More section).

COMMON VARIATIONS

For different reference voltages, the ADR43x family of references has a wide range of values that can interface with the ADC.

LEARN MORE

Kester, Walt. 2005. *The Data Conversion Handbook*. Chapters 6 and 7. Analog Devices.

Kester, Walt. 2006. *High Speed System Applications*. Analog Devices. Chapter 2, "Optimizing Data Converter Interfaces."

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*. Analog Devices.

MT-074 Tutorial, *Differential Drivers for Precision ADCs*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Voltage Reference Wizard Design Tool.

Data Sheets and Evaluation Boards

AD7982 Data Sheet.

AD7982 Evaluation Board.

ADA4941-1 Data Sheet.

ADR435 Data Sheet.

REVISION HISTORY

7/09—Rev. 0 to Rev. A

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Devices Connected/Referenced	
AD7356	Differential Input, Dual, 5 MSPS, 12-Bit SAR ADC
AD8138	Low Distortion Differential ADC Driver
OP177	Ultraprecision Operational Amplifier

DC-Coupled, Single-Ended-to-Differential Conversion Using the AD8138 Low Distortion Differential ADC Driver and the AD7356 5 MSPS, 12-Bit SAR ADC

CIRCUIT FUNCTION AND BENEFITS

This circuit provides a dc-coupled, single-ended-to-differential conversion of a bipolar input signal to the AD7356 5 MSPS, 12-bit successive approximation register (SAR) analog-to-digital converter (ADC). This circuit is designed to ensure maximum performance of the AD7356 by providing adequate settling time and low impedance.

CIRCUIT DESCRIPTION

Differential operation requires V_{INx+} and V_{INx-} of the ADC to be driven simultaneously with two equal signals that are 180° out of phase and are centered around the proper common-mode voltage. Because not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended-to-differential conversion. An ideal method of applying differential drive to the AD7356 is to use a differential amplifier, such as the AD8138. The AD8138 can be used as a single-ended-to-differential amplifier or as a differential-to-differential amplifier. It also provides common-mode level shifting. Figure 1 shows how the AD8138 can be used as a single-ended-to-differential amplifier in a dc-coupled application. The positive and negative outputs of the AD8138 are connected to the respective inputs on the ADC through a pair of series resistors to minimize the loading effects of the switched capacitor inputs of the ADC. The architecture of the AD8138 results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components. The single-ended-to-differential gain of the circuit in Figure 1 is equal to R_F/R_G, where $R_F = R_F1 = R_F2$ and $R_G = R_G1 = R_G2$.

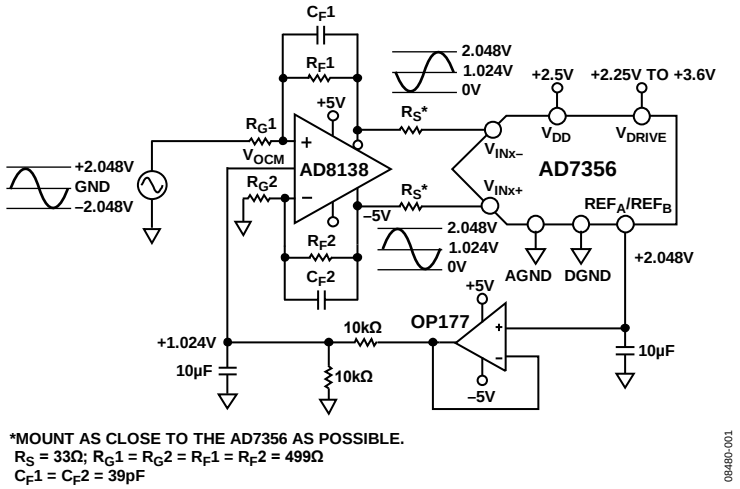

Figure 1. AD8138 as a DC-Coupled, Single-Ended-to-Differential Converter Driving the AD7356 Differential Inputs (Simplified Schematic: Decoupling and All Connections Not Shown)

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If the analog inputs source being used has zero impedance, all four resistors (R_G1, R_G2, R_F1, and R_F2) should be the same as is shown in Figure 1. If the source has a 50 Ω impedance and a 50 Ω termination, for example, increase the value of R_G2 by 25 Ω to balance this parallel impedance on the input and thus ensure that both the positive and negative analog inputs have the same gain. This also requires a small increase in R_F1 and R_F2 to compensate for the gain loss caused by increasing R_G1 and R_G2. Complete analysis for the terminated source condition is found in the ADIsimDiffAmp interactive design tool and in the MT-076 Tutorial.

The AD7356 requires a driver that has a very fast settling time due to the very short acquisition time required achieving 5 MSPS throughput with a serial interface. The track-and-hold amplifier on the front end of the AD7356 enters track mode on the rising edge of the 13th SCLK period during a conversion. The ADC driver must settle before the track-and-hold returns to hold (38 ns later for 5 MSPS throughput on the AD7356 using an 80 MHz SCLK). The AD8138 has a specified 16 ns settling time that satisfies this requirement.

The voltage applied to the V_{OCM} pin of the AD8138 sets up the common-mode voltage. In Figure 1, V_{OCM} is connected to 1.024 V, which is a divided version of the internal 2.048 V reference on the AD7356. If the on-chip 2.048 V reference on the AD7356 is to be used elsewhere in a system (as illustrated in Figure 1), the output from REF_A or REF_B must first be buffered. The OP177 features the highest precision performance of any op amp currently available and is a perfect choice for a reference buffer.

Note that, in Figure 1, the AD8138 operates on dual 5 V supplies whereas the AD7356 is specified for power supply voltages of 2.25 V to 3.6 V. Care must be taken to ensure that the maximum input voltage limits of the AD7356 are not exceeded during transient or power-on conditions (see MT-036 Tutorial). In addition, the circuit must be constructed on a multilayer printed circuit board (PCB) with a large area ground plane. Proper layout, grounding, and decoupling techniques must be used to achieve optimum performance (see MT-031 Tutorial, MT-101 Tutorial, and the AD7356 evaluation board layout).

COMMON VARIATIONS

The OP07D, an ultralow offset voltage op amp, is a lower cost alternative to the OP177. It offers similar performance with the exception of the offset voltage specification. Alternatively, the AD8628 or the AD8638 offers very high precision with very low drift with time and temperature.

LEARN MORE

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND,"* Analog Devices.

MT-036 Tutorial, *Op Amp Output Phase-Reversal and Input Over-Voltage Protection*, Analog Devices.

MT-074 Tutorial, *Differential Drivers for Precision ADCs*, Analog Devices.

MT-075 Tutorial, *Differential Drivers for High Speed ADCs Overview*, Analog Devices.

MT-076 Tutorial, *Differential Driver Analysis*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

John Ardizonni and Jonathan Pearson, "*Rules of the Road" for High-Speed Differential ADC Drivers* (Analog Dialogue, Volume 43, May 2009, Analog Devices).

ADIsimDiffAmp (Differential Amplifier Tool), Analog Devices.

Data Sheets and Evaluation Boards

AD7356 Data Sheet.

AD7356 Evaluation Board.

AD8138 Data Sheet.

OP177 Data Sheet.

OP07D Data Sheet.

REVISION HISTORY

1/13—Rev. A to Rev. B

Changes to Figure 1 1

11/09—Rev. 0 to Rev. A

Updated Format ..... Universal

Changes to Circuit Note Title 1

2/09—Revision 0: Initial Release

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Devices Connected/Referenced	
AD7366/ AD7367	Bipolar Input, Dual 12-/14-Bit, 2-Channel, SAR ADC
AD8021	Low Noise, High Speed Amplifier

Driving the AD7366/AD7367 Bipolar SAR ADC in Low-Distortion DC-Coupled Applications

CIRCUIT FUNCTION AND BENEFITS

The circuit described in this document provides single-ended, low-distortion sampling of an industrial level, dc-coupled signal. The driver circuit shown in Figure 1 is optimized for applications requiring best distortion performance. Maximum AD7366/AD7367 performance is achieved by providing adequate settling time and low impedance in the circuit.

CIRCUIT DESCRIPTION

The AD7366 and the AD7367 are, respectively, 12-bit and 14-bit, 1 MSPS, 2-channel, simultaneous sampling SAR ADCs. These devices have a total of four analog multiplexed inputs (two per channel), which operate in single-ended mode. The analog input range on the AD7366/AD7367 is programmable and can support ±10 V, ±5 V, and 0 V to 10 V using the internal 2.5 V reference. An analog input range of ±12 V requires a 3 V external reference.

The AD7366/AD7367 are fabricated on the Analog Devices, Inc., industrial CMOS process (*i*CMOS), which is a technology platform combining the advantages of low and high voltage CMOS. The input circuits of the AD7366/AD7367 operate on V_{DD} and V_{SS} voltages of ±12 V nominal, while the rest of the ADC operates on an AV_{CC}, a DV_{CC}, and a V_{DRIVE} of +5 V. The *i*CMOS process, therefore, allows the AD7366/AD7367 to accept high voltage bipolar signals in addition to reducing power consumption and package size.

In applications where the signal source has high impedance, analog input signals should be buffered before being applied to the inputs of the AD7366/AD7367 because large source impedances significantly affect the ac performance of the ADC. The choice of the op amp used to drive the inputs is a function of the particular application and depends on the analog input voltage range selected. The driver amplifier must be able to settle for a full-scale step to a 14-bit level (0.0061%) for the AD7367 or a 12-bit level (0.024%) for the AD7366 in less than the specified acquisition time of 140 ns.

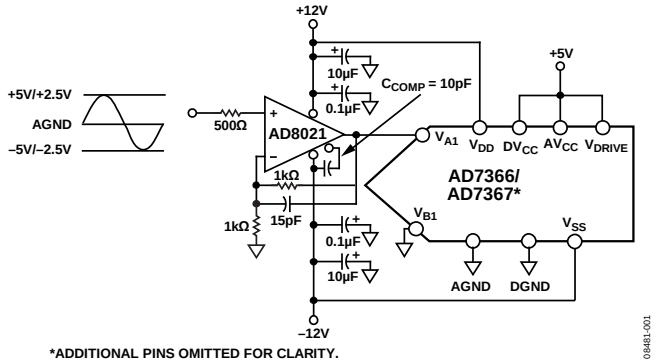

Figure 1. Typical Connection Diagram with the AD8021 for Driving the Analog Inputs of the AD7366/AD7367 (Simplified Schematic, Decoupling and All Connections Not Shown)

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The AD8021 high performance voltage feedback op amp is an ideal choice as a single-ended input buffer/driver for the AD7366/AD7367 due to its exceptionally high performance, high speed, low noise, and low distortion performance. It also meets the above stated requirement when operating in single-ended mode. Figure 1 shows the configuration of the AD7366/AD7367 with the AD8021 in a single-ended configuration. The AD8021 needs an external compensating NPO type capacitor (C_{COMP}), as indicated in Figure 1. The AD8021 is connected in the noninverting mode with a gain of 2. The AD7366/AD7367 programmable bipolar input voltage ranges (referenced to the input of the AD8021) are ±5 V and ±2.5 V.

The circuit must be constructed on a multilayer PC board with a large area ground plane. Proper layout, grounding, and decoupling techniques must be used to achieve optimum performance (see MT-031 Tutorial, MT-101 Tutorial, and the AD7366/AD7367 evaluation board layout).

COMMON VARIATIONS

The AD8022 is a suitable replacement for the AD8021 in high frequency applications where a dual version is required. For lower frequency applications, recommended op amps are the AD797, AD845, and AD8610.

LEARN MORE

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND."* Analog Devices.

MT-036 Tutorial, *Op Amp Output Phase-Reversal and Input Over-Voltage Protection.* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques.* Analog Devices.

Data Sheets and Evaluation Boards

AD7366 Data Sheet.

AD7367 Data Sheet.

AD8021 Data Sheet.

OP177 Data Sheet.

AD7366/AD7367 Evaluation Board.

REVISION HISTORY

09/09—Rev. 0 to Rev. A

Updated Format.....Universal

10/08—Revision 0: Initial Version

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Devices Connected/Referenced	
AD8352	Ultralow Distortion Differential RF/IF Amplifier
AD9445	14-Bit, 105 MSPS/125 MSPS Analog-to-Digital Converter

Using the AD8352 as an Ultralow Distortion Differential RF/IF Front End for High Speed ADCs

CIRCUIT FUNCTION AND BENEFITS

These circuits provide both a single-ended and a differential configuration for driving high speed ADCs using the AD8352 ultralow distortion differential RF/IF amplifier. The AD8352 provides the gain, isolation, and distortion performance necessary for efficiently driving high linearity converters, such as the AD9445. This device also provides balanced outputs whether driven differentially or single-ended, thereby maintaining excellent second-order distortion levels.

CIRCUIT DESCRIPTION

Figure 1 and Figure 2 illustrate two front-end circuits for driving the AD9445 14-bit ADC at 105 MSPS. Figure 1 provides a differential input configuration, while Figure 2 provides a single-ended input configuration.

In the differential configuration shown in Figure 1, the input 49.9 Ω resistor provides a differential input impedance to the 50 Ω RF/IF source. When the driver is located less than approximately one eighth of the wavelength of the maximum input RF/IF frequency from the AD8352, impedance matching is not required, thereby eliminating the need for this termination resistor. The output 24 Ω series resistors provide isolation from the input capacitance of the ADC, and the optimum value is determined empirically. The 100 MHz FFT plots shown in Figure 3 and Figure 4 display the performance results for the differential configuration.

In the single-ended input configuration shown in Figure 2, the net input impedance at V_{IP} is R_N (200 Ω) plus the external 24.9 Ω balancing resistor, or ~225 Ω. This requires a 64.9 Ω parallel resistor to provide the input impedance match for a 50 Ω source. If input reflections are minimal, this impedance match is not required. The 200 Ω resistor (R_N) is required to balance the output voltages to minimize second-order distortion.

The single-ended configuration provides −3 dB bandwidths similar to input differential drive and shows little or no degradation in overall third-order harmonic performance. The single-ended, third-order distortion levels are similar to the

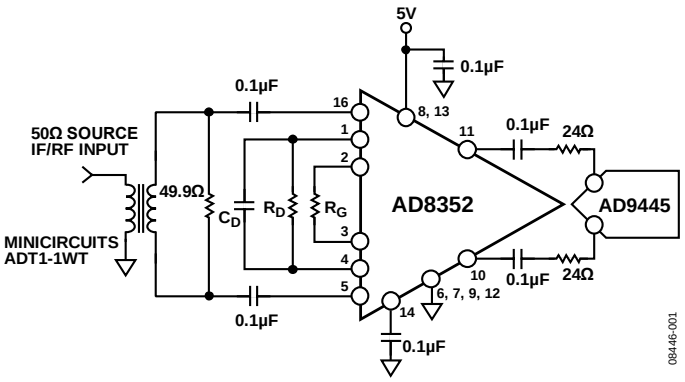

Figure 1. Differential Input to the AD8352 Driving the AD9445 14-Bit, 105 MSPS/125 MSPS ADC (Simplified Schematic, All Connections Not Shown)

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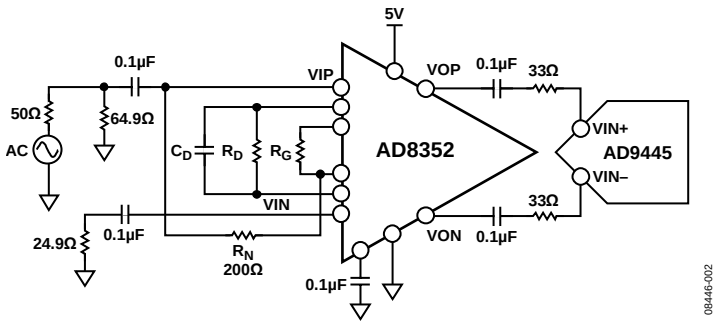

Figure 2. Single-Ended Input to the AD8352 Driving the AD9445 ADC (Simplified Schematic, All Connections Not Shown)

differential FFT plots in Figure 3 and Figure 4. The single-ended circuit avoids the use of a transformer or balun in front of the amplifier while still maintaining excellent distortion up to approximately 100 MHz. However, at frequencies above approximately 100 MHz, second-order distortion increases when the AD8352 is driven single-ended due to phase-related errors.

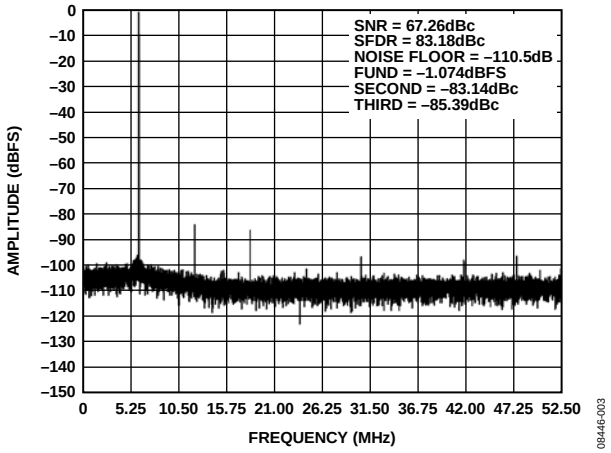

Figure 3. Single Tone Distortion, AD8352 Driving AD9445, Sampling Clock = 105 MSPS, Analog Input Frequency = 100 MHz, A_V = 10 dB. See Figure 1.

In both configurations, R_G is the gain setting resistor for the AD8352, with the R_D and C_D components providing distortion cancellation. The AD9445 differential input impedance is approximately 2 kΩ in parallel with 5 pF and requires a 2.0 V p-p differential signal (V_{REF} = 1 V) between V_{IN+} and V_{IN-} for a full-scale input signal.

The output of the amplifier is ac-coupled to allow for an optimum common-mode voltage at the ADC input. The common-mode voltage at the input of the AD9445 is set to 3.5 V by an internal network. Input ac-coupling can be required if the source also requires a common-mode voltage that is outside the optimum range of the AD8352. A V_{CM} common-mode pin is provided on the AD8352 that equally shifts both input and output common-mode levels. Increasing the gain of the AD8352 increases the system noise and, thus, decreases the SNR (3.5 dB at 100 MHz input for A_V = 10 dB) of the AD9445 when no filtering is used. However, it should be noted that amplifier gains from 3 dB to 18 dB, with proper selection of C_D and R_D, do not appreciably affect distortion levels. These circuits, when configured properly, can result in SFDR performance of better than 87 dBc at 70 MHz and 82 dBc at 180 MHz input. Single-ended drive, with appropriate C_D and R_D, gives similar results for SFDR and third-order intermodulation levels as shown in these figures.

Excellent layout, grounding, and decoupling techniques must be utilized in order to achieve the desired performance from the circuits discussed in this note. As a minimum, a 4-layer PCB should be used with one ground plane layer, one power plane layer, and two signal layers.

All IC power pins must be decoupled to the ground plane with low inductance multilayer ceramic capacitors (MLCC) of 0.01 µF to 0.1 µF (this is not shown in the diagrams for simplicity). Follow the recommendations on the individual data sheets for the ICs.

The product evaluation boards should be consulted for recommended layout and critical component placement. They can be accessed through the main product pages for the devices or their data sheets.

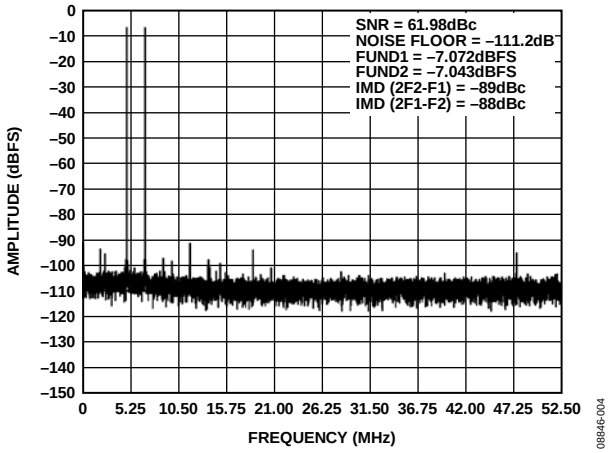

Figure 4. Two Tone Intermodulation Distortion, AD8352 Driving AD9445, Sampling Clock = 105 MSPS, Analog Input Frequency = 98 MHz and 101 MHz, A_V = 10 dB. See Figure 1.

COMMON VARIATIONS

Placing antialiasing filters between the ADC and the amplifier is a common approach for improving overall noise and broadband distortion performance for both band-pass and low-pass applications. For high frequency filtering, matching to the filter is required. The AD8352 maintains a 100 Ω output impedance well beyond most applications and is well-suited to drive most filter configurations with little or no degradation in distortion.

The AD8352 low distortion differential amplifier can be replaced by the high IP3, low noise figure AD8375 variable gain amplifier (VGA). The AD8375 is a digitally controlled, variable gain, wide bandwidth amplifier that provides precise gain control across a broad 24 dB gain range, with 1 dB resolution. The AD8376 is a dual version of the AD8375. (See Circuit Note CN-0002, *Using the AD8376 VGA to Drive Wide Bandwidth ADCs for High IF AC-Coupled Applications*.)

LEARN MORE

CN-0002 Circuit Note, *Using the AD8376 VGA to Drive Wide Bandwidth ADCs for High IF AC-Coupled Applications*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-073 Tutorial, *High Speed Variable Gain Amplifiers (VGAs)*. Analog Devices.

MT-075 Tutorial, *Differential Drivers for High Speed ADCs Overview*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Data Sheets

AD8352 Data Sheet.

AD8375 Data Sheet.

AD8376 Data Sheet.

AD9445 Data Sheet.

AD9445 Evaluation Board.

High Speed ADC Evaluation Kits and Evaluation Boards.

REVISION HISTORY

8/09—Rev. 0 to Rev. A

Updated Format ..... Universal

10/08—Revision 0: Initial Version

ANALOG DEVICES

Circuit Note
CN-0050

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Devices Connected/Referenced in this Circuit Note	
ADL5330	Variable Gain Amplifier (VGA)
AD8318	70 dB Logarithmic Detector/Controller

Stable, Closed-Loop Automatic Power Control for RF Applications

CIRCUIT FUNCTION AND BENEFITS

The circuit described in this document provides closed-loop, automatic power control using a VGA (ADL5330) and a log detector (AD8318). Due to the high temperature stability of the AD8318, this circuit provides stability over temperature because the AD8318 RF detector ensures the same level of temperature stability at the output of the ADL5330 VGA. The addition of the log amp detector converts the ADL5330 from an open-loop variable gain amplifier to a closed-loop output power control circuit. Because the AD8318, like the ADL5330, has a linear-in-dB transfer function, the P_{OUT} vs. setpoint transfer function also follows a linear-in-dB characteristic.

CIRCUIT DESCRIPTION

Although the ADL5330 variable gain amplifier provides accurate gain control, precise regulation of output power can be achieved with an automatic gain control (AGC) loop. Figure 1 shows the ADL5330 operating in an AGC loop. The addition of the AD8318 log amp allows the AGC to have improved temperature stability over a wide output power control range.

To operate the ADL5330 VGA in an AGC loop, a sample of the output RF must be fed back to the detector (typically using a directional coupler and additional attenuation). A setpoint voltage is applied by a DAC to the VSET input of the detector while VOUT is connected to the GAIN pin of the ADL5330. Based on the detector's defined linear-in-dB relationship between VOUT and the RF input signal, the detector adjusts the voltage on the GAIN pin (the detector's VOUT pin is an error amplifier output) until the level at the RF input corresponds to the applied setpoint voltage. GAIN settles to a value that results in the correct balance between the input signal level at the detector and the setpoint voltage.

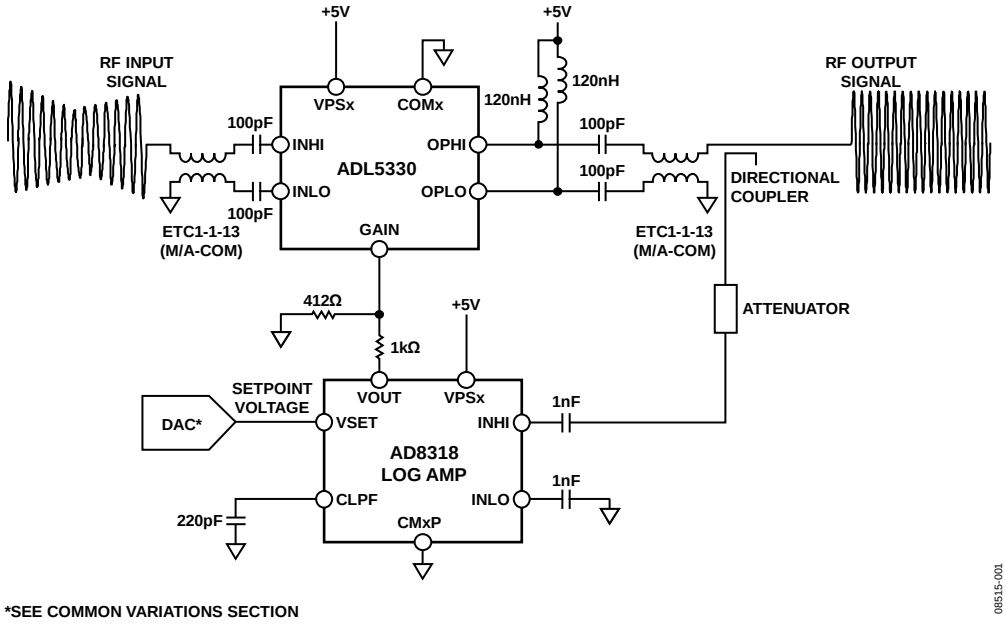

Figure 1. ADL5330 Operating in an Automatic Gain Control Loop in Combination with the AD8318 (Simplified Schematic: Decoupling and All Connections Not Shown)

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The basic connections for operating the ADL5330 in an AGC loop with the AD8318 are shown in Figure 1. The AD8318 is a 1 MHz to 8 GHz precision demodulating logarithmic amplifier. It offers a large detection range of 60 dB with ±0.5 dB temperature stability. The gain control pin of the ADL5330 is controlled by the output pin of the AD8318. This voltage, VOUT, has a range of 0 V to near VPSx. To avoid overdrive recovery issues, the AD8318 output voltage can be scaled down using a resistive divider to interface with the 0 V to 1.4 V gain control range of the ADL5330.

A coupler/attenuation of 23 dB is used to match the desired maximum output power from the VGA to the top end of the linear operating range of the AD8318 (at approximately −5 dBm at 900 MHz).

The detector's error amplifier uses CLPF, a ground-referenced capacitor pin, to integrate the error signal (in the form of a current). A capacitor must be connected to CLPF to set the loop bandwidth and to ensure loop stability.

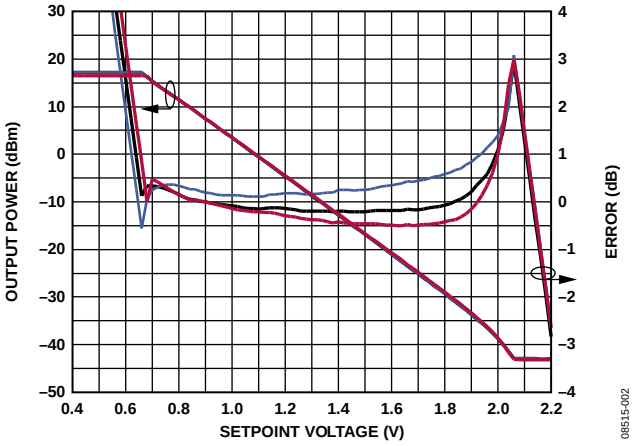

Figure 2. ADL5330 Output Power vs. AD8318 Setpoint Voltage, PIN = −1.5 dBm

Figure 2 shows the transfer function of the output power vs. the VSET voltage over temperature for a 900 MHz sine wave with an input power of −1.5 dBm. Note that the power control of the AD8318 has a negative sense. Decreasing VSET, which corresponds to demanding a higher signal from the ADL5330, tends to increase GAIN.

The AGC loop is capable of controlling signals just under the full 60 dB gain control range of the ADL5330. The performance over temperature is most accurate over the highest power range, where it is generally most critical. Across the top 40 dB range of output power, the linear conformance error is well within ±0.5 dB over temperature.

The broadband noise added by the logarithmic amplifier is negligible.

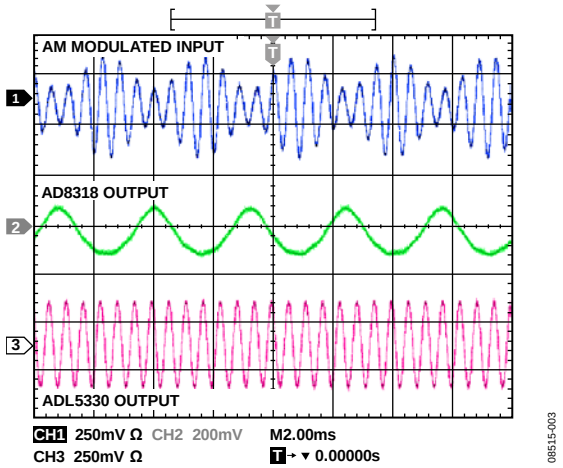

Figure 3. Oscilloscope Showing an AM Modulated Input Signal

For the AGC loop to remain in equilibrium, the AD8318 must track the envelope of the ADL5330 output signal and provide the necessary voltage levels to the ADL5330 gain control input. Figure 3 shows an oscilloscope screen shot of the AGC loop depicted in Figure 1. A 100 MHz sine wave with 50% AM modulation is applied to the ADL5330. The output signal from the ADL5330 is a constant envelope sine wave with amplitude corresponding to a setpoint voltage at the AD8318 of 1.5 V. Also shown is the gain control response of the AD8318 to the changing input envelope.

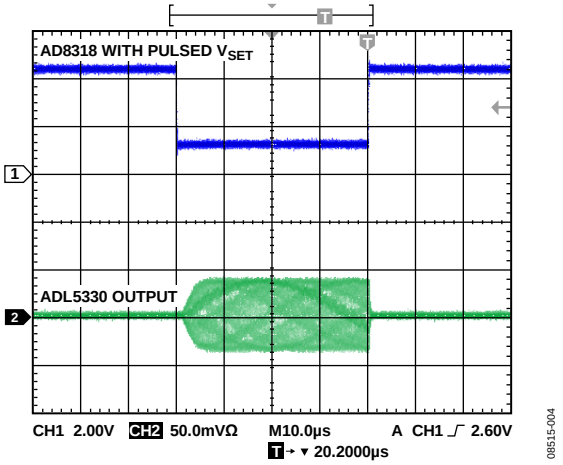

Figure 4. Oscilloscope Showing the ADL5330 Output

Figure 4 shows the response of the AGC RF output to a pulse on VSET. As VSET decreases to 1 V, the AGC loop responds with an RF burst. Response time and the amount of signal integration are controlled by the capacitance at the AD8318 CLPF pin—a function analogous to the feedback capacitor around an integrating amplifier. An increase in the capacitance results in slower response time.

The circuit must be constructed on a multilayer printed circuit board with a large area ground plane. Proper layout, grounding, and decoupling techniques must be used to achieve optimum performance (see the MT-031 Tutorial and the MT-101 Tutorial and the ADL5330 and ADL8318 evaluation board layouts).

On the underside of the ADL5330 and AD8318 chip scale packages, there is an exposed compressed paddle. This paddle is internally connected to the chip's ground. Solder the paddle to the low impedance ground plane on the printed circuit board to ensure specified electrical performance and to provide thermal relief. It is also recommended that the ground planes on all layers under the paddle be stitched together with vias to reduce thermal impedance.

COMMON VARIATIONS

This circuit can be used to implement a constant power out function (fixed setpoint with variable input power) or a variable power out function (variable setpoint with fixed or variable input power). If a lower output power control range is desired, the AD8318 log amp (60 dB power detection range) can be replaced with either the AD8317 (50 dB power detection range) or the AD8319 (45 dB power detection range). For a constant output power function, the lowest dynamic range detector (AD8319) is adequate because the loop always servos the detector input power to a constant level.

The ADL5330 VGA, which is optimized for transmit applications, can be replaced by the AD8368 VGA. The AD8368 is optimized for receive application low frequencies of up to 800 MHz and provides 34 dB of linear-in-dB voltage-controlled variable gain.

There are a number of DACs suitable for this application. All of the following DACs have internal references:

Single: AD5660/AD5640/AD5620 (16-bit/14-bit/12-bit),

Dual: AD5663R/AD5643R/AD5623R (16-bit/14-bit/12-bit)

Quad: AD5664R/AD5644R/AD5624R (16-bit/14-bit/12-bit)

LEARN MORE

Dana Whitlow, *Design and Operation of Automatic Gain Control Loops for Receivers in Modern Communications Systems*, Analog Devices Wireless Seminar, Chapter 7, 2006.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND,"* Analog Devices.

MT-073 Tutorial, *High Speed Variable Gain Amplifiers*, Analog Devices.

MT-077 Tutorial, *Log Amp Basics*, Analog Devices.

MT-078 Tutorial, *High Speed Log Amps*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets

ADL5330

AD8318

AD8317

AD8319

ADL5330 Evaluation Board

AD8318 Evaluation Board

REVISION HISTORY

9/10—Rev. A to Rev. B

Changes to Figure 1 1
Changes to Circuit Description Section 1
Changes to Common Variations Section 3

11/09—Rev. 0 to Rev. A

Updated Format ..... Universal
Changes to Circuit Note Title 1

10/08—Revision 0: Initial Release

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Devices Connected/Referenced	
ADA4937-1	Ultralow Distortion Differential ADC Driver
AD9246	14-Bit, 80 MSPS/105 MSPS/125 MSPS ADC

Driving the AD9233/AD9246/AD9254 ADCs in AC-Coupled Baseband Applications

CIRCUIT FUNCTION AND BENEFITS

The circuit described in this document and shown in Figure 1 uses the ADA4937-1 ADC driver to convert an ac-coupled, single-ended input signal to a differential signal suitable for driving the AD9246 14-bit, 125 MSPS analog-to-digital converter (ADC). The ADA4937-1 is a low noise, ultralow distortion, high speed differential amplifier with low dc offset and excellent dynamic performance. It is an ideal choice for driving high performance ADCs with resolutions up to 16 bits from dc to 100 MHz and is well suited for a wide variety of data acquisition and signal processing applications. Combined with power and cost savings over previously available ADCs, this circuit is suitable for applications in communications, instrumentation, and medical imaging. The ADA4937-2 is a dual version of the ADA4937-1 that can be used when driving a dual ADC.

CIRCUIT DESCRIPTION

The AD9246 is a monolithic, single 1.8 V supply, 14-bit, 80 MSPS/105 MSPS/125 MSPS ADC, featuring a high performance sample-and-hold amplifier (SHA) and on-chip voltage reference. The wide bandwidth, truly differential SHA allows a variety of user-selectable input ranges and offsets, including single-ended applications. The device can be applied in multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel input frequencies well beyond the Nyquist frequency of the ADC.

The AD9246 achieves its optimum performance when driven differentially. The ADA4937-1 not only provides the single-ended-to-differential conversion but also provides gain and level shifting. The output common voltage of the ADA4937-1 is set by connecting a resistive divider to the VOCM pin of the ADA4937-1. If the pin is left floating, the V_{OCM} voltage is approximately midsupply and is set by an internal divider.

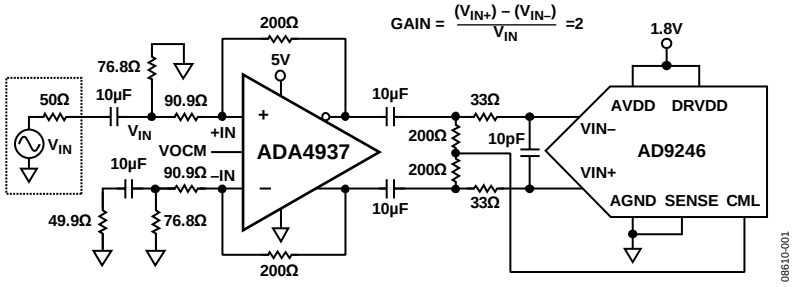

Figure 1. ADA4937-1 Driving the AD9246 14-Bit ADC
(Simplified Schematic: Decoupling and All Connections Not Shown)

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The ADA4937-1 is powered with a single 5 V supply and is configured for a gain-of-2 for a single-ended, input-to-differential output. The 76.8 Ω termination resistor, in parallel with the single-ended input impedance of 137Ω, provides a 50 Ω ac termination for the source. The additional 49.9Ω resistor, 10 µF capacitor, and 76.8 Ω resistor connected to the 90.9 Ω resistor on the inverting input balance the ac impedance driving the noninverting input. A detailed analysis of this configuration can be found in MT-076 Tutorial.

The signal generator has a symmetric, ground-referenced, bipolar output. The V_{OCM} pin of the ADA4937-1 is left unconnected; therefore, the internal divider sets the output common-mode voltage to midsupply. A portion of this is fed back to the summing nodes, biasing –IN and +IN at 1.14 V. For a common-mode voltage of 2.5 V, each ADA4937-1 output swings between 2.0 V and 3.0 V, providing a 2 V p-p differential output for a 1 V p-p single-ended input.

The output of the ADC driver is ac-coupled to a single-pole, low-pass noise filter. The low-pass filter reduces the noise bandwidth at the ADC input and provides a degree of isolation from the switched capacitor inputs of the ADC and the driver. In any configuration, the optimum value of the shunt capacitor, C, is dependent on the input frequency and source impedance and may need to be optimized. Table 1 displays recommended values for the RC network. However, these values are dependent on the input signal frequency and may require further optimization.

The input common-mode voltage to the ADC is set by the CML pin of the AD9246 and the pair of 200 Ω resistors. In other applications, the CML pin of the ADC and the V_{OCM} pin of the ADA4937-1 are used to set the input common-mode voltage to the ADC (see the Common Variations section). The ADA4937-1 is fabricated using the Analog Devices, Inc., proprietary silicon-germanium (SiGe), complementary bipolar process, enabling it to achieve very low levels of distortion with an input voltage noise of only 2.2 nV/ √Hz.

The circuit shown in Figure 1 was tested with a −1 dBFS signal at various input frequencies. Figure 2 shows a plot of the second and third harmonic distortion (HD2/HD3) vs. input frequency.

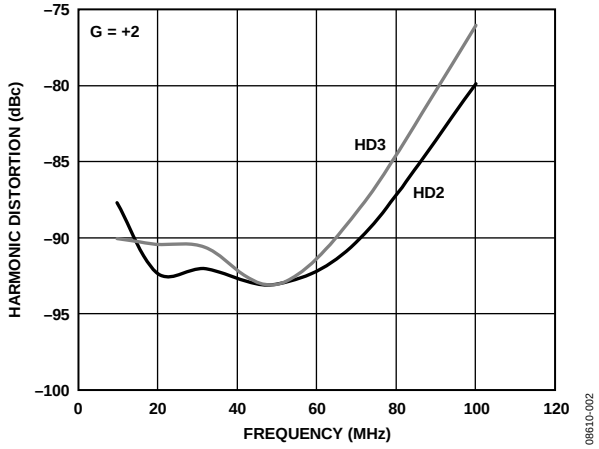

Figure 2. Second Harmonic Distortion (HD2) and Third Harmonic Distortion (HD3) for the ADA4937-1 Driving the AD9246 ADC

The circuit must be constructed on a multilayer PC board with a large area ground plane. Proper layout, grounding, and decoupling techniques must be used to achieve optimum performance (see MT-031 Tutorial, MT-101 Tutorial, and the AD9246 evaluation board layout).

It is required that the exposed pad on the underside of both the AD9246 and the ADA4937-1 (LFCSP packages) be connected to a large area ground plane to achieve the best electrical and thermal performance. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder filled or plugged.

COMMON VARIATIONS

The AD9246 (14-bit, 80 MSPS/105 MSPS/125 MSPS) ADC is pin compatible with both the AD9233 (12-bit, 80 MSPS/105 MSPS/125 MSPS) and the AD9254 (14-bit, 150 MSPS).

There are a few other amplifier configurations to consider when driving ADCs. They are differential ac-coupled input to differential output, dc-coupled single-ended input to ac-coupled differential output, dc-coupled single-ended input to differential output, and dc-coupled differential input to differential output.

In dc-coupled systems, the driver output common-mode voltage is set via the V_{OCM} pin of the ADA4937-1. The adjustable level of the output common-mode voltage allows the ADA4937-1 output to match the input common-mode voltage of the ADC. The internal common-mode feedback loop of the ADA4937-1 also provides exceptional output balance and suppression of even-order harmonic distortion products. Often in these applications, the ADC CML pin is connected directly to the V_{OCM} pin of the driver to ensure that optimal ADC input common-mode voltage is achieved. In other applications, the V_{OCM} pin can be driven from a low impedance source such as an op amp. It can also be left floating but bypassed with a capacitor; in this case the V_{OCM} voltage is set at the midpoint of the voltage applied to the two supply pins.

Table 1. RC Network Recommended Values

Input Frequency Range (MHz)	R Series (Ω)	C Differential (pF)
0 to 70	33	15
70 to 200	33	5
200 to 300	15	5
>300	15	Open (no capacitor)

LEARN MORE

Rob Reeder and Jim Caserta, *Wideband A/D Converter Front-End Design Considerations II: Amplifier- or Transformer Drive for the ADC?* Ask The Application Engineer—36, Analog Dialogue 41-02, February 2007.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND,"* Analog Devices.

MT-074 Tutorial, *Differential Drivers for Precision ADCs*, Analog Devices.

MT-075 Tutorial, *Differential Drivers for High Speed ADCs Overview*, Analog Devices.

MT-076 Tutorial, *Differential Driver Analysis*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

John Ardizonni and Jonathan Pearson, "Rules of the Road" for High-Speed Differential ADC Drivers, *Analog Dialogue*, Volume 43, May 2009, Analog Devices.

ADIsimDiffAmp (Differential Amplifier Tool), Analog Devices.

Data Sheets and Evaluation Boards

ADA4937-1 Data Sheet.

AD9246 Data Sheet

AD9246 Evaluation Board.

REVISION HISTORY

11/09—Rev. 0 to Rev. A

Updated Format ..... Universal

2/09—Revision 0: Initial Release

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Devices Connected/Referenced	
AD5450/AD5451/ AD5452/AD5453	8-/10-/12-/14-Bit Multiplying DACs
OP177	Ultra-Precision Operational Amplifier
ADR01	Low Noise Precision 10 V Reference

Unipolar, Precision DC, Digital-to-Analog Conversion Using the AD5450/AD5451/AD5452/AD5453 8-/10-/12-/14-Bit DACs

CIRCUIT FUNCTION AND BENEFITS

The circuit described in this document is a high performance, unipolar, precision DAC configuration that employs the AD5450/AD5451/AD5452/AD5453 family of precision multiplying DACs, the OP177 low noise, high precision operational amplifier (op amp), and the ADR01 precision 10 V reference. Because the op amp dictates the overall circuit dc performance in terms of precision, the OP177, a high precision, low noise op amp, is well matched for performance-driven applications. This circuit also uses the ADR01, which is a high accuracy, high stability, 10 V precision voltage reference. Because voltage reference temperature coefficient and long-term drift are primary considerations for applications requiring high precision conversion, this device is also an ideal candidate.

CIRCUIT DESCRIPTION

The circuit uses the AD5450/AD5451/AD5452/AD5453 CMOS, current-output DACs, which provide 8-, 10-, 12- and 14-bit operation, respectively. Because this is a current-output DAC, an op amp is required for current-to-voltage (I-V) conversion at the output of the DAC. Because an op amp bias current and offset voltage are both important selection criteria for precision current output DACs, this circuit employs the OP177 op amp, which has ultralow offset voltage (25 µV) and bias current (2 nA). The OP177 and the AD5450/AD5451/AD5452/AD5453 can be easily configured to provide a two-quadrant multiplying operation or a unipolar output voltage swing, as shown in Figure 1.

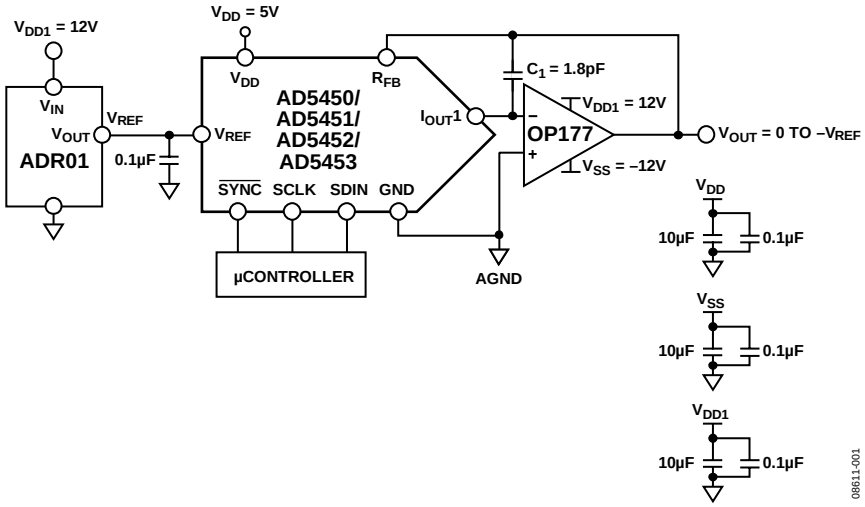

Figure 1. Unipolar Precision DC Configuration
(Simplified Schematic: Decoupling and All Connections Not Shown)

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The AD5450/AD5451/AD5452/AD5453are designed on a 5 V CMOS process and operate from a V_{DD} power supply of 2.5 V to 5.5 V. The DACs accept V_{REF} input ranges up to 10 V, as shown with the ADR01 reference in Figure 1. The ADR01 requires a supply voltage (V_{DD1}) of 12 V minimum and can be driven from the same supply voltage that powers the output amplifier.

When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -V_{REF} \times (D/2^N)$$

where *D* is the digital word loaded to the DAC, and *N* is the number of bits (D = 0 to 255 (8-bit AD5450); D = 0 to 1023 (10-bit AD5451); D = 0 to 4095 (12-bit AD5452); D = 0 to 16,383 (14-bit AD5453)).

The input offset voltage of an op amp is multiplied by the variable noise gain (due to the code-dependent output resistance of the DAC) of the circuit. A change in this noise gain between two adjacent digital codes produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, may cause the DAC to be nonmonotonic. In general, the input offset voltage should be a fraction of an LSB to ensure monotonic behavior when stepping through codes.

Relative accuracy or endpoint nonlinearity is one of the most widely used techniques in determining the accuracy performance of a DAC circuit. This is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full-scale error and is normally expressed in LSBs. Figure 2 shows the performance of the circuit shown in Figure 1 using the AD5453 14-bit DAC and an OP177 amplifier.

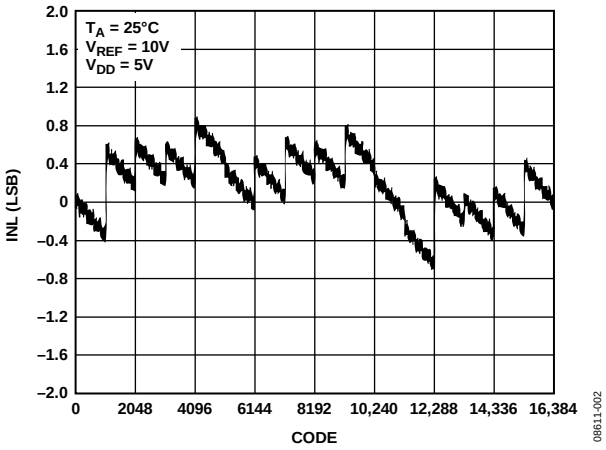

Figure 2. AD5453 14-Bit DAC Relative Accuracy Plot.

Excellent grounding, layout, and decoupling techniques must be used for proper operation of the circuit. All power supply pins should be decoupled directly at the pin with a low inductance (low ESL) 0.1 µF ceramic capacitor. The connection to ground should be directly to a large area ground plane. Additional decoupling using a 1 µF to 10 µF electrolytic capacitor is recommended on each power supply where it enters the PC board. The decoupling capacitors are not shown in Figure 1 for simplicity.

To optimize high frequency performance, the I-V amplifier should be located as close to the DAC as possible. The AD5450/AD5451/AD5452/AD5453 data sheets show the schematics and layouts used for the evaluation boards.

COMMON VARIATIONS

The OP1177 and AD8065 are other excellent op amp candidates for the I-V conversion circuit. They also provide a low offset voltage and ultralow bias current.

The 10.0 V output ADR01 can be replaced by either the ADR02 or ADR03, which are low noise references available from the same reference family as the ADR01 and provide 5.0 V and 2.5 V outputs, respectively. The ADR445 and ADR441 ultralow noise references are also suitable substitutes that provide 5.0 V and 2.5 V, respectively. Note that the size of the reference input voltage is restricted by the rail-to-rail voltage of the operational amplifier selected.

LEARN MORE

Kester, Walt. *The Data Conversion Handbook*. Chapters 3, 7. Analog Devices, 2005.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-033 Tutorial, *Voltage Feedback Op Amp Gain and Bandwidth*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

ADIsimPower Design Tool. Analog Devices.

Voltage Reference Wizard Design Tool. Analog Devices.

Data Sheets and Evaluation Boards

AD5450/AD5451/AD5452/AD5453 Data Sheets and Evaluation Boards.

OP177 Data Sheet.

AD8065 Data Sheet.

OP1177 Data Sheet.

ADR01 Data Sheet.

ADR02 Data Sheet.

ADR03 Data Sheet.

ADR441 Data Sheet.

ADR445 Data Sheet.

REVISION HISTORY

11/09—Rev. 0 to Rev. A

Updated Format ..... Universal

1/09—Revision 0: Initial Release

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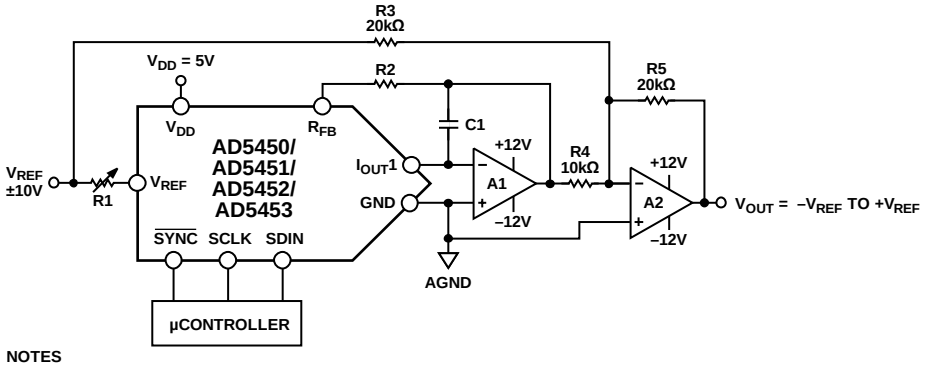
Devices Connected/Referenced	
AD5450/AD5451/ AD5452/AD5453	8-/10-/12-/14-Bit Multiplying DACs
AD8066	Dual High Performance *FastFET*™ Amplifier
ADR01	Low Noise, Precision 10 V Reference

Precision, Bipolar Configuration for the AD5450/AD5451/AD5452/AD5453 8-/10-/12-/14-Bit Multiplying DACs

CIRCUIT FUNCTION AND BENEFITS

This circuit is a bipolar, precision DAC configuration that employs an AD5450, AD5451, AD5452, orAD5453 precision multiplying DAC and the AD8066 low noise op amp. The DAC is the core-programmable element, and the amplifier selection dictates the performance in terms of precision or speed. For an accurate, high precision, low noise application, a dual operational amplifier (op amp) such as the AD8066 can be used to provide the current-to-voltage conversion and the signal conditioning. A low noise reference such as the ADR01 is required to drive the V_{REF} input, and the optimum output noise performance is obtained by using a low noise, low bandwidth output amplifier. The main advantages of this circuit are simplicity, constant reference input impedance, and the ability of V_{REF} to exceed the DAC V_{DD} supply voltage.



NOTES
1. R1 AND R2 ARE USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. ADJUST R1 FOR V_{OUT} = 0V WITH CODE 10000000 LOADED TO DAC.
2. MATCHING AND TRACKING ARE ESSENTIAL FOR RESISTOR PAIRS R3 AND R4.
3. C1 PHASE COMPENSATION (1pF TO 5pF) MAY BE REQUIRED IF A1/A2 IS A HIGH SPEED AMPLIFIER.

Figure 1. Bipolar Precision DC Conversion (Simplified Schematic: Decoupling and All Connections Not Shown)

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CIRCUIT DESCRIPTION

In many applications, it may be necessary to generate a full four-quadrant multiplying operation or a bipolar output voltage swing as shown in Figure 1. This can be easily accomplished by using a dual amplifier denoted by A1 and A2 and some external resistors. In this circuit, the A1 amplifier performs the current-to-voltage conversion, and the second amplifier, A2, provides a gain of 2. Biasing the external amplifier with an offset from the reference voltage results in a full four-quadrant multiplying operation. In dc applications, a suitable reference to drive the reference input is the ADR01. This is a high accuracy, high stability, 10 V precision voltage reference. Because voltage reference temperature coefficient and long-term drift are primary considerations for applications requiring high precision conversion, this device is an ideal candidate.

The AD5450/AD5451/AD5452/AD5453 DACs are designed on a 5 V CMOS process and operate from a V_{DD} power supply of 2.5 V to 5.5 V. They accept V_{REF} input ranges of up to 10 V as shown in Figure 1, and the power supply for the output amplifiers must be a bipolar supply with enough headroom to accommodate the analog output range, V_{OUT}. The transfer function of this circuit shows that both negative and positive output voltages are created as the input code, D, is incremented from Code 0 ($V_{OUT} = -V_{REF}$) to midscale ($V_{OUT} = 0$ V) to full-scale ($V_{OUT} = +V_{REF}$). V_{OUT} is represented by the following equation:

$$V_{OUT} = V_{REF} \times (D/2^{N-1}) - V_{REF.}$$

where:
N is the resolution of the DAC .
D is the digital word loaded to the DAC ,and *D* = 0 to 255 (8-bit AD5450), *D* = 0 to 1023 (10-bit AD5451), *D* = 0 to 4095 (12-bit AD5452), or *D* = 0 to 16,383 (14-bit AD5453).

An op amp is used in the current-to-voltage (I-V) stage of this circuit. The supply voltage of the op amp limits the reference voltage that can be used with the DAC. An op-amp's bias current and offset voltage are both important selection criteria for precision current output DACs. Therefore, this circuit employs the AD8066 op amp, which has ultralow offset voltage (0.4 mV typical) and bias current (2 pA typical).

The input offset voltage of an op amp is multiplied by the variable noise gain (due to the code-dependent output resistance of the DAC) of the circuit. A change in this noise gain between two adjacent codes produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, can cause the DAC to be nonmonotonic.

In general, the input offset voltage should be a fraction of an LSB to ensure monotonic behavior when stepping through codes. A compensation capacitor, C1, is used to prevent ringing or instability in the closed loop. Typical values in the 1 pF to 5 pF range can be used.

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

These DACs should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESL), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

Low ESR, 1 µF to 10 µF tantalum capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple. To optimize high frequency performance, the I-V amplifier should be located as close to the DAC as possible.

COMMON VARIATIONS

The OP2177 is another excellent dual op-amp candidate for the I-V conversion circuit. It also provides a low offset voltage (15 µV typical) and ultralow bias current (0.5 nA typical). The ADR02 and ADR03 with 5.0 V and 2.5 V output, respectively, are other low noise references available from the same reference family as the ADR01. Other low noise references that are suitable are the ADR441 and ADR445. The size of the reference input voltage is restricted by the rail-to-rail output voltage of the operational amplifier selected.

LEARN MORE

Kester, Walt. *The Data Conversion Handbook*. Chapter 3, 7. Analog Devices. 2005.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-033 Tutorial, *Voltage Feedback Op Amp Gain and Bandwidth*. Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

ADIsimPower Design Tool. Analog Devices.

Voltage Reference Wizard Design Tool, Analog Devices

Data Sheets

AD5450/AD5451/AD5452/AD5453 Data Sheet

AD8066 Data Sheet

OP2177 Data Sheet

ADR01 Data Sheet

ADR02 Data Sheet

ADR03 Data Sheet

ADR441 Data Sheet

ADR445 Data Sheet

REVISION HISTORY

1/10—Rev. 0 to Rev. A

Updated Format ..... Universal
Changes to Circuit Description..... 2

10/09—Revision 0: Initial Version

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Devices Connected/Referenced	
AD5450/AD5451/ AD5452/AD5453	8-/10-/12-/14-Bit Multiplying DAC
AD8065	High Performance *FastFET*™ Amplifier

Programmable Gain Element Using the AD5450/AD5451/AD5452/AD5453 Current Output DAC Family

CIRCUIT FUNCTION AND BENEFITS

In applications where the DAC output voltage range is required to be larger than the input voltage, a programmable gain circuit can be used. This circuit provides a programmable gain function using a multiplying DAC, the AD5450/AD5451/AD5452/AD5453, and a fast, low offset operational amplifier, the AD8065. The maximum gain value and the temperature coefficient are set by external resistors, and the resolution of the programmable gain is set by the resolution of the DAC.

CIRCUIT DESCRIPTION

The circuit shown in Figure 1 is the recommended method of increasing the gain of the circuit. R1, R2, and R3 should all have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits where gains of greater than 1 are required.

$$V_{OUT} = -Gain \times V_{IN} \times \frac{D}{2^N} \quad (1)$$

where D is the digital word loaded to the DAC. D = 0 to 255 (8-bit AD5450), D = 0 to 1023 (10-bit AD5451), D = 0 to 4095 (12-bit AD5452), D = 0 to 16383 (14-bit AD5453); N is the number of bits.

The key benefit of this circuit is its ability to overcome gain TC errors using resistor matching. The TC of the external resistors needs to match each other but do not need to match that of the DAC internal ladder resistance.

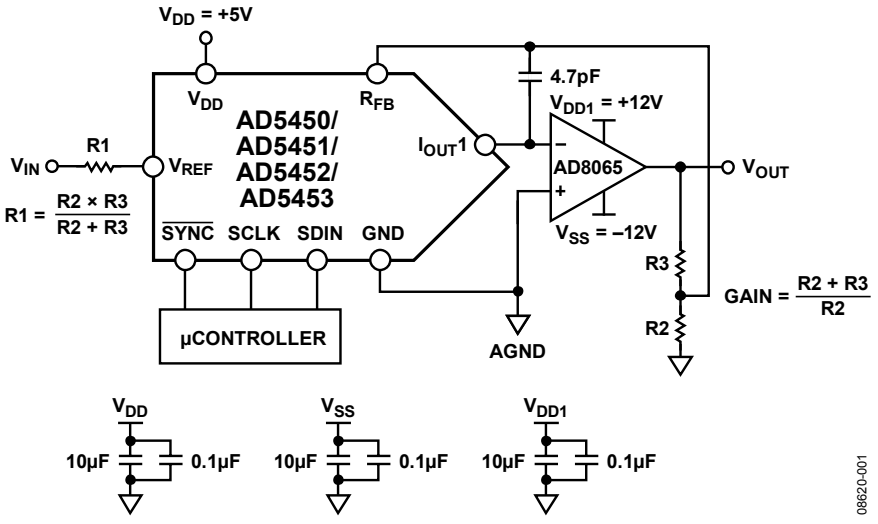

Figure 1. Programmable Gain Circuit Using a Current Output DAC (Simplified Schematic: Decoupling and All Connections Not Shown)

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Resistor R1 is required because R1 plus the input impedance of the DAC must equal the total feedback resistance which is RFB plus R2||R3. The input impedance of the DAC is RFB, so

$$R1 + RFB = RFB + R2||R3 \quad (2)$$

$$R1 = R2||R3 \quad (3)$$

The values of R1 and R2 must be chosen such that the output voltage does not exceed the output range of the operational amplifier for the given supply voltage. Also note that the bias current of the operational amplifier is multiplied by the total feedback resistance (RFB + R2||R3) to give an associated offset. Thus, the values of R1 and R2 cannot be too large or they will have a significant effect on the overall offset voltage.

The AD5450/AD5451/AD5452/AD5453 products are designed on a 5 V CMOS process and operate from a $V_{DD}1$ power supply of 2.5 V to 5.5 V. The output amplifier is driven from a dual power supply voltage (V_{DD}/V_{SS}), which needs to be large enough to accommodate the analog output range of the circuit. Generally, ±12 V supplies are sufficient. The 4.7 pF capacitor is used to prevent ringing or instability in the closed-loop application.

The input offset voltage of an op amp is multiplied by the variable noise gain (due to the code-dependent output resistance of the DAC) of the circuit. A change in this noise gain between two adjacent digital codes produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and produces a differential linearity error, which if large enough, could cause the DAC to be non-monotonic. The AD8065 benefits from both a low input offset voltage and low bias currents to overcome this issue.

COMMON VARIATIONS

The OP1177 is another excellent op amp candidate for the I-V conversion circuit. It also provides low offset voltage and ultralow bias current. For the selection of the reference, the input voltage is restricted by the rail-to-rail voltage of the operational amplifier selected and also the gain set up by the resistors R2 and R3.

LEARN MORE

ADIsimPower Design Tool. Analog Devices.

Kester, Walt. The Data Conversion Handbook. Chapter 3, 7. Analog Devices. 2005.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND."* Analog Devices.

MT-033 Tutorial, *Voltage Feedback Op Amp Gain and Bandwidth*. Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Voltage Reference Wizard Design Tool. Analog Devices.

Data Sheets

AD5450 Data Sheet

AD5451 Data Sheet

AD5452 Data Sheet

AD5453 Data Sheet

AD8065 Data Sheet

OP1177 Data Sheet

REVISION HISTORY

11/09—Rev. 0 to Rev. A

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Devices Connected/Referenced	
AD5765	Complete Quad, 16-Bit, High Accuracy DAC
ADR420	Precision 4.096 V Voltage Reference

High Accuracy, Bipolar Voltage Output Digital-to-Analog Conversion Using the AD5765 DAC

CIRCUIT FUNCTION AND BENEFITS

This circuit provides high accuracy, bipolar data conversion using the AD5765, a quad, 16-bit, serial input, bipolar voltage output DAC. This circuit utilizes the ADR420 precision reference to achieve optimal DAC performance over a full operating temperature range. The only external components needed for this precision 16-bit DAC are a reference voltage source, decoupling capacitors on the supply pins and reference inputs, and an optional short-circuit current-setting resistor. This implementation, therefore, leads to savings in cost and reduced board space. The circuit is well suited for both closed-loop servo control and open-loop control applications.

CIRCUIT DESCRIPTION

The AD5765 is a high performance digital-to-analog converter that offers guaranteed monotonicity, integral nonlinearity (INL) of ±1 LSB (C-grade device), low noise, and a 10 µs settling time. Performance is guaranteed over the following supply voltage ranges: The AVDD supply range is from +4.75 V to +5.25 V, and the AVSS supply range is from −4.75 V to −5.25 V. The nominal full-scale output voltage range is ±4.096 V.

A precision voltage reference must be used in order for the DAC to achieve the optimum performance over its full operating temperature range. The AD5765 incorporates reference buffers, which eliminate the need for both a positive and negative external reference and associated buffers. This leads to further savings in both cost and board space. Because the voltages applied to the reference inputs (REFAB, REFCD) are used to generate the buffered positive and negative internal references for the DAC cores, any error in the external voltage reference is reflected in the outputs of the device.

There are four possible sources of error to consider when choosing a voltage reference for high accuracy applications: initial accuracy, temperature coefficient of the output voltage, long term drift, and output voltage noise. Table 1 lists other

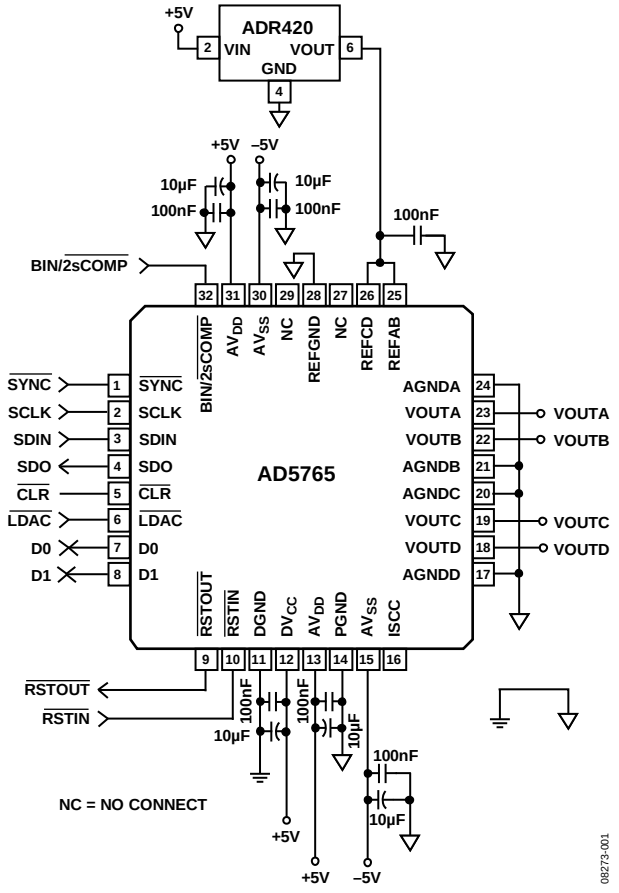

Figure 1. High Accuracy, Bipolar Configuration of the AD5765 DAC Using a Precision Reference

2.048 V precision reference candidates from Analog Devices, Inc., and their respective attributes.

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which the AD5765

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Table 1. Precision 2.048 V References

Part Number	Initial Accuracy Max (mV)	Long-Term Drift Typ (ppm)	Temp Drift Max (ppm/°C)	0.1 Hz to 10 Hz Noise Typ (μV p-p)
ADR430	±1	40	3	3.5
ADR420	±1	50	3	1.75
ADR390	±4	50	9	5

is mounted must be designed so that the analog and digital sections are physically separated and confined to certain areas of the board. If the AD5765 is in a system where multiple devices require an AGND-to-DGND connection, the connection is to be made at one point only. The star ground point is established as close as possible to the device. The AD5765 must have ample supply bypassing of 10 μF in parallel with 0.1 μF on each supply, located as close to the package as possible, ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESL), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply traces of the AD5765 must be as wide as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, must be shielded with digital ground to avoid radiating noise to other parts of the board and must never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (not required on a multilayer board, which has a separate ground plane; however, it is helpful to separate the lines). It is essential to minimize noise on the reference inputs because it couples through to the DAC output. Avoid crossover of digital and analog signals. Traces on opposite sides of the board must run at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is recommended but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the solder side. Best layout and performance are achieved with at least a 4-layer multilayer board, where there are a ground plane layer, a power supply layer, and two signal layers.

LEARN MORE

Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. Chapters 3 and 7.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Voltage Reference Wizard Design Tool.

Data Sheets and Evaluation Boards

AD5765 Data Sheet.

AD5765 Evaluation Board.

ADR420 Data Sheet.

REVISION HISTORY

6/09—Revision 0: Initial Version

ANALOG DEVICES

Circuit Note
CN-0079

Circuits from the Lab

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Devices Connected/Referenced	
AD5542	16-Bit Serial Input, Voltage Output DAC
ADR421	Precision 2.5 V Voltage Reference
AD8628	Auto-Zero Operational Amplifier

High Precision Digital-to-Analog Conversion Using the 16-Bit AD5542/AD5541 Voltage Output DAC, ADR421 Reference, and AD8628 Auto-Zero Op Amp

CIRCUIT FUNCTION AND BENEFITS

This circuit provides precision data conversion using the AD5542 voltage output DAC together with the ADR421BRZ voltage reference and the AD8628 auto-zero op amp as the reference buffer. The AD8628 reference buffer provide benefits previously found only in expensive auto-zeroing or chopper-stabilized amplifiers. Using Analog Devices, Inc., circuit topology, these *zero-drift* amplifiers combine low cost with high accuracy and low noise. No external capacitor is required, and the digital switching noise associated with most chopper-stabilized amplifiers is greatly reduced, thereby making this the optimum choice for reference buffering.

This circuit provides precision, low power, voltage output, digital-to-analog conversion. The AD5542 can be operated in either the buffered or unbuffered mode. The application and its requirements on settling time, input impedance, noise, etc., determine which mode of operation is best. The selection of the output buffer amplifier can be tailored to suit either dc precision or fast settling time. Where the DAC is required to drive a load less than 60 kΩ, an output buffer will be required. The output impedance of the DAC is constant and code independent, but to minimize gain errors the input impedance of the output amplifier should be as high as possible. The output amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The output amplifier adds another time constant to the system, thereby increasing the settling time of the final output.

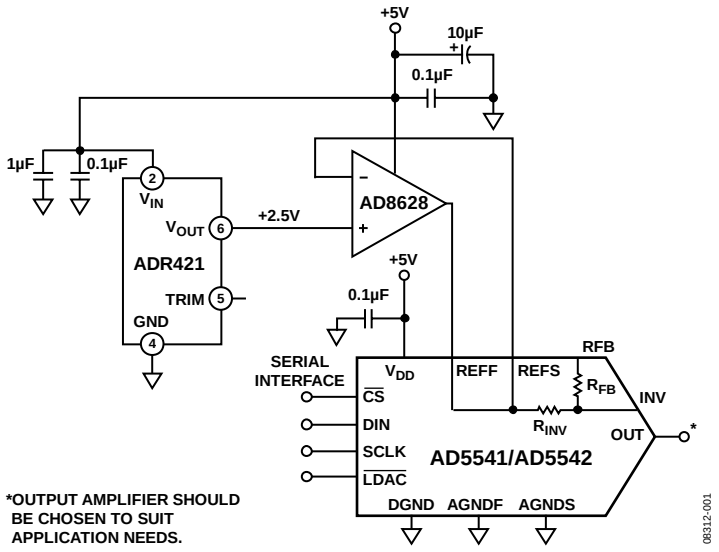

Figure 1. Precision DAC Configuration (Simplified Schematic)

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A higher 3 dB amplifier bandwidth results in a faster effective settling time of the combined DAC and amplifier. All devices in the circuit can be powered from a single +5 V supply. The input voltage range of the ADR421 reference is 4.5 V to 18 V.

CIRCUIT DESCRIPTION

This circuit utilizes the AD5542 voltage output DAC, providing 16-bit, fully accurate performance. The DAC architecture of the AD5541/AD5542 is a segmented R-2R voltage mode DAC. With this type of configuration the output impedance is independent of digital code, while the input impedance seen by the reference is heavily code dependent. For this reason, the reference buffer choice is very important to account for the code-dependent reference current, which may lead to linearity errors if the DAC reference is not adequately buffered. The op amp offset voltage, offset error temperature coefficient, and noise are important criteria when selecting a reference buffer with precision voltage output DACs. Offset errors in the reference circuit cause gain errors on the DAC output. This circuit employs the AD8628 zero-drift, single-supply, rail-to-rail, input/output operational amplifier. With an offset voltage of 1 μV, drift of less than 0.005 μV/°C, and noise of 0.5 μV p-p (0.1 Hz to 10 Hz), the AD8628 is suited for applications where error sources need to be minimized. The output voltage is dependent on the reference voltage, as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where D is the decimal data-word loaded to the DAC register and N is the resolution of the DAC.

For a reference of 2.5 V, the equation is simplified to the following:

$$V_{OUT} = \frac{2.5 \times D}{65{,}536}$$

This gives a V_{OUT} of 1.25 V for the midscale code and 2.5 V for the full-scale code.

The LSB size is 2.5 V/65,536, or 38.1 μV.

There is a common misconception that auto-zero amplifiers are not to be trusted because of intermodulation terms and unwanted harmonics filtering through to the output due to the internal switching action. Previous auto-zero amplifiers used either auto-zeroing or chopper stabilization techniques. Traditional auto-zeroing results in low noise energy at the auto-zeroing frequency at the expense of higher low frequency noise, due to aliasing of wideband noise into the auto-zeroed frequency band. Chopping results in less low frequency noise at the expense of larger noise energy at the chopping frequency. The AD8628 family uses both auto-zeroing and chopping in a patented "ping-pong" arrangement to obtain lower low frequency noise together with lower energy at the chopping and auto-zeroing frequencies, thereby maximizing the signal-to-noise ratio for the majority of applications without the need for additional filtering. The relatively high internal chopping frequency of 15 kHz simplifies filter requirements for a wide, useful, noise-free bandwidth in instrumentation and process control applications.

Measured results show that high accuracy, low noise performance with minimum high frequency intermodulation distortions transferred to the output is achievable using the AD8628 as a reference buffer in a high accuracy, high performance system.

Integral nonlinearity (INL) error is the deviation in LSBs of the actual DAC transfer function from an idealized transfer function. DNL error is the difference between an actual step size and the ideal value of 1 LSB. The circuit in Figure 1 provides 16-bit resolution with ±1 LSB INL error and ±1 LSB DNL error. Figure 2 and Figure 3 show the INL and DNL performance of the circuit.

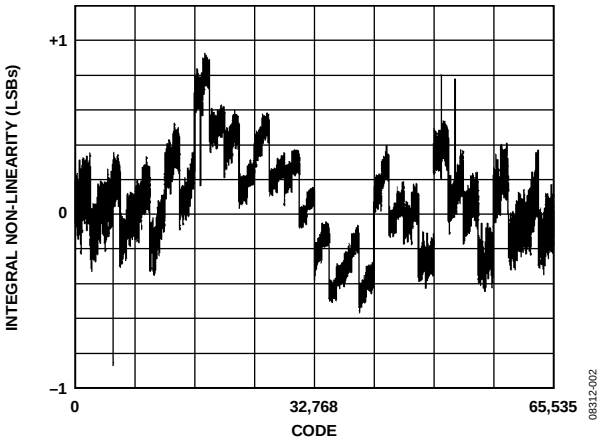

Figure 2. Integral Nonlinearity Error vs. Input Code

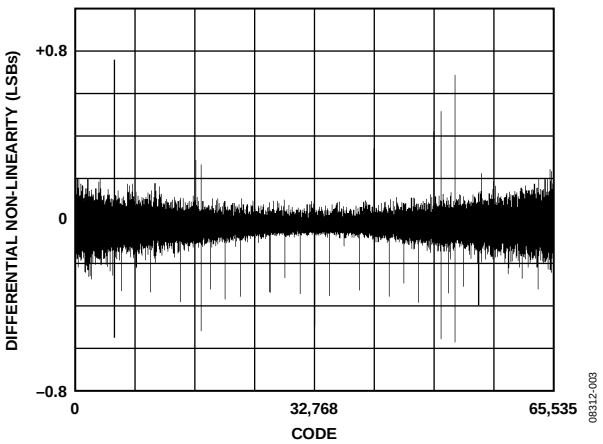

Figure 3. Differential Nonlinearity Error vs. Input Code

The offset error and gain error were measured to be 10 µV and 170 µV, respectively. The gain error of ±5 LSBs and the zero-code error of ±1 LSB are within the specified 38 µV (with a 2.5 V reference) at ambient temperature.

Figure 4 shows a 0.1 Hz to 10 Hz noise plot for the circuit.The output of the DAC, V_{OUT}, was connected to the input of a 0.1 Hz to 10 Hz bandwidth filter followed by an amplifier with a gain of 10,000. The voltage noise is captured on a scope. A very low peak-to-peak voltage of 57 mV is observed (5.7 µV with respect to the DAC output).

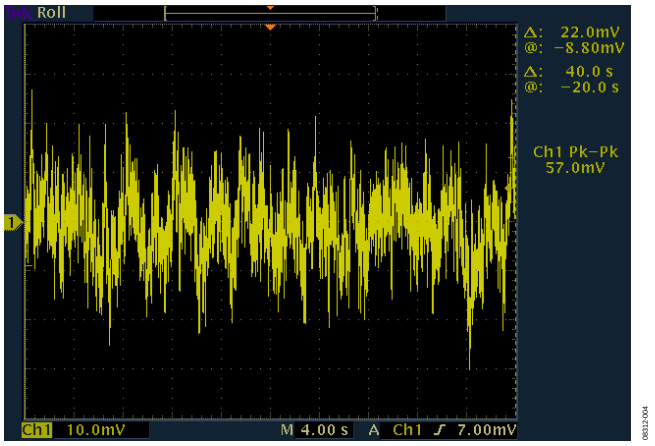

Figure 4. A 0.1 Hz to 10 Hz Output Noise Plot; Full-Scale Code Loaded into DAC (1/f Noise = 57 mV/10,000 = 5.7 µV)

Figure 5 shows the DAC output using the spectrum analyzer sweeping from 100 Hz to 100 kHz. No significant IMD terms were observed, thus showing that auto-zero amplifiers such as the AD8628 used as reference buffers are excellent choices.

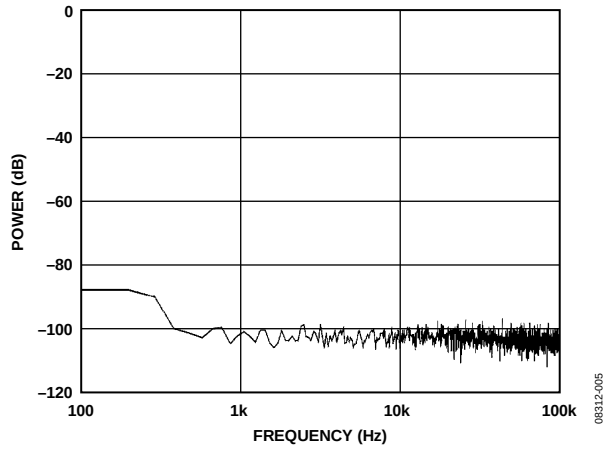

Figure 5. DAC Output Spectral Density Plot (dB Referenced to Full Scale)

In any circuit where accuracy is important, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board (PCB) containing the circuit should have separate analog and digital sections. If the circuit is used in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5542. The power supply to the AD5542 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be as physically close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor have low effective series resistance (ESR) and low effective series inductance (ESL), as is typical of common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching. The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground.

The circuit must be constructed on a multilayer PC board with a large area ground plane. Proper layout, grounding, and decoupling techniques must be used to achieve optimum performance (see Tutorial MT-031, *Grounding Data Converters and Solving the Mystery of AGND and DGND* and Tutorial MT-101, *Decoupling Techniques*).

COMMON VARIATIONS

The AD8538 is another excellent auto-zero op amp candidate to be used for buffering the reference in this circuit. It provides a low offset voltage and ultralow bias current. The 2.5 V output ADR421 can be replaced by either the ADR423 or the ADR424, which are low noise references available from the same reference family as the ADR421 and provide 3 V and 4.096 V, respectively. The ADR441 and the ADR431 ultralow noise references are suitable substitutes that provide 2.5 V, also. Note that the size of the reference input voltage is restricted by the rail-to-rail output voltage capability of the operational amplifier selected.

There is no output buffer used in this circuit because output buffer performance can be optimized for speed or dc precision, depending on the system bandwidth and application need. The AD5661 would be an excellent choice for an output buffer. This is a single-supply, 5 V to 16 V amplifier that uses Analog Devices' patented DigiTrim™ technique to achieve low offset voltage. It features low input bias current and wide signal bandwidth. The AD8605 or the AD8655 would also be excellent options.

LEARN MORE

Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. Chapters 3 and 7.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-016 Tutorial, *Basic DAC Architectures III: Segmented DACs*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*, Analog Devices.

MT-055 Tutorial, *Chopper Stabilized (Auto-Zero) Precision Op Amps*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Voltage Reference Wizard Design Tool.

Data Sheets

AD5541 Data Sheet.

AD5542 Data Sheet.

AD8628 Data Sheet.

ADR421 Data Sheet.

REVISION HISTORY

8/09—Revision 0: Initial Version

Circuits from the Lab™ Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0102.

Devices Connected/Referenced	
AD7190	4.8 kHz, Ultralow Noise, 24-Bit, Σ-Δ ADC with PGA
ADP3303	5 V Low Dropout Linear Regulator
ADP3303	3.3 V Low Dropout Linear Regulator

Precision Weigh Scale Design Using the AD7190 24-Bit Sigma-Delta ADC with Internal PGA

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

AD7190 Evaluation Board (EVAL-AD7190EBZ)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

This circuit is a weigh scale system that uses the AD7190, an ultralow noise, low drift, 24-bit sigma delta (Σ-Δ) analog-to-digital converter (ADC) with an internal programmable gain amplifier (PGA). The AD7190 simplifies the weigh scale design because most of the system building blocks are included on the chip. The AD7190 maintains good performance over the complete output data rate range, from 4.7 Hz to 4.8 kHz, which allows it to be used in weigh scale systems that operate at low speeds along with higher speed weigh scale systems, such as hopper scales.

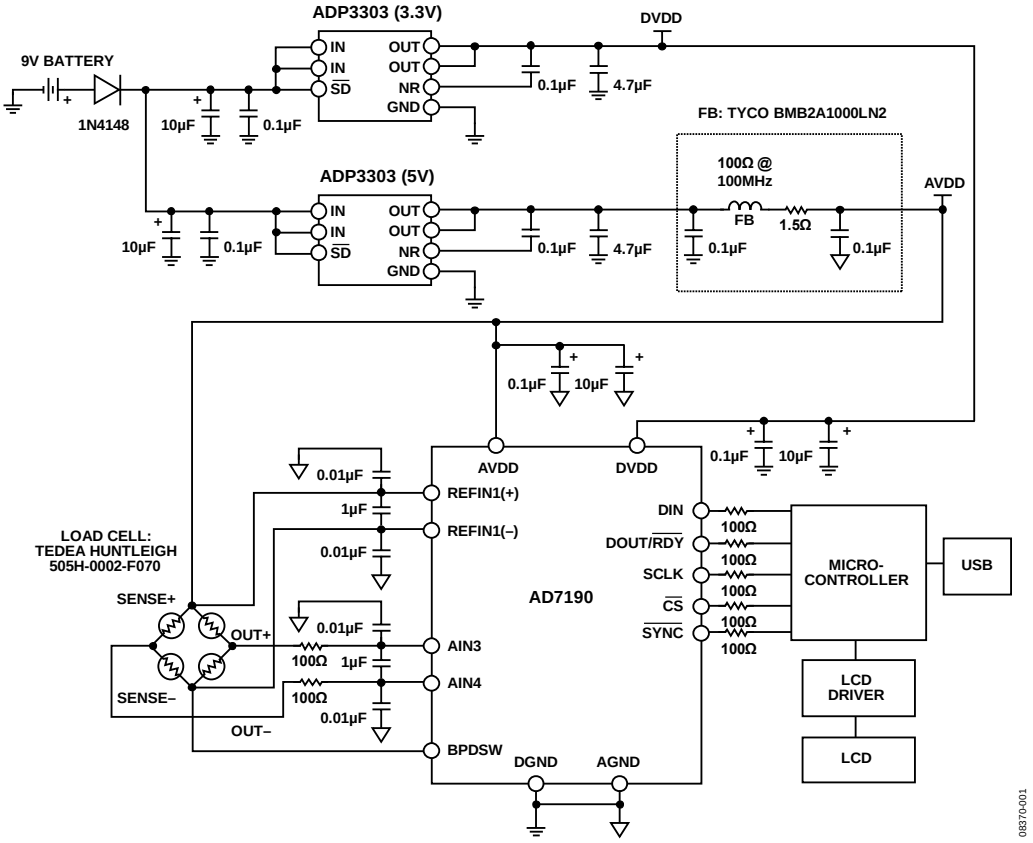

Figure 1. Weigh Scale System Using the AD7190 (Simplified Schematic: All Connections Not Shown)

Rev. A

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CIRCUIT DESCRIPTION

Because the AD7190 provides an integrated solution for weigh scales, it interfaces directly to the load cell. The only external components required are some filters on the analog inputs and capacitors on the reference pins for EMC purposes. The low level signal from the load cell is amplified by the internal PGA of the AD7190. The PGA is programmed to operate with a gain of 128. The conversions from the AD7190 are then sent to the microcontroller where the digital information is converted to weight and displayed on the LCD.

Figure 2 shows the actual test setup. A 6-wire load cell is used, because this gives the optimum system performance. A 6-wire load cell has two sense pins, in addition to the excitation, ground, and two output connections. The sense pins are connected to the high side and low side of the Wheatstone bridge. The voltage developed across the bridge can, therefore, be accurately measured, regardless of the voltage drop due to the wiring resistance. In addition, the AD7190 has differential analog inputs, and it accepts a differential reference. Connection of the load cell differential SENSE lines to the AD7190 reference inputs creates a ratiometric configuration that is immune to low frequency changes in the power supply excitation voltage. In addition, it eliminates the need for a precision reference. With a 4-wire load cell, the sense pins are not present, and the ADC reference pins are connected to the excitation voltage and ground. With this arrangement, the system is not completely ratiometric because there is a voltage drop between the excitation voltage and SENSE+ due to wiring resistance. There is also a voltage drop due to wire resistance on the low side.

Figure 2. Weigh Scale System Setup Using the AD7190

The AD7190 has separate analog and digital power supply pins. The analog section must be powered from 5 V. The digital power supply is independent of the analog power supply and can be any voltage between 2.7 V and 5.25 V. The microcontroller uses a 3.3 V power supply. Therefore, DVDD is also powered from 3.3 V. This simplifies the interface between the ADC and microcontroller because no external level shifting is required.

There are several methods to power the weigh scale system. It can be powered from the main power supply bus or battery powered (as shown in Figure 1). A 5 V low noise regulator is used to ensure that the AD7190 and the load cell receive a low noise supply. The ADP3303 (5 V) is used to generate the 5 V supply and is a low noise regulator. The filter network shown inside the dotted box ensures a low noise AVDD for the system. In addition, noise reduction capacitors are placed on the regulator output as recommended in the ADP3303 (5 V) data sheet. To optimize the EMC performance, the regulator output is filtered ahead of the AD7190 and the load cell. The 3.3 V digital supply is generated using the ADP3303 (3.3 V). It is essential that low noise regulators are used to generate all the power supply voltages to the AD7190 and the load cell, because any noise on the power supply or ground planes introduces noise into the system and degrades the circuit performance.

Figure 3 shows the rms noise of the AD7190 for different output data rates when the gain is equal to 128. Figure 3 shows that the rms noise increases as the output data rate increases. However, the device maintains good noise performance over the complete range of the output data rates.

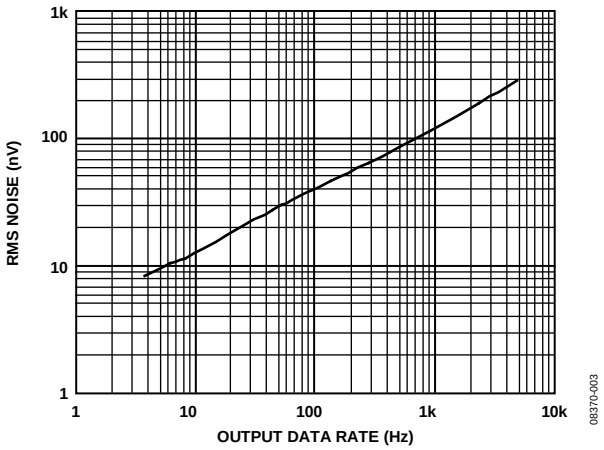

Figure 3. RMS Noise for Different Output Data Rates

If a 2 kg load cell with a sensitivity of 2 mV/V is used, the full-scale signal from the load cell is 10 mV when the excitation voltage is 5 V. A load cell has an offset, or TARE, associated with it. This TARE can have a magnitude that is up to 50% of the load cell full-scale output signal. The load cell also has a gain error that can be up to ±20% of full scale. Some customers use a DAC to remove or null the TARE. When the AD7190 uses a 5 V reference, its analog input range is equal to ±40 mV when the gain is set to 128 and the part is configured for bipolar operation. The wide analog input range of the AD7190 relative to the load cell full-scale signal (10 mV) is beneficial because it ensures that the offset and gain error of the load cell do not overload the front end of the ADC.

The AD7190 has an rms noise of 8.5 nV when the output data rate is 4.7 Hz. The number of noise-free counts is equal to

$$\frac{10\text{ mV}}{6.6\times 8.5\text{ nV}} = 178{,}250 \quad (1)$$

where the factor of 6.6 converts the rms voltage into a peak-to-peak voltage.

The resolution in grams is, therefore, equal to

$$\frac{2\text{ kg}}{178{,}250} = 0.01\text{ g} \quad (2)$$

The noise-free resolution is equal to

$$\log_2(178{,}250) = \frac{\log_{10}(178{,}250)}{\log_{10}(2)} = 17.4\text{ bits} \quad (3)$$

In practice, the load cell itself introduces some noise. There is also some time and temperature drift due to the load cell along with the drift of the AD7190. To determine the accuracy of the complete system, the weigh scale can be connected to a PC via the USB connector. Using LabVIEW software, the performance of the weigh scale system can be evaluated. Figure 4 shows the measured output performance when a 1 kg weight is placed on the load cell and 500 conversions are gathered. The noise of the system is calculated by the software to be 12 nV rms and 88 nV peak-to-peak. This equates to 113,600 noise-free counts, or 16.8 bits of noise-free code resolution.

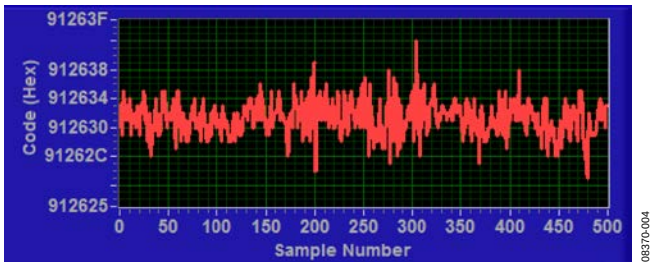

Figure 4. Measured Output Code for 500 Samples Showing the Effects of Noise

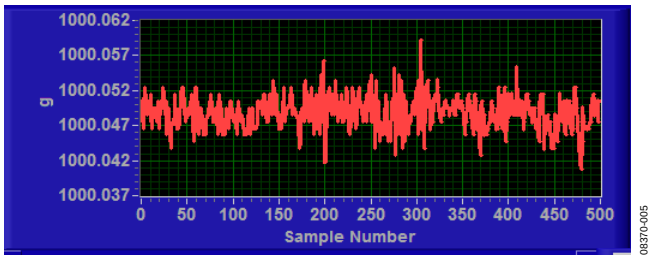

Figure 5. Measured Output in Grams for 500 Samples Showing the Effects of Noise

Figure 5 shows the performance in terms of weight. The peak-to-peak variation in output is 0.02 grams over the 500 codes. Therefore, the weigh scale system achieves an accuracy of 0.02 grams.

Figure 4 and Figure 5 show the actual (raw) conversions read back from the AD7190 when the load cell is attached. In practice, a digital post filter is used in a weigh scale system. The additional averaging that is performed in the post filter further improves the number of noise-free counts at the expense of a reduced data rate.

COMMON VARIATIONS

Note that all noise specifications in this section are given for a PGA gain of 128.

The AD7190 is a high precision ADC for high-end weigh scales. Other suitable ADCs are the AD7192 and AD7191. The AD7192 is pin-for-pin compatible with the AD7190. However, its rms noise is slightly higher. The AD7192 has an rms noise of 11 nV for an output data rate of 4.7 Hz, while the AD7190 has an rms noise of 8.5 nV at this output data rate. The AD7191 is a pin-programmable device. It has four output data rates and four gain settings. Due to its pin programmability and reduced feature set, it is an easy to use device. Its rms noise is the same as the rms noise of the AD7192.

For medium-end weigh scales, the AD7799 is a suitable device. At an output data rate of 4.17 Hz, the AD7799 has an rms noise of 27 nV.

Finally, for low-end weigh scales, the AD7798, AD7781 and AD7780 are suitable devices. The AD7798 has the same feature set as the AD7799. At 4.17 Hz, its rms noise is 40 nV. The AD7780 and AD7781 have one differential analog input and are pin programmable, allowing an output data rate of 10 Hz and 17.6 Hz and a gain of 1 or 128. The rms noise is 44 nV when the output data rate is 10 Hz.

As with any high accuracy circuit, proper layout, grounding, and decoupling techniques must be employed. See Tutorial MT-031, *Grounding Data Converters and Solving the Mystery of AGND and DGND* and Tutorial MT-101, *Decoupling Techniques* for more details.

A complete design support documentation package for this circuit note can be found at http://www.analog.com/CN0102-DesignSupport.

CIRCUIT EVALUATION AND TEST

With the exception of the external load cell and the PC, the circuit shown in Figure 1 is contained on the AD7190 evaluation board (EVAL-AD7190EBZ).

Interface to the evaluation board via a standard USB connector, J1. J1 is used to connect the evaluation board to the USB port of a PC. A standard USB connector cable is included with the AD7190 evaluation board to allow the evaluation board to interface with the USB port of the PC. Because the board is powered via the USB connector, there is no need for an external power supply, although if preferred, one may be connected via J2.

Equipment Needed

The EVAL-AD7190EBZ evaluation board and a PC running Windows® 2000, Windows XP, or Windows Vista (32-bit) are the only items required other than the external load cell. A Tedea Huntleigh 505H-0002-F070 load cell was used to obtain the results presented. The load cell is not shipped with the evaluation board and must be purchased from the manufacturer by the customer.

Getting Starting

The EVAL-AD7190EBZ evaluation board ships with a CD containing software to control the AD7190 that can be installed onto a standard PC. The software communicates with the AD7190 through the USB cable that accompanies the board. The software allows the user to read conversion data from the AD7190. Data can be read from the AD7190 and displayed or stored for later analysis.

Install the AD7190 evaluation board software using the supplied AD7190 evaluation board CD before connecting the board to the PC. For full details on this, refer to the UG-222 User Guide.

Functional Block

Figure 1 shows the basic functional block diagram of the test setup.

Setup and Test

Complete instructions for setup and testing of the AD7190 evaluation board can be found in UG-222 User Guide.

After installing the software, configure the AD7190 evaluation board for use with the external load cell by setting the appropriate links (jumpers) as described in Table 1 of the UG-222 User Guide. Ensure that the links are set before applying power to the evaluation board.

The load cell connects to the evaluation board header, J4. Operation of the **WeighScale Demo** is described in UG-222.

LEARN MORE

CN0102 Design Support Package:
http://www.analog.com/CN0102-DesignSupport

Kester, Walt. 1999. *Sensor Signal Conditioning*. Section 2. Analog Devices.

Kester, Walt. 1999. *Sensor Signal Conditioning*. Section 3. Analog Devices.

Kester, Walt. 1999. *Sensor Signal Conditioning*. Section 4. Analog Devices.

MT-004 Tutorial, *The Good, the Bad, and the Ugly Aspects of ADC Input Noise—Is No Noise Good Noise?* Analog Devices.

MT-022 Tutorial, *ADC Architectures III: Sigma-Delta ADC Basics,* Analog Devices.

MT-023 Tutorial, *ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD7190 Data Sheet

AD7190 Evaluation Board (EVAL-AD7190EBZ)

AD7191 Data Sheet

AD7192 Data Sheet

AD7780 Data Sheet

AD7781 Data Sheet

AD7798 Data Sheet

AD7799 Data Sheet

ADP3303 Data Sheet

REVISION HISTORY

12/12—Rev. 0 to Rev. A

Added Evaluation and Design Support Section 1
Changes to Common Variations Section 3
Added Circuit Evaluation and Test Section, Equipment Needed Section, Getting Started Section, Functional Block Section, and Setup and Test Section 4
Changes to Learn More Section 4

8/09—Revision 0: Initial Version

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Devices Connected/Referenced	
AD7780	Pin Programmable, Low Noise, Low Power 24-Bit Σ-Δ ADC with PGA
ADP3303	3.3 V Low Dropout Linear Regulator

Weigh Scale Design Using the AD7780 24-Bit Sigma-Delta ADC with Internal PGA

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

AD7780 Evaluation Board (EVAL-AD7780EBZ)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

This circuit is a weigh scale system that uses the AD7780. The AD7780 is a pin programmable, low power, low drift 24-bit Σ-Δ ADC that includes a PGA and uses an internal clock. Therefore, the device simplifies the weigh scale design since most of the system building blocks are included on the chip. The device consumes only 330 µA typically and is, therefore, suitable for any low power or battery application. The AD7780 also has a power-down mode that allows the user to switch off the power to the bridge sensor and power down the AD7780 when not converting, thus increasing the battery life.

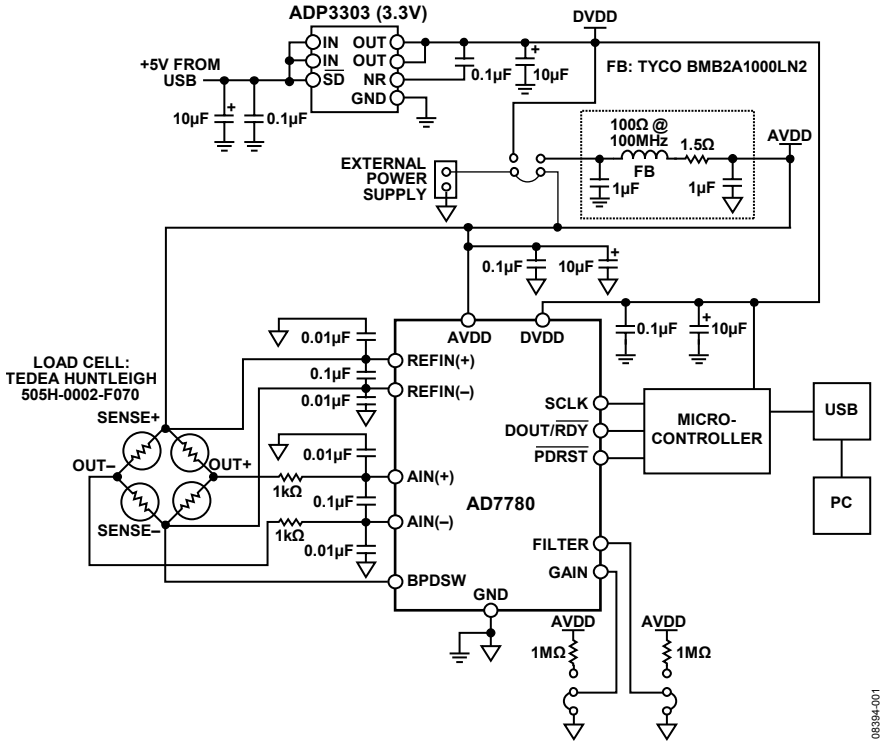

Figure 1. Weigh Scale System Using the AD7780 (Simplified Schematic: All Connections Not Shown)

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Figure 2. Weigh Scale System Setup Using the AD7780

CIRCUIT DESCRIPTION

Since the AD7780 provides an integrated solution for weigh scales, it interfaces directly to the load cell. The only external components required are some filters on the analog inputs and capacitors on the reference pins for EMC purposes. The low level signal from the load cell is amplified by the AD7780's internal PGA. The PGA is programmed to operate with a gain of 128. The conversions from the AD7780 are then sent to the PC using the USB interface where the digital information is converted to weight.

Figure 2 shows the actual test setup. A 6-wire load cell is used, as this gives the optimum system performance. A 6-wire load cell has two sense pins, in addition to the excitation, ground, and two output connections. The sense pins are connected to the high side and low side of the Wheatstone bridge. The voltage developed across the bridge can, therefore, be accurately measured regardless of the voltage drop due to the wiring resistance. In addition, the AD7780 has a differential analog input, and it accepts a differential reference. Connection of the load cell differential SENSE lines to the AD7780 reference inputs creates a ratiometric configuration that is immune to low frequency changes in the power supply excitation voltage.

With a 4-wire load cell, the sense pins are not present, and the ADC reference pins are connected to the excitation voltage and ground. With this arrangement, the system is not completely ratiometric because there will be a voltage drop between the excitation voltage and SENSE+ due to wiring resistance. There will also be a voltage drop due to wire resistance on the low side.

The AD7780 has separate analog and digital power supply pins. The analog and digital power supplies are independent of each other, so AVDD and DVDD can be at different potentials. The microcontroller uses a 3.3 V power supply. Therefore, DVDD is also powered from 3.3 V. This simplifies the interface between the ADC and the microcontroller because no external level shifting is required. The 3.3 V digital supply is generated using the ADP3303 (3.3 V) regulator.

There are several methods to power the weigh scale system. It can be powered from the main power supply bus or it can be powered from the ADP3303 (3.3 V). When the weigh scale is excited with 5 V, then the main power supply bus must be used. When exciting the load cell with 3.3 V, the main power supply bus or the ADP3303 (3.3 V) can be used. The ADP3303 (3.3 V) is a low noise regulator. In addition, noise reduction capacitors are placed on the regulator output as recommended in the ADP3303 (3.3 V) data sheet. To optimize the EMC, the regulator output is filtered before being supplied to the AD7780 and the load cell. It is essential that any regulators used to generate the power supply to the AD7780 and the load cell are low noise regulators, as any noise on the power supply or ground planes will introduce noise into the system and degrade the circuit performance.

If a 2 kg load cell with a sensitivity of 2 mV/V is used, the full-scale signal from the load cell is 10 mV when the excitation voltage is 5 V. A load cell has an offset, or TARE, associated with it. This TARE can have a magnitude that is up to 50% of the load cell full-scale output signal. The load cell also has a gain error that can be up to ±20% of full scale. Some customers use a DAC to remove or null the TARE. When the AD7780 uses a 5 V reference, its analog input range is equal to ±40 mV when the gain is set to 128. The wide analog input range of the AD7780 relative to the load cell full-scale signal (10 mV) is beneficial, as it ensures that the offset and gain error of the load cell do not overload the ADC's front end.

The AD7780 has an rms noise of 49 nV when the output data rate is 10 Hz. The number of noise-free counts is equal to

$$\frac{10\text{ mV}}{6.6 \times 49\text{ nV}} = 30{,}920 \quad (1)$$

where the factor of 6.6 converts the rms voltage into a peak-to-peak voltage.

The resolution in grams is, therefore, equal to

$$\frac{2\text{ kg}}{30{,}920} = 0.07\text{ g} \quad (2)$$

The noise free resolution is equal to

$$\log_2(30{,}920) = \frac{\log_{10}(30{,}920)}{\log_{10}(2)} = 14.9\text{ bits} \quad (3)$$

In practice, the load cell itself will introduce some noise. There will also be some time and temperature drift of the load cell along with the AD7780's drift. To determine the accuracy of the complete system, the weigh scale can be connected to the PC via the USB connector. Using LabView software, the performance of the weigh scale system can be evaluated. Figure 3 shows measured output performance when a 1 kg weight is placed on the load cell and 500 conversions are gathered (5 V excitation voltage used). The noise of the system is calculated by the software to 50 nV rms. This equates to 30,300 noise-free counts or 14.9 bits of noise-free code resolution.

Figure 4 shows the performance in terms of weight. The peak-to-peak variation in output is 0.075 grams over the 500 codes. So, the weigh scale system achieves an accuracy of 0.075 grams.

The plots show the actual (raw) conversions being read back from the AD7780 when the load cell is attached. In practice, a digital post filter is used in a weigh scale system.

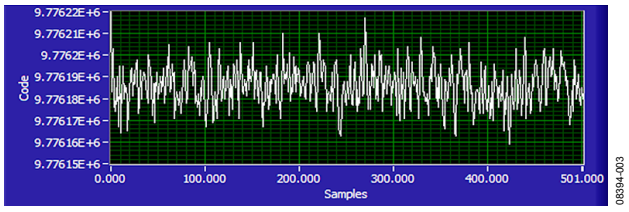

Figure 3. Measured Output Code for 500 Samples Showing the Effects of Noise

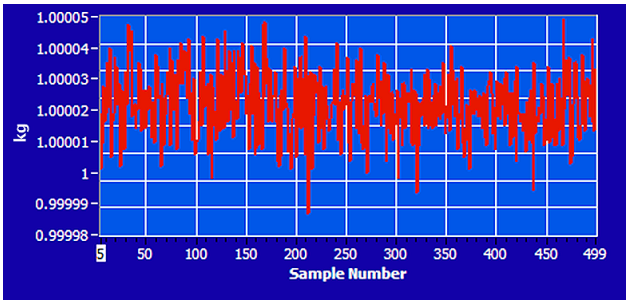

Figure 4. *Measured Output in Kilograms for 500 Samples Showing the Effects of Noise*

The additional averaging that is performed in the post filter will further improve the number of counts at the expense of a reduced data rate.

COMMON VARIATIONS

Note: The noise specifications given in this section are for a PGA gain of 128.

The AD7780 is a low noise, low power ADC for weigh scale design. Other suitable ADCs are the AD7798 and AD7781. The AD7781 has the same feature set as the AD7780, but it is a 20-bit ADC. The AD7798 allows a wider selection of output data rates. At 4.17 Hz, its rms noise is 40 nV.

For medium-end weigh scales, the AD7799 is a suitable device. At an output data rate of 4.17 Hz, the AD7799 has an rms noise of 27 nV.

For precision weigh scale design, the AD7190, AD7192, and AD7191 are suitable. The AD7190 has an rms noise of 8.5 nV when the output data rate is programmed to 4.7 Hz. It also offers a wide range of output data rates. It can operate up to 4.8 kHz and still maintain good performance. The AD7192 is pin-for-pin compatible with the AD7190. However, its rms noise is slightly higher. The AD7192 has an rms noise of 11 nV for an output data rate of 4.7 Hz. The AD7191 is a pin programmable device. It has four output data rates and four gain settings. Due to its pin programmability and reduced feature set, it is an easy to use device. Its rms noise is the same as the AD7192's rms noise.

As with any high accuracy circuit, proper layout, grounding, and decoupling techniques must be employed. See Tutorial MT-031, *Grounding Data Converters and Solving the Mystery of AGND and DGND* and Tutorial MT-101, *Decoupling Techniques* for more details.

A complete design support documentation package for this circuit note can be found at the following address: http://www.analog.com/CN0107-DesignSupport.

CIRCUIT EVALUATION AND TEST

With the exception of the external load cell and the PC, the circuit of Figure 1 is contained on the AD7780 evaluation board (EVAL-AD7780EBZ).

Interface to the evaluation board via a standard USB connector, J1. J1 is used to connect the evaluation board to the USB port of a PC. A standard USB connector cable is included with the AD7780 evaluation board to allow the evaluation board to interface with the USB port of the PC. Because the board is powered via the USB connector, there is no need for an external power supply, although if preferred, one may be connected via J2.

Equipment Needed

The EVAL-AD7780EBZ evaluation board and a PC running Windows 2000, Windows XP, or Windows Vista (32-bit) are the only items required other than the external load cell. A Tedea Huntleigh 505H-0002-F070 load cell was used to obtain the results presented in this circuit note. The load cell is not shipped with the evaluation board and must be purchased from the manufacturer by the customer.

Getting Starting

The EVAL-AD7780EBZ evaluation board is shipped with a CD containing software that can be installed onto a standard PC to control the AD7780. The software communicates with the AD7780 through the USB cable, which accompanies the board. The software allows you to read conversion data from the AD7780. Data can be read from the AD7780 and displayed or stored for later analysis.

Install the AD7780 evaluation board software using the supplied AD7780 evaluation board CD before connecting the board to the PC. Complete details can be found in UG-078.

Functional Block

Figure 1 shows the basic functional block diagram of the test setup.

Setup and Test

Complete instructions for setup and test of the AD7780 evaluation board can be found in user guide UG-078.

After installing the software, the AD7780 evaluation board should be configured for use with the external load cell by setting the appropriate links (jumpers) as described in Table 1 of UG-078. Make sure the links are set before applying power to the evaluation board.

The load cell connects to the evaluation board header J4. Operation of the Weighscale Demo is described in UG-078.

LEARN MORE

CN0107 Design Support Package:
http://www.analog.com/CN0107-DesignSupport

Kester, Walt. 1999. *Sensor Signal Conditioning*, Analog Devices. Sections 2, 3, 4.

MT-004 Tutorial, *The Good, the Bad, and the Ugly Aspects of ADC Input Noise—Is No Noise Good Noise?* Analog Devices.

MT-022 Tutorial, *ADC Architectures III: Sigma-Delta ADC Basics,* Analog Devices.

MT-023 Tutorial, *ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD7780 Data Sheet

AD7780 Evaluation Board

AD7781 Data Sheet

AD7190 Data Sheet

AD7191 Data Sheet

AD7192 Data Sheet

AD7780 Data Sheet

AD7798 Data Sheet

AD7799 Data Sheet

ADP3303 Data Sheet

REVISION HISTORY

11/10—Rev. 0 to Rev. A

Added Evaluation and Design Support Section 1
Changes to Circuit Description Section 3
Added Circuit Evaluation and Test Section 4

10/09—Revision 0: Initial Version

Circuits from the Lab

Circuits from the Lab™ tested circuit designs address common design challenges and are engineered for quick and easy system integration. For more information and/or support, visit www.analog.com/CN0108.

Devices Connected/Referenced	
AD7781	Pin Programmable, Low Noise, Low Power 20-Bit Σ-Δ ADC with PGA
ADP3303	3.3 V Low Dropout Linear Regulator

Weigh Scale Design Using the AD7781 20-Bit Sigma-Delta ADC with Internal PGA

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

AD7781 Evaluation Board (EVAL-AD7781EBZ)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

This circuit is a weigh scale system that uses the AD7781. The AD7781 is a pin programmable, low power, low drift 20-bit Σ-Δ converter that includes a PGA and uses an internal clock. Therefore, the device simplifies the weigh scale design since most of the system building blocks are included on the chip. The device consumes only 330 µA typically and is, therefore, suitable for any low power or battery application. The AD7781 also has a power-down mode that allows the user to switch off the power to the bridge sensor and power down the AD7781 when not converting, thus increasing the battery life.

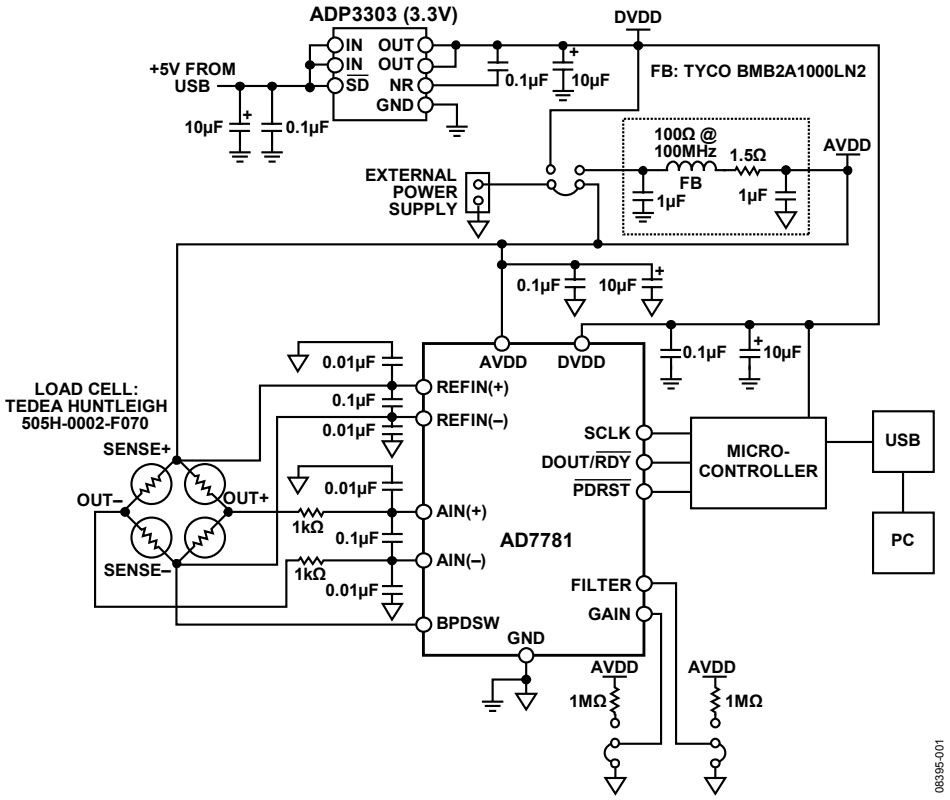

Figure 1. Weigh Scale System Using the AD7781 (Simplified Schematic: All Connections Not Shown)

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Figure 2. Weigh Scale System Using AD7781

CIRCUIT DESCRIPTION

Since the AD7781 provides an integrated solution for weigh scales, it interfaces directly to the load cell. The only external components required are some filters on the analog inputs and capacitors on the reference pins for EMC purposes. The low level signal from the load cell is amplified by the AD7781's internal PGA. The PGA is programmed to operate with a gain of 128. The conversions from the AD7781 are then sent to the PC using the USB interface where the digital information is converted to weight.

Figure 2 shows the actual test setup. A 6-wire load cell is used, as this gives the optimum system performance. A 6-wire load cell has two sense pins, in addition to the excitation, ground, and two output connections. The sense pins are connected to the high side and low side of the Wheatstone bridge. The voltage developed across the bridge can, therefore, be accurately measured regardless of the voltage drop due to the wiring resistance. In addition, the AD7781 has a differential analog input, and it accepts a differential reference. Connection of the load cell differential SENSE lines to the AD7781 reference inputs creates a ratiometric configuration that is immune to low frequency changes in the power supply excitation voltage.

With a 4-wire load cell, the sense pins are not present, and the ADC reference pins are connected to the excitation voltage and ground. With this arrangement, the system is not completely ratiometric because there will be a voltage drop between the excitation voltage and SENSE+ due to wiring resistance. There will also be a voltage drop due to wire resistance on the low side.

The AD7781 has separate analog and digital power supply pins. The analog and digital power supplies are independent of each other, so AVDD and DVDD can be at different potentials. The microcontroller uses a 3.3 V power supply. Therefore, DVDD is also powered from 3.3 V. This simplifies the interface between the ADC and the microcontroller because no external level shifting is required. The 3.3 V digital supply is generated using the ADP3303 (3.3 V) regulator.

There are several methods to power the weigh scale system. It can be powered from the main power supply bus or it can be powered from the ADP3303 (3.3 V). When the weigh scale is excited with 5 V, then the main power supply bus must be used. When exciting the load cell with 3.3 V, the main power supply bus or the ADP3303 (3.3 V) can be used. The ADP3303 (3.3 V) is a low noise regulator. In addition, noise reduction capacitors are placed on the regulator output as recommended in the ADP3303 (3.3 V) data sheet. To optimize the EMC, the regulator output is filtered before being supplied to the AD7781 and the load cell. It is essential that any regulators used to generate the power supply to the AD7781 and the load cell are low noise regulators, as any noise on the power supply or ground planes will introduce noise into the system and degrade the circuit performance.

If a 2 kg load cell with a sensitivity of 2 mV/V is used, the full-scale signal from the load cell is 10 mV when the excitation voltage is 5 V. A load cell has an offset, or TARE, associated with it. This TARE can have a magnitude that is up to 50% of the load cell full-scale output signal. The load cell also has a gain error that can be up to ±20% of full scale. Some customers use a DAC to remove or null the TARE. When the AD7781 uses a 5 V reference, its analog input range is equal to ±40 mV when the gain is set to 128. The wide analog input range of the AD7781 relative to the load cell full-scale signal (10 mV) is beneficial, as it ensures that the offset and gain error of the load cell do not overload the ADC's front-end.

The AD7781 (C grade) has an rms noise of 49 nV when the output data rate is 10 Hz. The number of counts is equal to

$$\frac{10\text{ mV}}{6.6 \times 49\text{ nV}} = 30{,}920 \quad (1)$$

where the factor of 6.6 converts the rms voltage into a peak-to-peak voltage.

The resolution in grams is

$$\frac{2\text{ kg}}{30{,}920} = 0.07\text{g} \quad (2)$$

The noise-free resolution is equal to

$$\log_2(30{,}920) = \frac{\log_{10}(30{,}920)}{\log_{10}(2)} = 14.9\ bits \quad (3)$$

In practice, the load cell itself will introduce some noise. There will also be some time and temperature drift of the load cell along with the AD7781's drift. To determine the accuracy of the complete system, the weigh scale can be connected to the PC via the USB connector. Using LabView software, the performance of the weigh scale system can be evaluated. Figure 3 shows measured output performance when a 1 kg weight is placed on the load cell and 500 conversions are gathered (5 V excitation voltage used). The noise of the system is calculated by the software to be 50 nV rms. This equates to 30,300 noise-free counts or 14.9 bits of noise-free code resolution.

Figure 4 shows the performance in terms of weight. The peak-to-peak variation in output is 0.075 grams over the 500 codes. So, the weigh scale system achieves an accuracy of 0.075 grams.

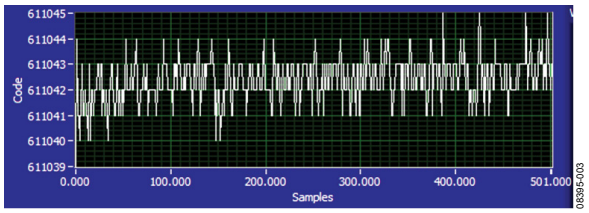

Figure 3. Measured Output Code for 500 Samples Showing the Effects of Noise

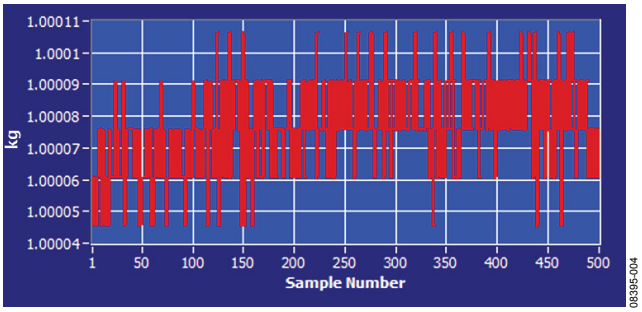

Figure 4. *Measured Output in Kilograms for 500 Samples Showing the Effects of Noise*

The plots show the actual (raw) conversions being read back from the AD7781 when the load cell is attached. In practice, a digital post filter is used in a weigh scale system. The additional averaging that is performed in the post filter will further improve the number of noise-free counts at the expense of a reduced data rate.

COMMON VARIATIONS

Note: The noise specifications given in this section are for a PGA gain of 128.

The AD7781 is a low noise, low power ADC for weigh scale design. Other suitable ADCs are the AD7798 and AD7780. The AD7780 has the same feature set as the AD7781, but it is a 24-bit ADC. The AD7798 allows a wider selection of output data rates. At 4.17 Hz, its rms noise is 40 nV.

For medium-end weigh scales, the AD7799 is a suitable device. At an output data rate of 4.17 Hz, the AD7799 has an rms noise of 27 nV.

For precision weigh scale design, the AD7190, AD7192, and AD7191 are suitable. The AD7190 has an rms noise of 8.5 nV when the output data rate is programmed to 4.7 Hz. It also offers a wide range of output data rates. It can operate up to 4.8 kHz and still maintain good performance. The AD7192 is pin-for-pin compatible with the AD7190. However, its rms noise is slightly higher. The AD7192 has an rms noise of 11 nV for an output data rate of 4.7 Hz. The AD7191 is a pin programmable device. It has four output data rates and four gain settings. Due to its pin programmability and reduced feature set, it is an easy to use device. Its rms noise is the same as the AD7192's rms noise.

As with any high accuracy circuit, proper layout, grounding, and decoupling techniques must be employed. See Tutorial MT-031, *Grounding Data Converters and Solving the Mystery of AGND and DGND* and Tutorial MT-101, *Decoupling Techniques* for more details.

A complete design support documentation package for this circuit note can be found at the following address: http://www.analog.com/CN0108-DesignSupport.

CIRCUIT EVALUATION AND TEST

With the exception of the external load cell and the PC, the circuit of Figure 1 is contained on the AD7780 Evaluation Board (EVAL-AD7781EBZ).

Interface to the evaluation board via a standard USB connector, J1. J1 is used to connect the evaluation board to the USB port of a PC. A standard USB connector cable is included with the AD7781 evaluation board to allow the evaluation board to interface with the USB port of the PC. Because the board is powered via the USB connector, there is no need for an external power supply, although if preferred, one may be connected via J2.

Equipment Needed

The EVAL-AD7781EBZ evaluation board and a PC running Windows 2000, Windows XP, or Windows Vista (32-bit) are the only items required other than the external load cell. A Tedea Huntleigh 505H-0002-F070 load cell was used to obtain the results presented in this circuit note. The load cell is not shipped with the evaluation board and must be purchased from the manufacturer by the customer.

Getting Starting

The EVAL-AD7781EBZ evaluation board is shipped with a CD containing software that can be installed onto a standard PC to control the AD7781. The software communicates with the AD7781 through the USB cable, which accompanies the board. The software allows you to read conversion data from the AD7781. Data can be read from the AD7781 and displayed or stored for later analysis.

Install the AD7781 evaluation board software using the supplied AD7781 evaluation board CD before connecting the board to the PC. Complete details can be found in user guide UG-079.

Functional Block

Figure 1 of this circuit note shows the basic functional block diagram of the test setup.

Setup and Test

Complete instructions for setup and test of the AD7781 evaluation board can be found in user guide UG-079.

After installing the software, the AD7781 evaluation board should be configured for use with the external load cell by setting the appropriate links (jumpers) as described in Table 1 of UG-079. Make sure the links are set before applying power to the evaluation board.

The load cell connects to the evaluation board header J4. Operation of the Weighscale Demo is described in UG-079.

LEARN MORE

CN0108 Design Support Package:
http://www.analog.com/CN0108-DesignSupport

Kester, Walt. 1999. *Sensor Signal Conditioning*, Analog Devices. Sections 2, 3, 4.

MT-004 Tutorial, *The Good, the Bad, and the Ugly Aspects of ADC Input Noise—Is No Noise Good Noise?* Analog Devices.

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Data Sheets and Evaluation Boards

AD7190 Data Sheet

AD7191 Data Sheet

AD7192 Data Sheet

AD7780 Data Sheet

AD7781 Data Sheet

AD7781 Evaluation Board

AD7798 Data Sheet

AD7799 Data Sheet

ADP3303 Data Sheet

REVISION HISTORY

11/10—Rev. 0 to Rev. A

Added Evaluation and Design Support Section 1
Changes to Common Variations Section 3
Added Circuit Evaluation and Test Section 4

10/09—Revision 0: Initial Version

CN08395-0-11/10(A)

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Devices Connected/Referenced	
AD9958/ AD9858	500 MSPS/1 GSPS Direct Digital Synthesizer (DDS)
AD9515	Clock Distribution IC and Pin Programmable Mini-Divider
AD6645	14-Bit, 80 MSPS/105 MSPS ADC

Low Jitter Sampling Clock Generator for High Performance ADCs Using the AD9958/AD9858 500 MSPS/1 GSPS DDS and AD9515 Clock Distribution IC

CIRCUIT FUNCTION AND BENEFITS

This circuit uses a direct digital synthesizer (DDS) with sub-Hertz tuning resolution as a low jitter sampling clock source for high performance ADCs. The AD9515 clock distribution IC provides PECL logic levels to the ADC. However, the AD9515 internal divider feature also allows the DDS to run at a higher frequency into the AD9515 front end, effectively increasing input slew rate. A higher slew rate into the AD9515 input squaring circuit can help reduce broadband jitter in the clock path.

Jitter on the ADC sampling clock produces degradation in the overall signal-to-noise ratio (SNR). The relationship is given by Equation 1.

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f t_j}\right) \quad (1)$$

where f is the full-scale analog input frequency, and t_j is the rms jitter. "SNR" in Equation 1 is the SNR due solely to clock jitter and does not depend on the resolution of the ADC.

The following data supports low jitter attainable from a DDS in clocking applications. Further details on Equation 1 and its use for evaluating the jitter on ADC sampling clocks can be found in Application Note AN-501.

CIRCUIT DESCRIPTION

The circuit configuration in Figure 1 shows a DDS-based clock generator, consisting of a DDS followed by a reconstruction filter and an AD9515 clock distribution IC, used to provide the sampling clock for an analog-to-digital converter (ADC). The DDS sampling clock is derived from a Rohde and Schwarz SMA signal generator. The jitter measurement was made by using the clock derived from the DDS and the AD9515 as the sampling clock for the high performance AD6645 14-bit, 80 MSPS/105 MSPS ADC. The analog input signal for the ADC is a filtered 170.3 MHz sine wave derived from a low jitter Wenzel crystal oscillator (www.wenzel.com). Data was taken on two different DDSes: the AD9958 (500 MSPS) and the AD9858 (1 GSPS).

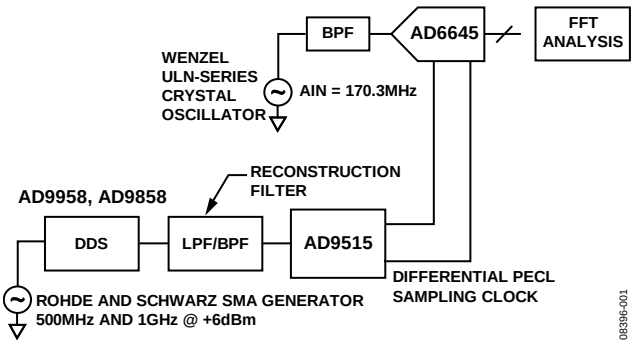

Figure 1. DDS-Based ADC Sampling Clock Generator (Simplified Diagram)

By evaluating the contribution of the ADC's differential non-linearity and thermal noise and then applying the DDS-based clock and measuring the ADC SNR, the added jitter attributable to the DDS-based clock can be derived. For more details on the measurement setup and the jitter calculations, refer to Application Note AN-823. Also, Application Note AN-837 is instructive for designing DAC reconstruction filters with optimal stop-band performance.

Table 1 shows data for the AD9958 test results. The data confirms that better jitter performance is achieved as the frequency, or slew rate, of the DDS output frequency is increased and as the DDS output filter pass band is decreased. Table 2 shows the AD9858 with a 5% band-pass filter, a 225 MHz low-pass filter, and various levels of DDS output power. As expected, lower jitter is achieved as power is increased and bandwidth reduced. With a 5% band-pass filter, the majority of the spurs from the DAC are attenuated. The jitter in this case is much more dependent on noise coupling between the DAC output and the limiter input. This is proven by the strong correlation between jitter reduction and increased

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slew rate. Note that rms jitter values consistently less than 1 ps can be achieved using the AD9858 circuit.

These circuits must be constructed on multilayer PC boards with large area ground planes using proper grounding, layout, and decoupling techniques (see MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND* and MT-101 Tutorial, *Decoupling Techniques*) in order to achieve these performance levels. Consult the evaluation board documentation for the AD9958, AD9858, AD9515, and AD6645 for more guidance.

Table 1. Jitter Response of AD9958 and AD9515 vs. f_{OUT}, Power, Frequency, and Filter BW

Product	DDS Sample Rate (MHz)	DDS Output Frequency (MHz)	DDS Output Power (dBm)	DDS Reconstruction Filter (MHz)	AD9515 Divider Output Setting	AD9515 Output Frequency (MHz)	Jitter (rms) (ps)
AD9958/AD9515	500	38.88	−3.6	200 LPF	1	38.88	4.1
AD9958/AD9515	500	38.88	−3.6	200 LPF	2	19.44	4.1
AD9958/AD9515	500	38.88	−4.7	47 LPF	1	38.88	2.4
AD9958/AD9515	500	38.88	−4.7	47 LPF	2	19.44	2.4
AD9958/AD9515	500	38.88	−3.3	5% BPF	1	38.88	1.5
AD9958/AD9515	500	38.88	−3.3	5% BPF	2	19.44	1.5
AD9958/AD9515	500	77.76	−3.8	200 LPF	1	77.76	2.5
AD9958/AD9515	500	77.76	−3.8	200 LPF	2, 4	38.88, 19.44	2.5
AD9958/AD9515	500	77.76	−4.9	85 LPF	1	77.76	1.5
AD9958/AD9515	500	77.76	−4.9	85 LPF	2, 4	38.88, 19.44	1.5
AD9958/AD9515	500	77.76	−3.8	5% BPF	1	77.76	1.1
AD9958/AD9515	500	77.76	−3.8	5% BPF	2, 4	38.88, 19.44	1.1
AD9958/AD9515	500	155.52	−5.5	200 LPF	2	77.76	1.5
AD9958/AD9515	500	155.52	−5.5	200 LPF	4, 8	38.88, 19.44	1.5
AD9958/AD9515	500	155.52	−5.6	5% BPF	2	77.76	0.68
AD9958/AD9515	500	155.52	−5.6	5% BPF	4, 8	38.88, 19.44	0.68

Table 2. Jitter Response of AD9858 and AD9515 vs. f_{OUT}, Power, Frequency, and Filter BW

Product	DDS Sample Rate (MHz)	DDS Output Frequency (MHz)	DDS Output Power (dBm)	DDS Reconstruction Filter (MHz)	AD9515 Divider Output Setting	AD9515 Output Frequency (MHz)	Jitter (rms) (ps)
AD9858/AD9515	1000	155.52	+7.7	225 LPF	2	77.76	0.56
AD9858/AD9515	1000	155.52	+7.7	225 LPF	4,8	38.88, 19.44	0.56
AD9858/AD9515	1000	155.52	+7.7	5% BPF	2	77.76	0.33
AD9858/AD9515	1000	155.52	+7.7	5% BPF	4, 8	38.88, 19.44	0.33
AD9858/AD9515	1000	155.52	+2.6	225 LPF	2	77.76	0.63
AD9858/AD9515	1000	155.52	+2.6	225 LPF	4, 8	38.88, 19.44	0.63
AD9858/AD9515	1000	155.52	+1.1	5% BPF	2	77.76	0.42
AD9858/AD9515	1000	155.52	+1.1	5% BPF	4, 8	38.88, 19.44	0.42
AD9858/AD9515	1000	155.52	−3.2	225 LPF	2	77.76	0.73
AD9858/AD9515	1000	155.52	−3.2	225 LPF	4, 8	38.88, 19.44	0.73
AD9858/AD9515	1000	155.52	−4.6	5% BPF	2	77.76	0.64
AD9858/AD9515	1000	155.52	−4.6	5% BPF	4, 8	38.88, 19.44	0.64

COMMON VARIATIONS

Analog Devices offers a variety of direct digital synthesizer, clock distribution chips, and clock buffers to build a DDS-based clock generator. Refer to www.analog.com/dds and www.analog.com/clock for more information.

LEARN MORE

AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*. Analog Devices.

AN-823 Application Note, *Direct Digital Synthesizers in Clocking Applications*. Analog Devices.

AN-837 Application Note, *DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance*. Analog Devices.

Kester, Walt. 2005. *The Data Conversion Handbook*. Analog Devices. Chapters 6 and 7.

Kester, Walt. 2006. *High Speed System Applications*. Analog Devices. Chapter 2, "Optimizing Data Converter Interfaces."

Kester, Walt. 2006. *High Speed System Applications*. Analog Devices. Chapter 3, "DACs, DDSs, PLLs, and Clock Distribution."

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Data Sheets and Evaluation Boards

AD6645 Data Sheet.

AD9515 Data Sheet.

AD9858 Data Sheet.

AD9958 Data Sheet.

AD6645 Evaluation Board.

AD9515 Evaluation Board.

AD9858 Evaluation Board.

AD9958 Evaluation Board.

REVISION HISTORY

7/09—Revision 0: Initial Version

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Devices Connected/Referenced	
AD5292	10-Bit, 1% Resistor Tolerance Digital Potentiometer
OP184	Rail-to-Rail Input and Output, Low Noise, High Slew Rate Operational Amplifier

Variable Gain Noninverting Amplifier Using the AD5292 Digital Potentiometer and the OP184 Op Amp

CIRCUIT FUNCTION AND BENEFITS

This circuit provides a low cost, high voltage, variable gain noninverting amplifier using the AD5292 digital potentiometer in conjunction with the OP184 operational amplifier.

The circuit offers 1024 different gains, controllable through an SPI-compatible serial digital interface. The ±1% resistor tolerance performance of the AD5292 provides low gain error over the full resistor range, as shown in Figure 2.

The circuit supports rail-to-rail inputs and outputs for both single-supply operation at +30 V and dual-supply operation at ±15 V, and is capable of delivering up to ±6.5 mA output current.

In addition, the AD5292 has an internal 20-times programmable memory that allows a customized gain setting at power-up.

The circuit provides accuracy, low noise, and low THD and is well suited for signal instrumentation conditioning.

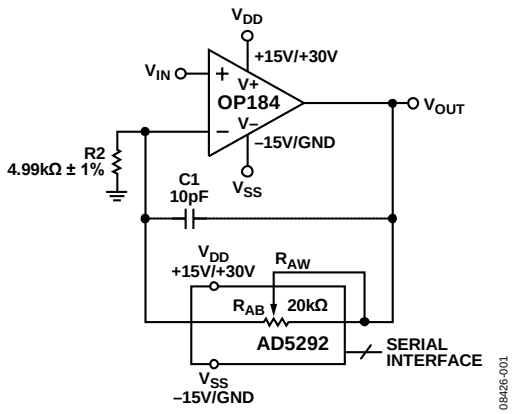

Figure 1. Variable Gain NonInverting Amplifier Simplified Schematic (Decoupling and All Connections Not Shown)

CIRCUIT DESCRIPTION

The circuit employs the AD5292 digital potentiometer in conjunction with the OP184 operational amplifier, providing a low cost, variable gain noninverting amplifier.

The input signal, V_{IN}, is amplified by the OP184. The op amp offers low noise, high slew rate, and rail-to-rail inputs and outputs.

The maximum circuit gain is defined in Equation 1.

$$G = 1 + \frac{R_{AB}}{R_2} \rightarrow R_2 = \frac{R_{AB}}{G-1} \quad (1)$$

The maximum current through the AD5292 is ±3 mA, which limits the maximum input voltage, V_{IN}, based on the circuit gain as described in Equation 2.

$$|V_{IN}| \leq 0.003 \times R_2 \quad (2)$$

When the input signal connected to V_{IN} is higher than the theoretical maximum value from Equation 2, R_2 should be increased, and the new gain can be recalculated using Equation 1.

The ±1% internal resistor tolerance of the AD5292 ensures a low gain error, as shown in Figure 2.

The circuit gain equation is

$$G = 1 + \frac{(1024 - D) \times {R_{AB}}/{1024}}{R_2} \quad (3)$$

where D is the code loaded in the digital potentiometer.

Rev. B

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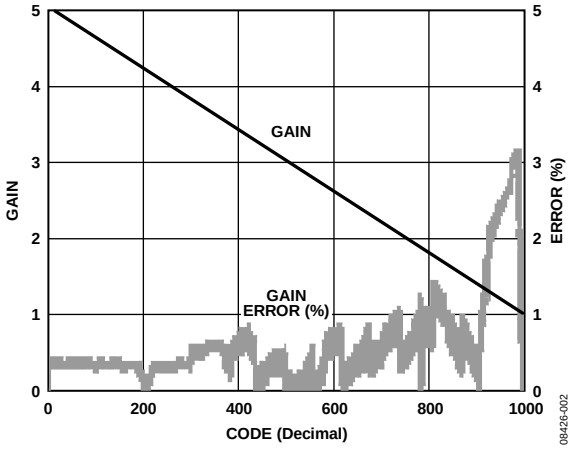

Figure 2. Gain and Gain Error vs. Decimal Code

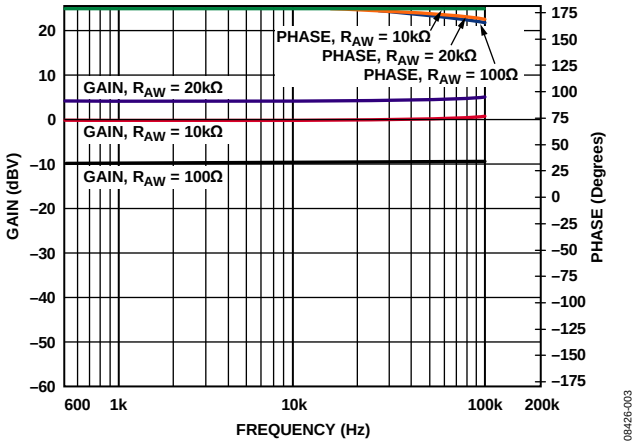

Figure 3. Gain and Phase vs. Frequency for AC Input Signal

When the circuit input is an ac signal, the parasitic capacitances of the digital potentiometer can cause undesirable oscillation in the output. This can be avoided, however, by connecting a small capacitor, C_1, between the inverter input and its output. A value of 10 pF was used for the gain and phase plots shown in Figure 3.

A simple modification of the circuit provides a logarithmic gain function, as shown in Figure 4. In this case, the digital potentiometer is configured in the ratiometric mode.

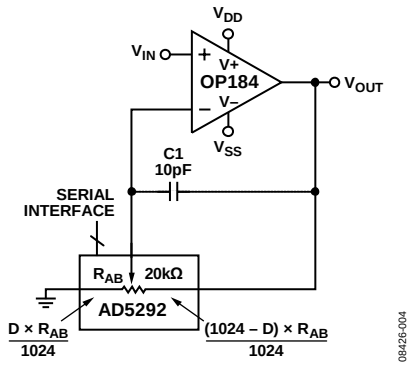

Figure 4. Logarithmic Gain Circuit

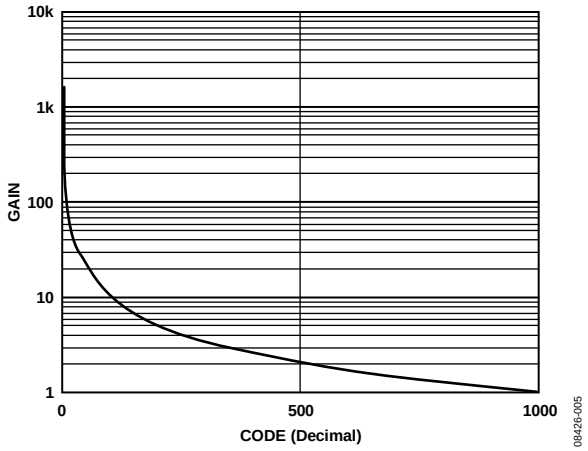

Figure 5. Logarithmic Gain Function

The circuit gain is defined in Equation 4

$$G = 1 + \frac{(1024 - D)}{D} = \frac{1024}{D} \quad (4)$$

where D is the code loaded in the digital potentiometer. A gain plot vs. code is shown in Figure 5.

The AD5292 has a 20-times programmable memory, which allows presetting the output voltage in a specific value at power-up.

Excellent layout, grounding, and decoupling techniques must be utilized in order to achieve the desired performance from the circuits discussed in this note (see Tutorial MT-031, *Grounding Data Converters and Solving the Mystery of AGND and DGND* and Tutorial MT-101, *Decoupling Techniques*). As a minimum, a 4-layer PCB should be used with one ground plane layer, one power plane layer, and two signal layers.

COMMON VARIATIONS

The AD5291 (8 bits with 20-times programmable power-up memory) and the AD5293 (10 bits with no power-up memory) are both ±1% tolerance digital potentiometers that are suitable for this application.

LEARN MORE

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-032 Tutorial, *Ideal Voltage Feedback (VFB) Op Amp*, Analog Devices.

MT-087 Tutorial, *Voltage References*, Analog Devices.

MT-091 Tutorial, *Digital Potentiometers*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD5291 Data Sheet.

AD5292 Data Sheet.

AD5292 Evaluation Board.

AD5293 Data Sheet.

OP184 Data Sheet.

REVISION HISTORY

3/10—Rev. A to Rev. B

Changes to Circuit Function and Benefits Section 1

12/09—Rev. 0 to Rev. A

Corrected trademark 1

8/09—Revision 0: Initial Version

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Devices Connected/Referenced	
AD5292	Digital Potentiometer, 10 Bits, 1% Resistor Tolerance
AD8221	Precision Instrumentation Amplifier

Low Cost, High Voltage, Programmable Gain Instrumentation Amplifier Using the AD5292 Digital Potentiometer and the AD8221 In-Amp

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 provides a low cost, high voltage, programmable gain instrumentation amplifier using the AD5292 digital potentiometer and the AD8221 instrumentation amplifier.

The circuit offers 1,024 different gain settings, controllable through an SPI digital interface. The ±1% resistor tolerance performance of the AD5292 provides low gain error over the full resistor range, as shown in Figure 2.

The circuit provides a high performance instrumentation amplifier that delivers the industry's highest CMRR over frequency in its class and dynamic programmable gain for both single supply operation at +30 V and dual supply operation at ±15 V. In addition, the AD5292 has an internal 20-times programmable memory that allows the user to customize the instrumentation amplifier gain at power-up.

The circuit provides accurate, low noise, high gain and is well suited for signal instrumentation conditioning, precision data acquisition, biomedical analysis, and aerospace instrumentation.

CIRCUIT DESCRIPTION

This circuit employs the AD5292 digital potentiometer in conjunction with the AD8221 instrumentation amplifier, providing an overall low cost, high voltage, programmable gain instrumentation amplifier.

The differential input signal, +IN and –IN, is amplified by the AD8221. The instrumentation amplifier offers accuracy, low noise, high CMRR, and high slew rate.

The maximum circuit gain is defined in Equation 1, where R_{AW_MIN} is the wiper resistance of the AD5292 in the rheostat mode and represents the minimum value of the gain-setting resistance (100 Ω).

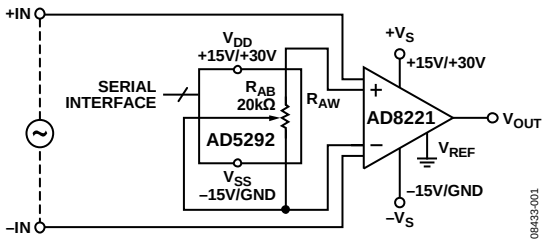

Figure 1. Programmable Gain Instrumentation Amplifier (Simplified Schematic: Decoupling and All Connections Not Shown)

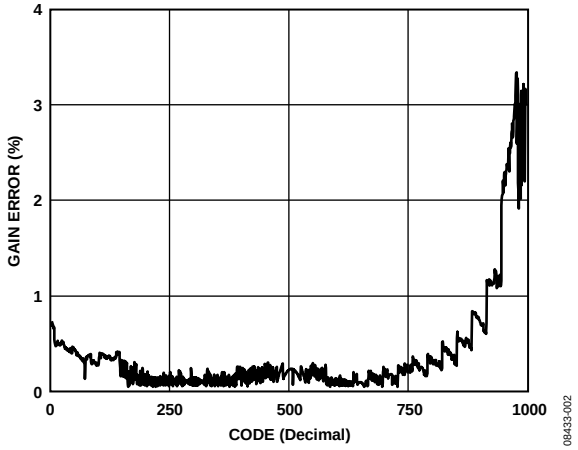

Figure 2. Gain Error vs. Code

$$G = 1 + \frac{49.4\,k\Omega}{R_{AB}} \le 1 + \frac{49.4\,k\Omega}{R_{AW\_MIN}} \le 500 \quad (1)$$

The circuit gain formula for any particular AD5292 resistance is

$$G = 1 + \frac{49.4\,k\Omega}{(1024 - D) \times R_{AB}/1024} \quad (2)$$

This equation is plotted in Figure 3 as a function of D, the decimal code.

Rev. A

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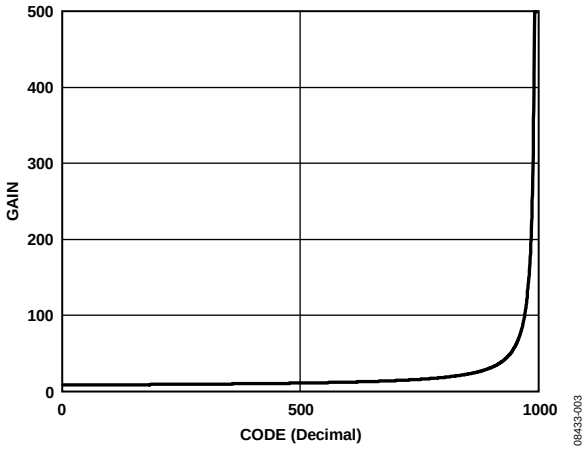

Figure 3. Gain vs. Decimal Code

The maximum current allowed through the AD5292 is ±3 mA, which limits the allowable circuit gain as a function of differential input voltage.

Equation 3 shows the maximum gain limit as a function of the differential input voltage, V_{IN}. This equation is derived by substituting $R_{AB} = V_{IN}/3$ mA into Equation 1. The equation is plotted in Figure 5.

$$G \le 1 + \frac{148}{V_{IN}} \quad (3)$$

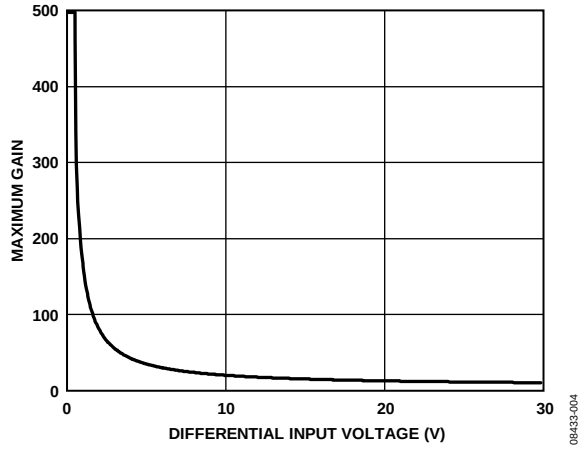

Figure 4. Allowable Gain vs. Differential Input Voltage

Equation 1 limits the maximum circuit gain to 500. Equation 2 can be solved for D, yielding Equation 4, which calculates the minimum allowable resistance (in terms of the digital code) in the AD5292 without exceeding the current limit.

$$D \ge 1024 - \left(\frac{49.4k\Omega \times 1024}{R_{AB} \times (G-1)} \right) \quad (4)$$

where D is the code loaded in the digital potentiometer, and G is the maximum gain calculated from Equation 3.

When the input to the circuit is an ac signal, the parasitic capacitances in the digital potentiometer can cause a reduction in the maximum AD8221 bandwidth. A gain and phase plot is shown in Figure 5.

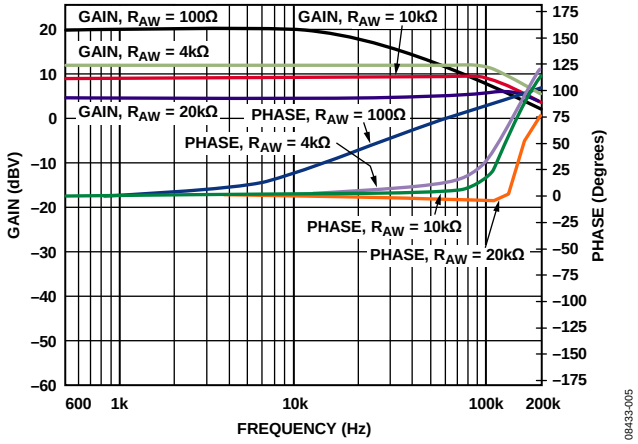

Figure 5. Gain and Phase vs. Frequency (Vertical Scale Compressed to Show All Gain Curves)

The AD5292 has a 20-times programmable memory, which allows presetting the output voltage in a specific value at power-up.

Excellent layout, grounding, and decoupling techniques must be used to achieve the desired performance from the circuits discussed in this note (see MT-031 Tutorial and MT-101 Tutorial). As a minimum, a 4-layer PCB should be used with one ground plane layer, one power plane layer, and two signal layers.

COMMON VARIATIONS

The AD5291 (eight bits with 20-times programmable power-up memory) and the AD5293 (10 bits, no power-up memory) are both ±1% tolerance digital potentiometers that are suitable for this application.

LEARN MORE

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND."* Analog Devices.

MT-032 Tutorial, *Ideal Voltage Feedback (VFB) Op Amp.* Analog Devices.

MT-061 Tutorial, *Instrumentation Amplifier (In-Amp) Basics.* Analog Devices.

MT-087 Tutorial, *Voltage References.* Analog Devices.

MT-091 Tutorial, *Digital Potentiometers.* Analog Devices.

MT-095 Tutorial, *EMI, RFI, and Shielding Concepts.* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques.* Analog Devices.

Data Sheets and Evaluation Boards

AD5292 Data Sheet.

AD5292 Evaluation Board.

AD8221 Data Sheet.

AD8221 Evaluation Board.

AD5291 Data Sheet.

AD5293 Data Sheet.

REVISION HISTORY

3/10—Rev. 0 to Rev. A

Changes to Circuit Function and Benefits Section..... 1

8/09—Revision 0: Initial Version

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Devices Connected/Referenced	
AD7191	4.8 kHz, Ultralow Noise, 24-Bit Σ-Δ ADC
ADP3303	5 V Low Dropout Linear Regulator
ADP3303	3.3 V Low Dropout Linear Regulator

Precision Weigh Scale Design Using the AD7191 24-Bit Sigma-Delta ADC with Internal PGA

CIRCUIT FUNCTION AND BENEFITS

This circuit is a weigh scale system that uses the AD7191. The AD7191 is a pin programmable, low noise, low drift, 24-bit Σ-Δ converter that includes a PGA and uses an internal clock. Therefore, the device simplifies the weigh scale design because most of the system building blocks are included on chip. The device has four output data rates and four gain settings that are selected using dedicated pins. This simplifies the interface to the ADC.

CIRCUIT DESCRIPTION

Since the AD7191 provides an integrated solution for weigh scales, it interfaces directly to the load cell. The only external components required are some filters on the analog inputs and capacitors on the reference pins for EMC purposes. The low level signal from the load cell is amplified by the AD7191's PGA. The PGA is programmed to operate with a gain of 128. The conversions from the AD7191 are then sent to the microcontroller where the digital information is converted to weight and displayed on the LCD.

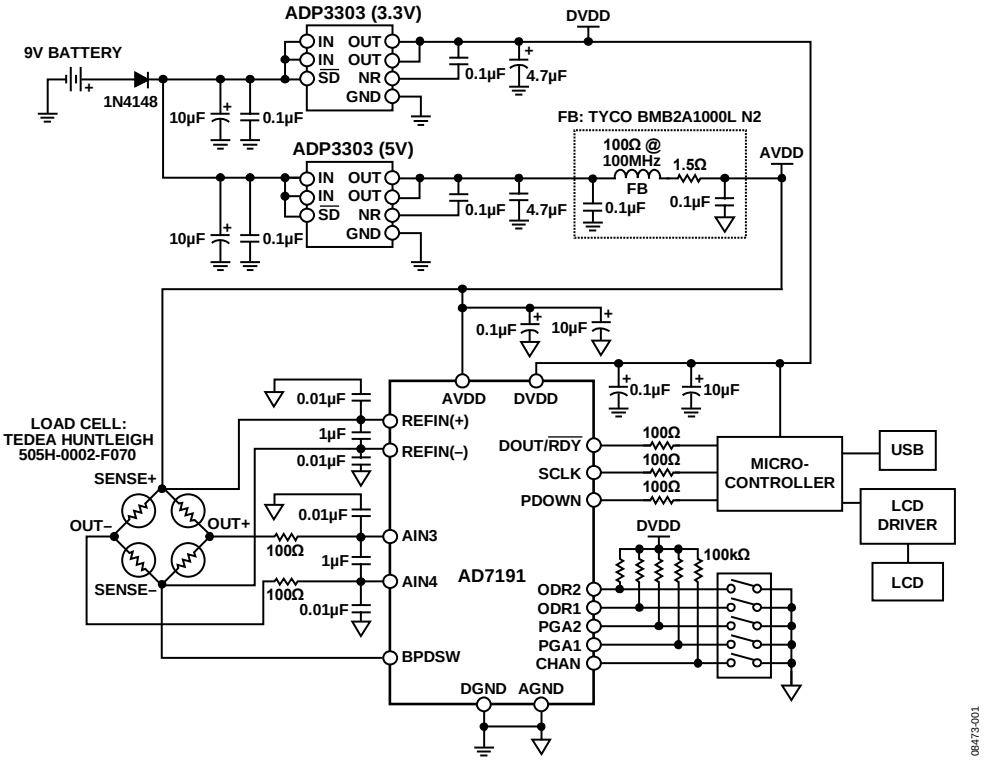

Figure 1. Weigh Scale System Using the AD7191 (Simplified Schematic: All Connections Not Shown)

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Figure 2. Weigh Scale System Using the AD7191

Figure 2 shows the actual test setup. A 6-wire load cell is used, as this gives the optimum system performance. A 6-wire load cell has two sense pins in addition to the excitation, ground, and two output connections. These sense pins are connected to the high side and low side of the Wheatstone bridge. The voltage developed across the bridge can, therefore, be accurately measured. In addition, the AD7191 has differential analog inputs and accepts a differential reference. Connection of the load cell differential SENSE lines to the AD7191 reference inputs creates a ratiometric configuration that is immune to low frequency changes in the power supply excitation voltage. With a 4-wire load cell the sense pins are not present, and the ADC reference pins are connected to the excitation voltage and ground. With this arrangement, the system is not completely ratiometric because there will be a voltage drop between the excitation voltage and SENSE+ due to wiring resistance. There will also be a voltage drop due to wire resistance on the low side.

The AD7191 has separate analog and digital power supplies. The digital power supply is independent of the analog power supply, and it can equal any voltage between 2.7 V and 5.25 V. The microcontroller uses a 3.3 V power supply. Therefore, DVDD is also powered from 3.3 V. This simplifies the interface between the ADC and the microcontroller because no external level shifting is required.

There are several methods to power the weigh scale system. It can be powered from the mains power supply or battery powered (as shown in Figure 1). A 5 V low noise regulator is used to ensure that the AD7191 and the load cell receive a low noise supply. A low noise ADP3303 (5 V) regulator is used to generate the 5 V supply. The filter network shown inside the dotted box ensures a low noise AVDD for the system. In addition, noise reduction capacitors are placed on the regulator output as recommended in the ADP3303 (5 V) data sheet. To optimize the EMC performance, the regulator output is filtered before being supplied to the AD7191 and the load cell. The 3.3 V digital supply is generated using the ADP3303 (3.3 V). It is essential that low noise regulators are used to generate all the power supply voltages to the AD7191 and the load cell, as any noise on the power supply or ground planes will introduce noise into the system and degrade the circuit performance.

If a 2 kg load cell with a sensitivity of 2 mV/V is used, the full-scale signal from the load cell is 10 mV when the excitation voltage is 5 V. A load cell has an offset or TARE associated with it. This TARE can have a magnitude that is up to 50 % of the load cell's full-scale output signal. The load cell also has a gain error that can be up to ±20% of full scale. Some customers use a DAC to remove or null the TARE. When the AD7191 uses a 5 V reference, its analog input range is equal to ±40 mV when the gain is set to 128. The wide analog input range of the AD7191 relative to the load cell full-scale signal (10 mV) is beneficial, as it ensures that the offset and gain error of the load cell do not overload the ADC's front-end.

The AD7191 has an rms noise of 15 nV when the output data rate is 10 Hz. The number of noise-free counts is equal to

$$\frac{10\text{ mV}}{6.6 \times 15\text{ nV}} = 101{,}000 \quad (1)$$

where the factor of 6.6 converts the rms voltage to a peak-to-peak voltage.

The resolution in grams is, therefore, equal to

$$\frac{2\text{ kg}}{101{,}000} = 0.02\text{ g} \quad (2)$$

and the noise-free code resolution is equal to

$$\log_2(101{,}000) = \frac{\log_{10}(101{,}000)}{\log_{10}(2)} = 16.6\text{ bits} \quad (3)$$

In practice, the load cell itself will introduce some noise. There also will be some drift due to time and temperature due to the load cell along with the AD7191's drift. To determine the accuracy of the complete system, the weigh scale can be connected to the PC via the USB connector. Using LabView software, the performance of the weigh scale system can be evaluated. Figure 3 shows the measured output performance when a 1 kg weight is placed on the load cell and 500 conversions are gathered. The noise of the system is calculated by the software to be 17 nV rms and 98 nV peak-to-peak. This equates to 102,000 noise-free counts or 16.6 bits of noise-free code resolution.

Figure 4 shows the performance in terms of weight. The peak-to-peak variation in output is 0.02 grams over the 500 codes. Therefore, the weigh scale system achieves an accuracy of 0.02 grams.

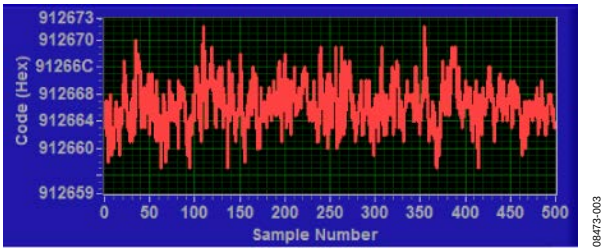

Figure 3. Measured Output Code for 500 Samples Showing the Effects of Noise

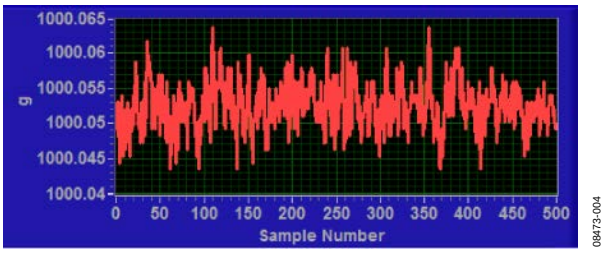

Figure 4. Measured Output in Grams for 500 Samples Showing the Effects of Noise

The plots show the actual conversions being read back from the AD7191 when the load cell is attached. In practice, a digital post filter is used in a weigh scale system. The additional averaging that is performed in the post filter will further improve the number of noise-free counts at the expense of a reduced data rate.

COMMON VARIATIONS

Note: All noise specifications in this section are given for a PGA gain of 128.

The AD7191 is a pin-programmable ADC for high-end weigh scales. Other suitable ADCs are the AD7190 and AD7192. The AD7190 has an rms noise of 8.5 nV when the output data rate is programmed to 4.7 Hz. It also offers a wide range of output data rates. It can operate up to 4.8 kHz and still maintain good performance. The AD7192 is pin-for-pin compatible with the AD7190. However, its rms noise is slightly higher. The AD7192 has an rms noise of 11 nV for an output data rate of 4.7 Hz.

For medium-end weigh scales, the AD7799 is a suitable device. At an output data rate of 4.17 Hz, the AD7799 has an rms noise of 27 nV.

Finally, for low-end weigh scales, the AD7798, AD7781 and AD7780 are suitable devices. The AD7798has the same feature set as the AD7799. At 4.17 Hz, its rms noise is 40 nV. The AD7780 and AD7781 have one differential analog input and are pin-programmable, allowing an output data rate of 10 Hz and 17.6 Hz and a gain of 1 or 128. The rms noise is 44 nV when the output data rate is 10 Hz.

As with any high accuracy circuit, proper layout, grounding, and decoupling techniques must be employed. See Tutorial MT-031, *Grounding Data Converters and Solving the Mystery of AGND and DGND* and Tutorial MT-101, *Decoupling Techniques* for more details.

LEARN MORE

Kester, Walt. 1999. *Sensor Signal Conditioning*. Sections 2, 3, 4. Analog Devices.

MT-004 Tutorial, *The Good, the Bad, and the Ugly Aspects of ADC Input Noise—Is No Noise Good Noise?* Analog Devices.

MT-022 Tutorial, *ADC Architectures III: Sigma-Delta ADC Basics,* Analog Devices.

MT-023 Tutorial, *ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD7190 Data Sheet

AD7191 Data Sheet

AD7191 Evaluation Board

AD7192 Data Sheet

AD7780 Data Sheet

AD7781 Data Sheet

AD7798 Data Sheet

AD7799 Data Sheet

ADP3303 Data Sheet

REVISION HISTORY

7/13—Rev. 0 to Rev. A

Changes to Circuit Description Section..... 3

10/09—Revision 0: Initial Version

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Devices Connected/Referenced	
AD7192	4.8 kHz, Ultralow Noise 24-Bit Σ-Δ ADC with PGA
ADP3303	5 V Low Dropout Linear Regulator
ADP3303	3.3 V Low Dropout Linear Regulator

Precision Weigh Scale Design Using the AD7192 24-Bit Sigma-Delta ADC with Internal PGA

CIRCUIT FUNCTION AND BENEFITS

This circuit is a weigh scale system that uses the AD7192. The AD7192 is an ultralow noise, low drift, 24-bit Σ-Δ converter that includes a PGA. Therefore, the device simplifies the weigh scale design because most of the system building blocks are included on chip. Since the part operates with an output data rate from 4.7 Hz to 4.8 kHz and maintains good performance over the complete output data rate range, this allows the part to be used in weigh scale systems that operate at low speeds along with higher speed weigh scale systems, such as hopper scales.

CIRCUIT DESCRIPTION

Since the AD7192 provides an integrated solution for weigh scales, it interfaces directly to the load cell. The only external components required are some filters on the analog inputs and capacitors on the reference pins for EMC purposes. The low level signal from the load cell is amplified by the AD7192's PGA. The PGA is programmed to operate with a gain of 128. The conversions from the AD7192 are then sent to the microcontroller where the digital information is converted to weight and displayed on the LCD.

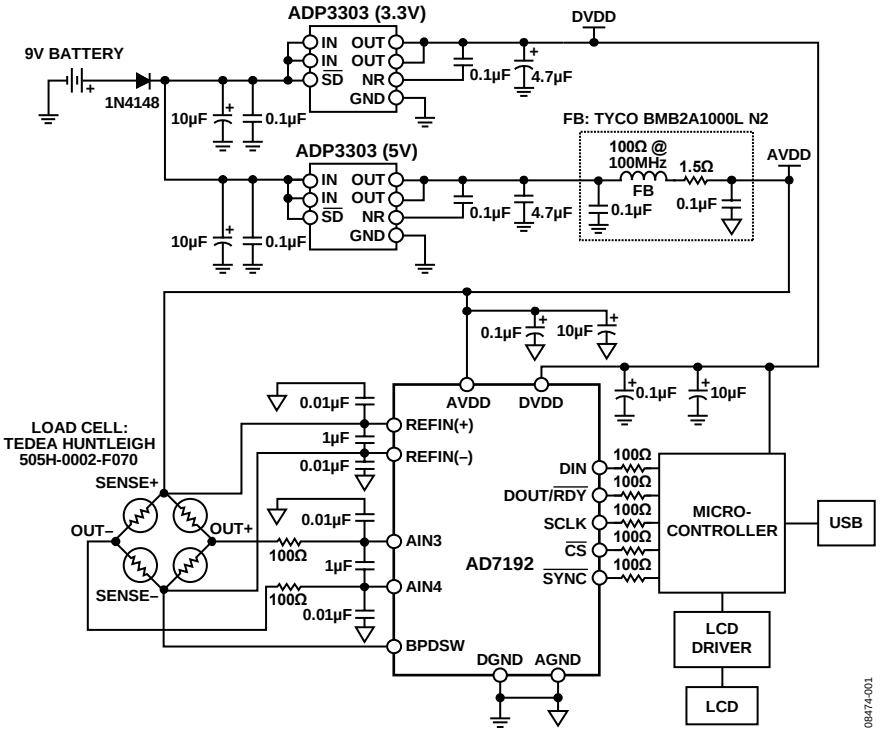

Figure 1. Weigh Scale System Using the AD7192 (Simplified Schematic: All Connections Not Shown)

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Figure 2 shows the actual test setup. A 6-wire load cell is used, as this gives the optimum system performance. A 6-wire load cell has two sense pins, in addition to the excitation, ground, and two output connections. These sense pins are connected to the high side and low side of the Wheatstone bridge. The voltage developed across the bridge can, therefore, be accurately measured. In addition, the AD7192 has differential analog inputs, and it accepts a differential reference. Connection of the load cell differential SENSE lines to the AD7192 reference inputs creates a ratiometric configuration that is immune to low frequency changes in the power supply excitation voltage. With a 4-wire load cell, the sense pins are not present, and the ADC reference pins are connected to the excitation voltage and ground. With this arrangement, the system is not completely ratiometric because there will be a voltage drop between the excitation voltage and SENSE+ due to wire resistance. There will also be a voltage drop due to wire resistance on the low side.

The AD7192 has separate analog and digital power supplies. The digital power supply is independent of the analog power supply and can equal any voltage between 2.7 V and 5.25 V. The microcontroller uses a 3.3 V power supply. Therefore, DVDD is also powered from 3.3 V. This simplifies the interface between the ADC and the microcontroller because no external level shifting is required.

There are several methods to power the weigh scale system. It can be powered from the mains power supply or battery powered (as shown in Figure 1). A 5 V low noise regulator is used to ensure that the AD7192 and the load cell receive a low noise supply. An ADP3303 (5 V) low noise regulator is used to generate the 5 V supply. The filter network shown inside the dotted box ensures a low noise AVDD for the system. In addition, noise reduction capacitors are placed on the regulator output as recommended in the ADP3303 (5 V) data sheet. To optimize the EMC performance, the regulator output is filtered before being supplied to the AD7192 and the load cell. The 3.3 V digital supply is generated using the ADP3303 (3.3 V). It is essential that low noise regulators are used to generate all the power supply voltages to the AD7192 and the load cell, as any noise on the power supply or ground planes will introduce noise into the system and degrade the circuit performance.

Figure 2. Weigh Scale System Using the AD7192

If a 2 kg load cell with a sensitivity of 2 mV/V is used, the full-scale signal from the load cell is 10 mV when the excitation voltage is 5 V. A load cell has an offset or TARE associated with it. This TARE can have a magnitude that is up to 50% of the load cell's full-scale output signal. The load cell also has a gain error, which can be up to ±20% of full scale. Some customers use a DAC to remove or null the TARE. When the AD7192 uses a 5 V reference, its analog input range is equal to ±40 mV when the gain is set to 128 and the part is configured for bipolar operation. The wide analog input range of the AD7192 relative to the load cell's full-scale signal (10 mV) is beneficial as it ensures that the offset and gain error of the load cell do not overload the ADC's front end.

The AD7192 has an rms noise of 11 nV when the output data rate is 4.7 Hz. The number of noise-free counts is equal to

$$\frac{10\text{ mV}}{6.6 \times 11\text{ nV}} = 137{,}740 \quad (1)$$

where the factor of 6.6 converts the rms voltage into a peak-to-peak voltage.

The resolution in grams is

$$\frac{2\text{ kg}}{137{,}740} = 0.015\text{ g} \quad (2)$$

The noise-free code resolution is equal to

$$\log_2(137{,}740) = \frac{\log_{10}(137{,}740)}{\log_{10}(2)} = 17\text{ bits} \quad (3)$$

In practice, the load cell itself will introduce some noise. There will also will be some drift due to time and temperature of the load cell along with the AD7192's drift. To determine the accuracy of the complete system, the weigh scale can be connected to the PC via the USB connector. Using LabView software, the performance of the weigh scale system can be evaluated. Figure 4 shows the measured output performance when a 1 kg weight is placed on the load cell and 500 conversions are gathered. The noise of the system is calculated by the software to be 14 nV and is 98 nV peak-to-peak. This equates to 102,000 noise-free counts or 16.6 bits of noise-free code resolution.

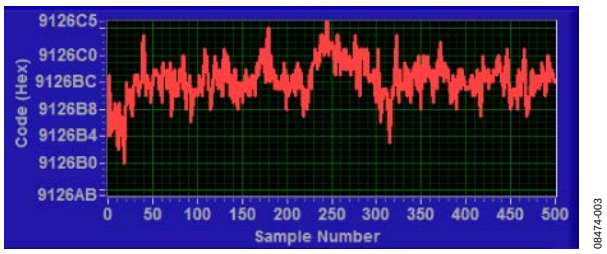

Figure 3. Measured Output Code for 500 Samples Showing the Effects of Noise

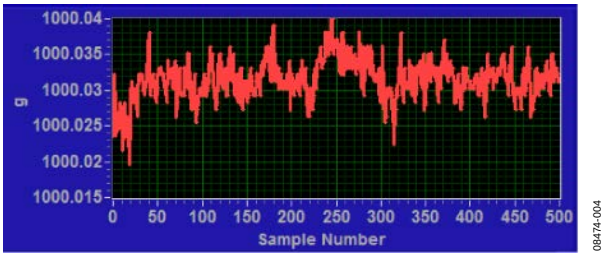

Figure 4. Measured Output Code for 500 Samples Showing the Effects of Noise

Figure 4 shows the performance in terms of weight. The variation in output is 0.02 grams over the 500 codes. So, the weigh scale system achieves an accuracy of 0.02 grams.

The plots show the actual conversions being read back from the AD7192 when the load cell is attached. In practice, a digital post filter is used in a weigh scale system. The additional averaging that is performed in the post filter will further improve the number of noise-free counts at the expense of a reduced data rate.

COMMON VARIATIONS

Note: All noise specifications in this section are given for a PGA gain of 128.

The AD7192 is a high precision ADC for high-end weigh scales. Other suitable ADCs are the AD7190 and AD7191. The AD7190 is pin-for-pin compatible with the AD7192. However, its rms noise is slightly lower. The AD7190 has an rms noise of 8.5 nV for an output data rate of 4.7 Hz while the AD7192 has an rms noise of 11 nV at this output data rate. The AD7191 is a pin programmable device. It has four output data rates and four gain settings. Due to its pin programmability and reduced feature set, it is an easy to use device. Its rms noise is the same as the AD7192's rms noise.

For medium-end weigh scales, the AD7799 is a suitable device. At an output data rate of 4.17 Hz, the AD7799 has an rms noise of 27 nV.

Finally, for low-end weigh scales, the AD7798, AD7781, and AD7780 are suitable devices. The AD7798 has the same features set as the AD7799. At 4.17 Hz, its rms noise is 40 nV. The AD7780 and AD7781 have one differential analog input and are pin programmable, allowing an output data rate of 10 Hz and 17.6 Hz and a gain of 1 or 128. The rms noise is 44 nV when the output data rate is 10 Hz.

As with any high accuracy circuit, proper layout, grounding, and decoupling techniques must be employed. See Tutorial MT-031, *Grounding Data Converters and Solving the Mystery of AGND and DGND* and Tutorial MT-101, *Decoupling Techniques* for more details.

LEARN MORE

Kester, Walt. 1999. *Sensor Signal Conditioning*. Sections 2, 3, 4. Analog Devices.

MT-004 Tutorial, *The Good, the Bad, and the Ugly Aspects of ADC Input Noise—Is No Noise Good Noise?* Analog Devices.

MT-022 Tutorial, *ADC Architectures III: Sigma-Delta ADC Basics,* Analog Devices.

MT-023 Tutorial, *ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD7190 Data Sheet

AD7191 Data Sheet

AD7192 Data Sheet

AD7192 Evaluation Board

AD7780 Data Sheet

AD7781 Data Sheet

AD7798 Data Sheet

AD7799 Data Sheet

ADP3303 Data Sheet

REVISION HISTORY

7/13—Rev. 0 to Rev. A

Changes to Circuit Description Section 3

9/09—Revision 0: Initial Version

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Devices Connected/Referenced	
AD5360	16-Channel, 16-Bit Voltage-Output DAC
AD790	High Speed Precision Comparator
AD8597	Low Noise Amplifier
ADR435	5 V Ultralow Noise Voltage Reference

Automated Calibration Technique That Reduces the AD5360 16-Channel, 16-Bit DAC Offset Voltage to Less Than 1 mV

CIRCUIT FUNCTION AND BENEFITS

The circuit described in this document and shown in Figure 1 provides a method of calibrating that removes an unknown offset error. When using high precision, high resolution DACs in industrial process control and instrumentation applications, low offset is often a critical specification. The circuit uses built-in features of the AD5360 in conjunction with an external comparator and an operational amplifier to determine if the DAC output voltages are above or below a ground reference signal. With the amount of offset known, the user can adjust the codes sent to the DAC to null out the offset.

CIRCUIT DESCRIPTION

The AD5360 is a 16 channel, 16-bit digital to analog converter. The nominal output range is ±10 V when used with a 5 V reference. The AD5360 contains two offset DACs. Each offset DAC is connected to a group of eight DACs and is used to adjust the mid-scale point of the output span. For example, the offset DAC can be programmed to change the output span from ±10 V to −8 V to +12 V, or other values as required by the application.

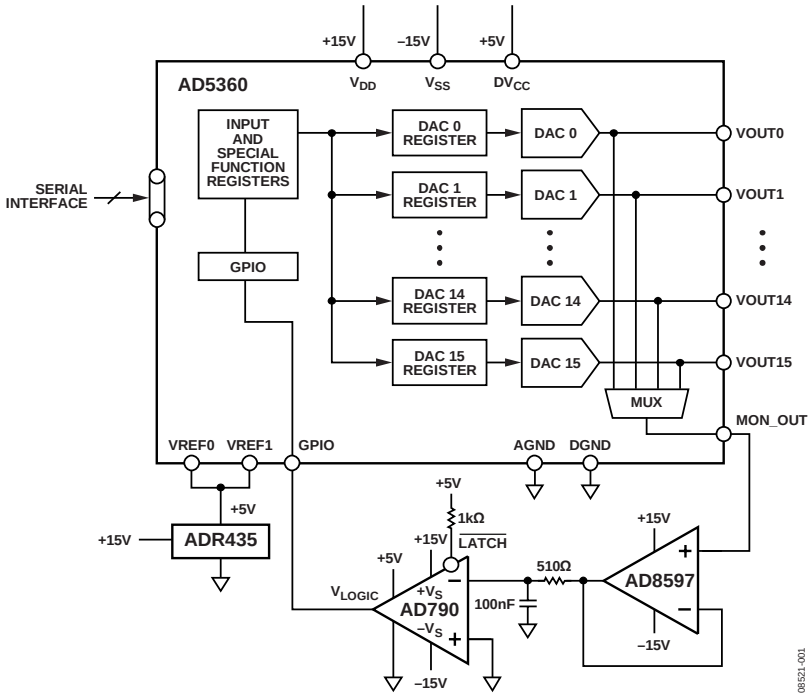

Figure 1. Autocalibration Circuit for AD5360 DAC That Reduces the Offset Voltage to Less Than 1 mV (Simplified Schematic: Decoupling and All Connections Not Shown).

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The AD5360 is factory trimmed to have a very low offset. The trimming is done with the offset DAC at its default value, and the offset error due to the offset DAC is effectively removed. When the value of the offset DAC is changed from its default value, however, its offset error affects the offset error of the main DACs.

The circuit described here allows for the offset error of the main DACs to be measured and calibrated out under those conditions. The circuit relies on a general-purpose I/O pin and an on-chip monitor multiplexer. The GPIO (general-purpose I/O) pin is set as an input, and by reading the GPIO internal register, the logic status of the GPIO pin is determined. The analog multiplexer is programmable to connect any of the 16 DAC outputs to a single pin, the MON_OUT pin. The multiplexer switches have a low but finite on resistance, R_{ON} so that any current drawn from MON_OUT creates a voltage drop across R_{ON} and, therefore, an output error. To prevent this, MON_OUT is buffered by an AD8597 low-noise amplifier. The low pass filter following the amplifier reduces the amount of noise seen by the AD790 high speed precision comparator and prevents false triggering.

The AD790 can be operated on ±15 V supplies, making it compatible with the AD5360. The AD790 also requires an additional +5 V V_{LOGIC} supply when operating on ±15 V supplies. In addition, the AD790 has a 15 V maximum differential input voltage; therefore, it can tolerate the output voltages from the AD5360 without attenuation. In Figure 1, the comparator output is low if the channel offset is positive, indicating that the output voltage must be reduced to remove the offset. The comparator output is high if the channel offset is negative, indicating that the output voltage must be increased to remove the offset.

To calibrate a DAC, the DAC channel is loaded with the digital value, which should ideally provide a voltage equal to SIGGND (that is, 0 V). In this example the DAC channel is assumed to have a negative offset. Reading the GPIO register shows that the comparator output is low, indicating that the input must be incremented until the output toggles. As progressively higher codes are written to the DAC input register, the GPIO register is read until the comparator trips to the high state. The AD790 has a maximum hysteresis band of 0.65 mV; therefore, reducing the DAC code again allows a more accurate determination of the DAC offset.

When comparator output trips back to the low state, SIGGND is somewhere between those two codes. Due to the errors of the components used in the circuit, there is typically a span of three or four codes between comparator trip points. There is no way to determine exactly which code gives the lowest offset output using this method, but by picking a code that is the average of the two trip point codes, the DAC channel offset is typically less than 1 mV from SIGGND.

Excellent layout, grounding, and decoupling techniques must be used to achieve the desired performance from the circuits discussed in this note (see MT-031 Tutorial and MT-101 Tutorial). As a minimum, a 4-layer PCB should be used with one ground plane layer, one power plane layer, and two signal layers.

COMMON VARIATIONS

The AD5362 is an 8-channel version of the AD5360. The AD5361 and AD5363 are 14-bit versions of the AD5360 and AD5362, respectively. The AD8599 is a dual version of the AD8597.

The circuit described here can be used with any of the AD536x devices mentioned above. The reference can also be changed to give different output ranges if required.

LEARN MORE

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND,"* Analog Devices.

MT-083 Tutorial, *Comparators*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD5360

AD5361

AD5362

AD5363

AD5360, AD5361, AD5362, AD5363 Evaluation Board

AD8597

AD790

ADR435

REVISION HISTORY

9/09—Revision 0: Initial Version

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Devices Connected/Referenced	
AD5360	16-Channel, 16-Bit Voltage Output DAC
ADR431/ ADR421	2.5 V Ultralow Noise Voltage Reference
ADR435	5 V Ultralow Noise Voltage Reference

16 Channels of Programmable Output Span Using the AD5360 16-Bit Voltage Output DAC

CIRCUIT FUNCTION AND BENEFITS

This circuit is a multichannel DAC configuration with different output spans on groups of channels. It utilizes the AD5360 to provide 16 DAC channels with 16 bits of resolution. The AD5360 is configured to have eight channels with an output span of ±10 V and eight channels with an output span of ±5 V.

CIRCUIT DESCRIPTION

The AD5360 is a 16-channel, 16-bit DAC available both in 56-lead LFCSP and 52-lead LQFP packages. The AD5360 has two reference input pins. VREF0 is the reference pin for DAC channels VOUT0 to VOUT7. VREF1 is the reference pin for DAC channels VOUT8 to VOUT15.

Figure 1 shows a typical configuration for the AD5360 using two external references. The nominal output span for the AD5360 is four times the reference voltage, with the mid-scale point at 0 V. The ADR431 and ADR421 are low noise precision 2.5 V references. The ADR435 is a low noise precision 5 V reference. When connected as shown in Figure 1, the AD5360 will have an output span of ±5 V on VOUT0 to VOUT7 and an output span of ±10 V on VOUT8 to VOUT15. The AD5360 has two offset DAC registers, which allow the mid-scale point of the span to be altered within the limits of part functionality and headroom.

The circuit must be constructed on a multilayer PC board with a large area ground plane. Proper layout, grounding, and decoupling techniques must be used to achieve optimum performance (see Tutorial MT-031 and Tutorial MT-101).

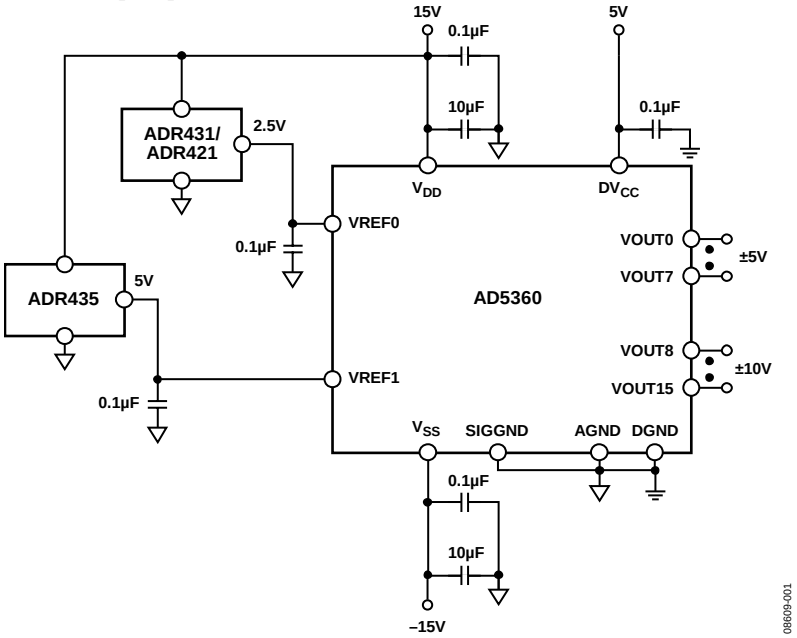

Figure 1. 16 Channels of Programmable Output Voltage Span Using the AD5360 DAC (Simplified Schematic: Decoupling and All Connections Not Shown)

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COMMON VARIATIONS

The AD5362 is an 8-channel version of the AD5360. The AD5361 and AD5363 are 14-bit versions of the AD5360 and AD5362, respectively.

The circuit described here can be used with any of the AD536x devices mentioned above. The references can also be changed to give different output ranges if required.

LEARN MORE

Kester, Walt. *The Data Conversion Handbook*. Chapter 3, 7. Analog Devices. 2005.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

Voltage Reference Wizard Design Tool. Analog Devices.

Data Sheets and Evaluation Boards

AD5360 Data Sheet

AD5360 Evaluation Board

AD5361 Data Sheet

AD5362 Data Sheet

AD5363 Data Sheet

ADR421 Data Sheet

ADR431 Data Sheet

ADR435 Data Sheet

REVISION HISTORY

10/09—Revision 0: Initial Version

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Devices Connected/Referenced	
ADXL345	3-Axis, ±2 *g*/±4 *g*/±8 *g*/±16 *g* Digital Accelerometer
ADuC7024	Precision Analog Microcontroller, 12-Bit Analog I/O, ARM7TDMI® MCU

Sensing Low-*g* Acceleration Using the ADXL345 Digital Accelerometer Connected to the ADuC7024 Precision Analog Microcontroller

CIRCUIT FUNCTION AND BENEFITS

The ADXL345 is a small, thin, low power, 3-axis accelerometer with high resolution (13-bit) measurement up to ±16 *g*. Digital output data is formatted as 16-bit twos complement and is accessible through either an SPI (3- or 4-wire) or I²C digital interface.

The ADXL345 is well suited for mobile device applications. It measures the static acceleration of gravity in tilt-sensing applications, as well as dynamic acceleration resulting from motion or shock. Its high resolution (4 mg/LSB) enables measurement of inclination changes of about 0.25°. Using a digital output accelerometer such as the ADXL345 eliminates the need for analog-to-digital conversion, reducing system cost and real estate. Additionally, the ADXL345 includes a variety of built-in features. Activity/inactivity detection, tap/double-tap detection, and free-fall detection are all done internally with no need for the host processor to perform any calculations. A built-in 32-stage FIFO memory buffer reduces the burden on the host processor, allowing algorithm simplification and power savings. Additional system level power savings can be implemented using the built-in activity/inactivity detection and by using the ADXL345 as a "motion switch" to turn the whole system off when no activity is felt and on when activity is sensed again.

The ADXL345 communicates via I²C or SPI interface. The circuits described in this document demonstrate how to implement communication via these protocols.

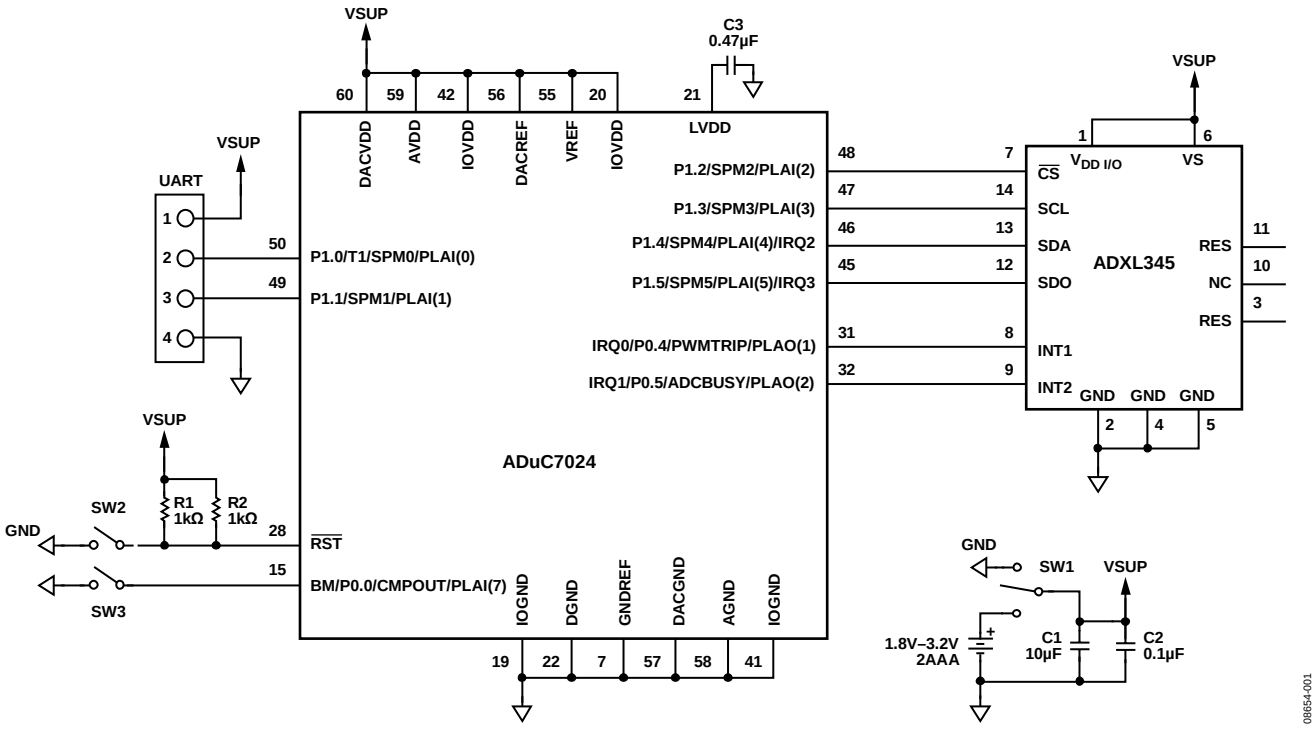

Figure 1. ADXL345 and ADuC7024 in 4-Wire SPI Configuration (Simplified Schematic: Decoupling and All Connections Not Shown)

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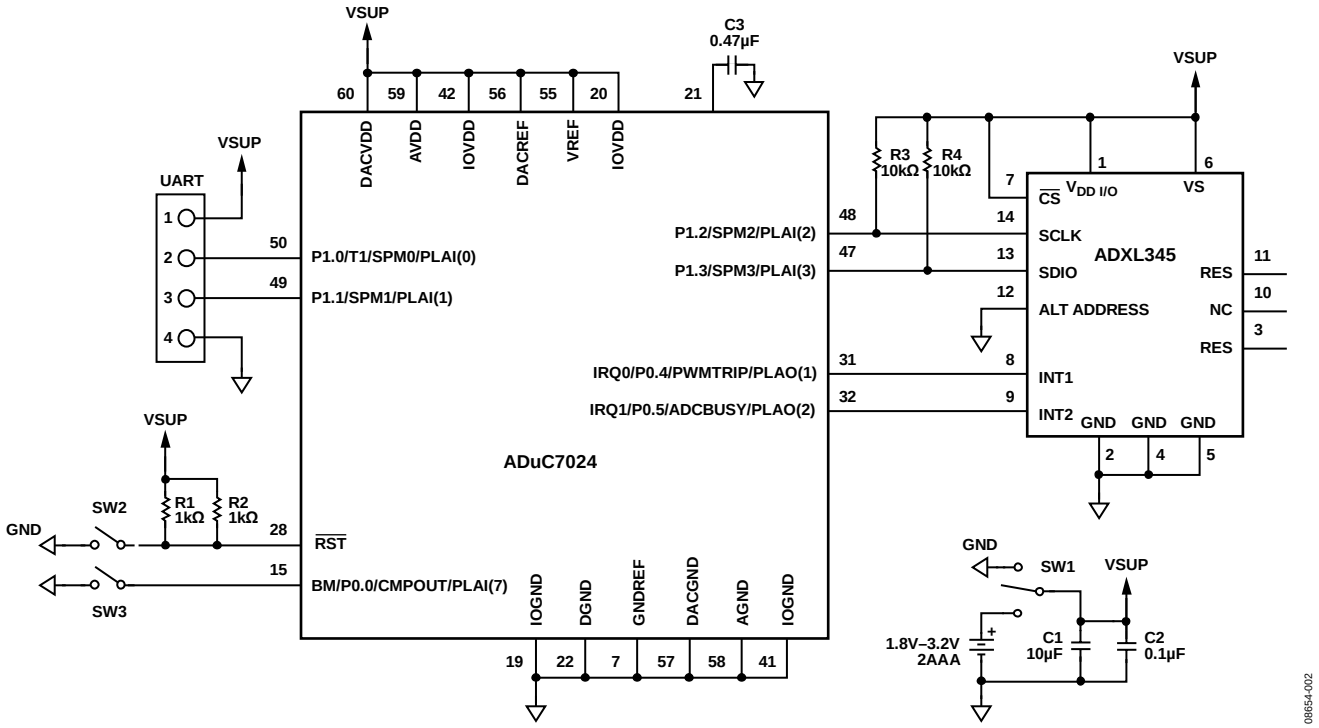

Figure 2. ADXL345 and ADuC7024 in I²C Configuration (Simplified Schematic: Decoupling and All Connections Not Shown)

CIRCUIT DESCRIPTION

This circuit uses an ADuC7024 precision analog microcontroller in conjunction with the ADXL345 digital accelerometer. Both are I²C- and SPI-ready. Figure 1 shows the ADXL345 and ADuC7024 in an SPI configuration, and Figure 2 shows the same devices in an I²C configuration. The $\overline{CS}$ pin (Pin 7 on the ADXL345) is used to select the desired interface. I²C mode is enabled if the $\overline{CS}$ pin is tied high to $V_{DD\ I/O}$. In SPI mode, $\overline{CS}$ is toggled to signify the beginning and end of each transmission. When $\overline{CS}$ is pulled high, this indicates that no SPI transmission is occurring or that an I²C transmission may occur.

Both schematics are simplified, but required connections (supplies, ground connections, etc.) are shown. In these schematics, the ADuC7024 is programmed via UART (connected to Pin 49 and Pin 50). SW2 and SW3 are Reset and Download buttons, respectively, for programming the microcontroller. SW1 is an on/off power switch.

COMMON VARIATIONS

Figure 1 shows the ADXL345 in a 4-wire SPI configuration. The ADXL345 can also communicate via 3-wire SPI. Figure 3 outlines this configuration.

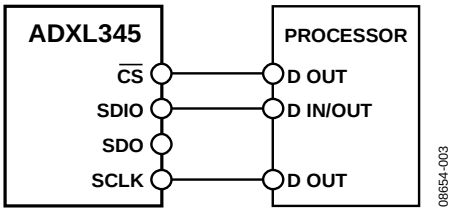

Figure 3. 3-Wire SPI Connection Diagram

The circuit described uses the ADuC7024 microcontroller. The same configuration can be applied with any SPI- or I²C-capable microcontroller, as outlined in the diagrams in Figure 4. The standard I²C and SPI connections are used. Pin functions for the two protocols are listed in Table 1.

Table 1. ADXL345 Pin Functionality in SPI and I²C Communication Modes

		Functionality	
ADXL345 Pin Number	**Pin Name**	**I²C**	**SPI**
7	$\overline{CS}$	(Connect to V_{DD} for I²C)	Chip Select
12	SDO/ALT ADDRESS	Alternate Address Select	Serial Data Output
13	SDA/SDI/SDIO	Serial Data	Serial Data Input (SPI 4-Wire)/ Serial Data Input and Output (SPI 2-Wire)
14	SCL/SCLK	Serial Communications Clock	Serial Communications Clock

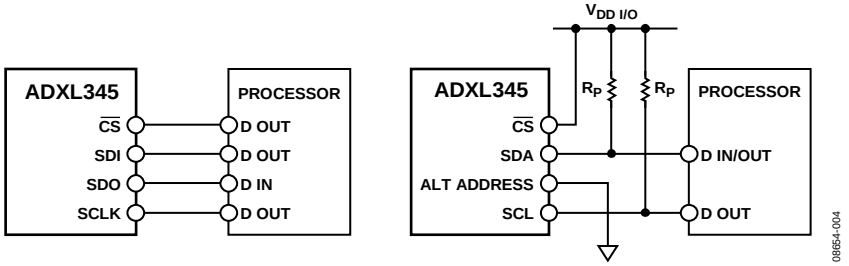

Figure 4. SPI (left) and I²C (right) Connection Diagrams

LEARN MORE

This circuit is used in the ADXL345 Development Board (model number EVAL-ADXL345Z-DB). For information on ADXL345 operation and register functions, please refer to the ADXL345 data sheet.

For information on programming the ADuC7024, please see the ADuC7024 data sheet. Sample code for the I²C configuration shown in Figure 2 is available at www.analog.com/static/imported-files/circuit_notes/CN0133_Source_Code.zip.

Data Sheets and Evaluation Boards

ADXL345 Data Sheet

ADXL345 Evaluation Tools

ADuC7024 Data Sheet

ADuC7024 Evaluation Tools

REVISION HISTORY

10/09—Revision 0: Initial Version

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Devices Connected/Referenced	
ADL5356	1.2 GHz to 2.5 GHz, Dual-Balanced Mixer, LO Buffer, IF Amplifier, and RF Balun
AD8376	Ultralow Distortion IF Dual VGA
AD9258	14-Bit, 125 MSPS, 1.8 V Dual ADC
AD9517-4	12-Output Clock Generator with Integrated 1.6 GHz VCO

High Performance, Dual Channel IF Sampling Receiver

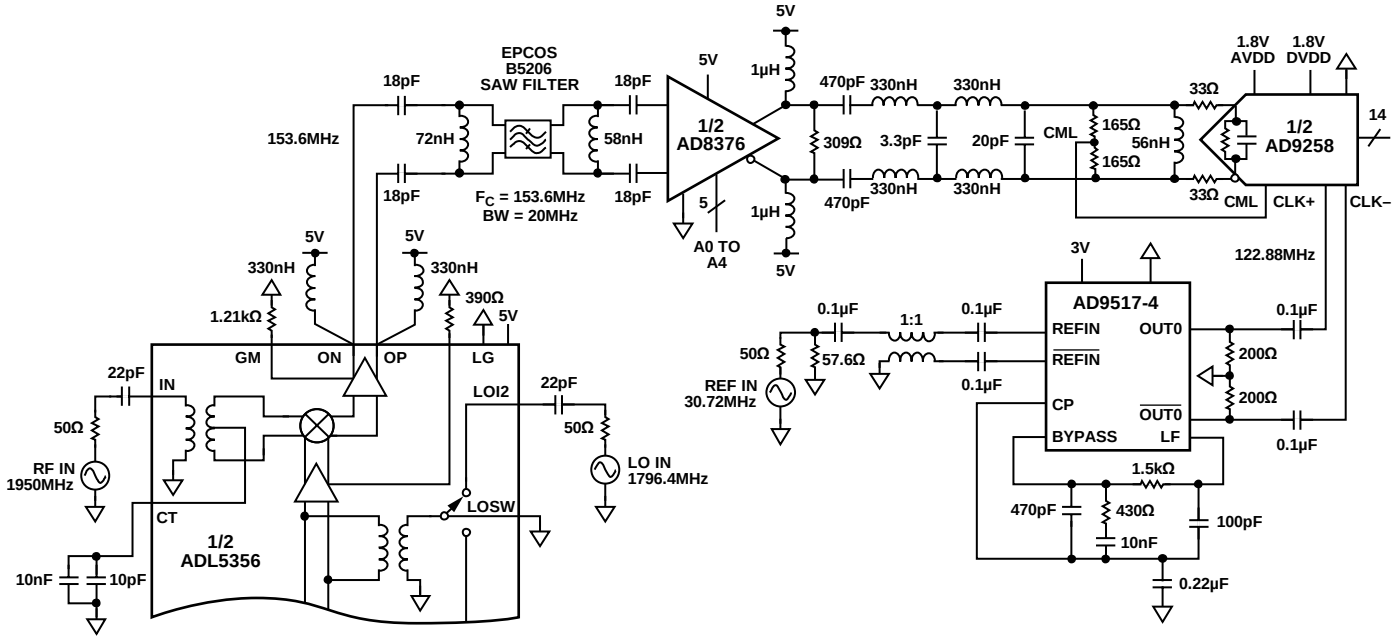
CIRCUIT FUNCTION AND BENEFITS

This circuit is a high performance, dual channel IF sampling receiver, also called a "main" and "diversity" receiver in base station terminology. The downconverting receiver uses a single IF frequency of 153.6 MHz and includes a dual downconverting mixer, digitally controlled dual VGA, dual ADC, and clock synthesizer. The circuit takes an incoming RF waveform and outputs a dual 14-bit resolution digital data stream. It is optimized for high frequency IF sampling and provides exceptional spurious-free dynamic range (SFDR) performance of 79.61 dBc with a sampling rate of 122.88 MSPS at the high gain setting.

CIRCUIT DESCRIPTION

This circuit includes the RF front end, as well as the IF sampling receiver. It is composed of a dual balanced mixer, broadband IF SAW filter, digitally controlled dual VGA, and dual ADC. The circuit also includes a synthesizer, which generates the ADC sampling clock.

The ADL5356 dual balanced mixer is designed to downconvert radio frequencies (RF) primarily between 1200 MHz and 2500 MHz to lower intermediate frequencies (IF) between 30 MHz and 450 MHz.



NOTES
1. ALL PINS AND CONNECTIONS TO ADL5356, AD8376, AD9258 AND AD9417 NOT SHOWN. CONSULT PRODUCT DATA SHEETS FOR DETAILED INFORMATION.

08713-001

Figure 1. Broadband Dual Channel IF Sampling Receiver (Simplified Schematic: Only One-Half of the Receiver Is Shown. All Connections and Decoupling Not Shown)

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The RF and LO input ports are already ac-coupled to prevent nonzero dc voltages from damaging the RF balun or LO input circuits, which are part of the ADL5356. The ADL5356 is configured for single-ended LO operation with a recommended LO drive of 0 dBm. With the LOSW pin of the mixer grounded, only one of the two LO channels (LOI2) is used in this circuit.

The mixer differential IF interface requires pull-up choke inductors to bias the open-collector outputs and to set the output impedance match. The shunting impedance of the choke inductors used to couple dc current into the IF amplifier should be selected to provide the desired output return loss. The real part of the mixer output impedance is approximately 200 Ω, which matches many commonly used SAW filters without the need for a transformer.

The receiver channel filtering is mainly performed by a 153.6 MHz, 20 MHz bandwidth Epcos model B5206 SAW filter which follows the mixer. The typical insertion loss (IL) of this filter is about 9 dB. The natural matched impedance of this SAW filter is 100 Ω differential. A simple L-C reactive network matches the SAW filter to the mixer 200 Ω differential output and the AD8376 VGA 150 Ω differential input impedance.

Table 1 highlights the cascaded performance of the dual mixer plus SAW filter. Note that IP3 is the third-order intercept point; IP1dB is the input referred −1 dB compression point; and NF is the noise figure.

A receiver gain control of 24 dB is provided by the AD8376 dual, high output linearity VGA that is optimized for ADC interfacing. Two independent 5-bit binary codes change each attenuator setting in 1 dB steps such that the gain of each amplifier can be set from +20 dB to −4 dB. The output third order intercept point (IP3) and noise floor essentially remain constant across the 24 dB available gain range. This is a valuable feature in a variable gain receiver where it is desirable to maintain a constant instantaneous dynamic range as the receiver gain is modified. The output IP3 of the AD8376 and the subsequent antialiasing filter is in excess of 50 dBm with a 2 V p-p composite signal.

The AD8376 provides a 150 Ω input impedance and is tuned to drive a 150 Ω load impedance. The open-collector output structure requires dc bias through an external bias network. A set of 1 µH choke inductors are used on each channel output to provide bias to the open-collector output pins. An optimized differential fourth order band-pass antialiasing filter is implemented at the DGA outputs before analog-to-digital conversion. Note that the antialiasing filter is terminated with shunt input and output resistances of about 300 Ω. The shunt resistances at either end of the filter, 309 Ω at the input and 330 Ω (through two 165 Ω bias setting resistors) at the output, combine to present the AD8376 with a nominal 150 Ω load impedance.

The band-pass antialiasing attenuates the output noise of the AD8376 outside of the intended Nyquist zone. In general, the SNR improves several dB by including a reasonable order antialiasing filter. The antialiasing filter is comprised of a fourth order Butterworth filter with a resonant tank circuit. The resonant tank helps ensure that the ADC input looks like a real resistance at the target center frequency by resonating out the capacitive portion of the ADC load (see AN-742 and AN-827 application notes). In addition, the ac-coupling capacitors and the bias chokes introduce additional zeros into the transfer function. The overall frequency response takes on a band-pass characteristic, helping to reject noise outside of the intended Nyquist zone. The filter provides a 20 MHz pass band centered at 153.6 MHz with 0.3 dB flatness and an insertion loss of about 3 dB.

The ADC utilized is the 14-bit AD9258, which samples at rates up to 125 MSPS. The AD9258's analog inputs are driven by the AD8376 through the band-pass antialiasing filter. The ADC sampling rate is set to 122.88 MSPS with a full-scale input range of 2 V p-p. The AD9258 differential clock signal is provided by the AD9517-4, a clock generation IC with on-chip VCO. The LVPECL level output, OUT0, is used for low jitter. The AD9517-4 uses its internal VCO frequency of 1474.56 MHz to derive the 122.88 MHz output clock to the ADC. A loop filter, designed with the ADISimCLK™ simulation software, provides a 60 kHz cutoff frequency and 50° of phase margin, giving timing jitter of about 160 fs rms. This jitter corresponds to a theoretical SNR of 76 dB, assuming a 153.6 MHz input, using the formula SNR = $20 \log(1/2\pi \times f_{IN} \times t_j)$.

Using this circuit, exceptional SFDR performance of 79.61 dBc at 153.6 MHz is achieved at maximum gain, as shown in Figure 2.

Table 1. Cascaded performance of the dual mixer plus SAW filter (RF =1950 MHz, LO = 1796.4 MHz, IF = 153.6 MHz, RF power = −10 dBm, LO power = 0 dBm)

	Gain (dB)	IP3 (dBm)	IP1dB (dBm)	NF (dB)
ADL5356	8.2	30.0	11.5	9.7
ADL5356 + SAW	−0.3	28.6	11.7	10.9

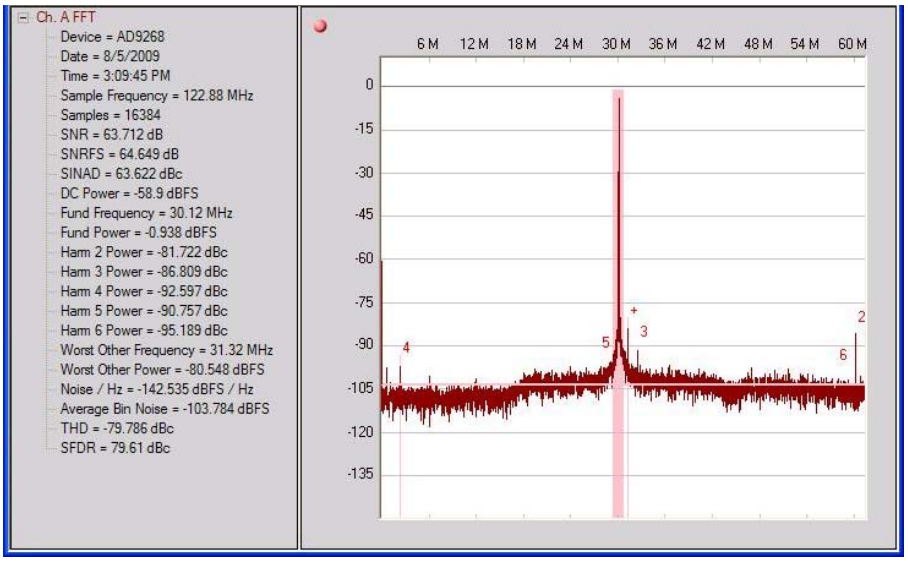

Figure 2. Measured Single-Tone Performance of the Circuit in Figure 1 for a 1950 MHz RF Input Signal. Sampling Frequency = 122.88 MSPS, IF Input = 153.6 MHz

COMMON VARIATIONS

Front-end LNAs and attenuators are not included in this circuit but can easily be interfaced to the 50 Ω single-ended RF inputs of the ADL5356 mixer. For a complete receiver design, ADL5521/ADL5523 LNAs may be incorporated.

The standard configuration using the ADL5356 allows reception of RF signals from 1.2 GHz to 2.4 GHz, but it is possible to use the ADL5358 mixer, which covers RF input frequencies from 500 MHz to 1700 MHz.

An Epcos (www.epcos.com) SAW filter follows the mixer and provides the necessary channel selectivity over a bandwidth ranging from 20 MHz to 40 MHz, depending on the chosen filter. The circuit shown uses a 20 MHz bandwidth, 153.6 MHz centered SAW filter (part number: B5206) but can also accommodate other pin-compatible filters.

Some empirical optimization may be needed to help compensate for actual PCB parasitics in SAW filter matching and antialias filter implementation. Details of designing the interstage filters can be found in the AN-742 and AN-827 application notes.

To ensure repeatability of band response, 1% capacitors are recommended for the SAW filter matching components and the antialiasing filter. In addition, Coilcraft 0603CS or similar inductors are recommended. Other resistors, capacitors, and inductors can be 10% values.

Excellent layout, grounding, and decoupling techniques must be utilized in order to achieve the desired performance from the circuits discussed in this note. As a minimum, a 4-layer PCB should be used with one ground plane layer, one power plane layer, and two signal layers.

All IC power pins must be decoupled to the ground plane with low inductance multilayer ceramic capacitors (MLCC) of 0.01 µF to 0.1 µF (for simplicity, not shown in the diagrams). Follow the recommendations on the individual data sheets and in Tutorial MT-101.

The product evaluation boards should be consulted for recommended layout and critical component placement. These can be accessed through the product pages for the devices.

Even though the AD8376 and AD9258 (or other ADC) may be powered from different supplies, sequencing is not an issue because the input signal to the ADC is ac-coupled.

The individual data sheet for the ADC should be consulted regarding the proper sequencing of the AVDD and the DVDD power supplies (if separate supplies are used).

LEARN MORE

AN-742 Application Note. *Frequency Domain Response of Switched Capacitor ADCs*. Analog Devices.

AN-827 Application Note. *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*. Analog Devices.

CN-0002 Circuit Note, *Using the AD8376 VGA to Drive Wide Bandwidth ADCs for High IF AC-Coupled Applications*, Analog Devices.

CN-0046 Circuit Note, *An Ultra Low Distortion Differential RF/IF Front-End for High Speed ADCs*, Analog Devices.

Kester, Walt. *High Speed System Applications*, Chapter 2 "Optimizing Data Converter Interfaces," Analog Devices, 2006.

MT-007 Tutorial, *Aperture Time, Aperture Jitter, Aperture Delay Time—Removing the Confusion*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-073 Tutorial, *High Speed Variable Gain Amplifiers (VGAs)*, Analog Devices.

MT-075 Tutorial, *Differential Drivers for High Speed ADCs Overview*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD8376 Data Sheet

AD9258 Data Sheet

AD9258 Evaluation Board

AD9517-4 Data Sheet

AD9517-4 Evaluation Board

ADL5356 Data Sheet

ADL5356 Evaluation Board

REVISION HISTORY

1/10—Revision 0: Initial Version

Circuits from the Lab™

Circuits from the Lab™ tested circuit designs address common design challenges and are engineered for quick and easy system integration. For more information and/or support, visit www.analog.com/CN0155.

Devices Connected/Referenced	
AD7195	4.8 kHz, Ultralow Noise, 24-Bit Σ-Δ ADC with PGA and AC Excitation
ADP3303	5 V Low Dropout Linear Regulator
ADP3303	3.3 V Low Dropout Linear Regulator

Precision Weigh Scale Design Using a 24-Bit Sigma-Delta ADC with Internal PGA and AC Excitation

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

AD7195 Evaluation Board (EVAL-AD7195EBZ)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

This circuit is an ac excited weigh scale system that uses the AD7195, an ultralow noise, low drift, 24-bit Σ-Δ ADC with internal PGA and drivers to implement ac excitation of the load cell.

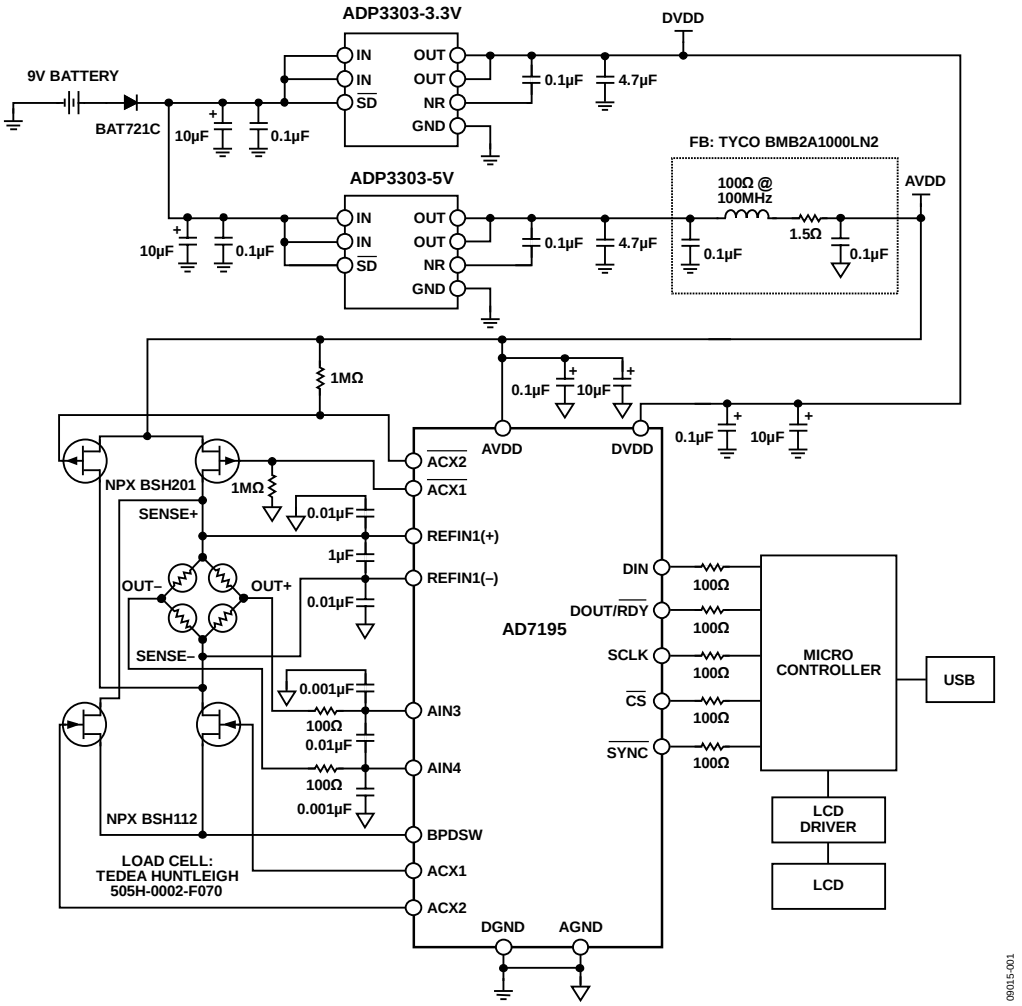

Figure 1. Weigh Scale System Using the AD7195 with AC Excitation (Simplified Schematic: All Connections Not Shown)

Rev. A

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The AD7195 simplifies the weigh scale design in low offset systems because most of the system building blocks are included on the chip. The AD7195 maintains good performance over the complete output data rate range, from 4.7 Hz to 4.8 kHz, which allows it to be used in weigh scale systems that operate at low speeds along with higher speed weigh scale systems.

CIRCUIT DESCRIPTION

With ac excitation, the polarity of the excitation voltage to the load cell is switched using external MOSFETs. Consecutive values are then averaged, which removes dc induced offsets. The AD7195 contains the internal logic to control the switching of the external MOSFETs. The driver signals from the AD7195 are precisely timed and nonoverlapping, which ensures that no short circuit occurs when switching the polarity of the bridge drive voltage. Pull-up and pull-down 1 MΩ resistors are connected to $\overline{ACX2}$ and ACX2 to prevent short-circuiting during power-up.

The AD7195 provides an integrated solution for ac excited load cells. The AD7195 can accept an inverted reference voltage, which is required when the excitation voltage to the load cell is inverted. The AD7195 synchronizes the ac excitation with the conversions and performs the averaging. Only a few external components are required. Along with the MOSFET transistors, the only other external components required are some filters on the analog inputs and capacitors on the reference pins for EMC purposes.

The low level signal from the load cell is amplified by the AD7195 internal PGA. The PGA is programmed to operate with a gain of 128. The conversions from the AD7195 are then sent to the PC via the USB connector. Using LabView™ software, the conversions are converted to weight and displayed.

Figure 2 shows the actual test setup. A 6-wire load cell is used because this gives the optimum system performance. A 6-wire load cell has two sense pins in addition to the excitation, ground, and two output connections. The sense pins are connected to the high side and low side of the Wheatstone bridge. The voltage developed across the bridge can, therefore, be accurately measured regardless of the voltage drop due to the wiring resistance. In addition, the AD7195 has differential analog inputs, and it accepts a differential reference. Connection of the load cell differential SENSE lines to the AD7195 reference inputs creates a ratiometric configuration that is immune to low frequency changes in the power supply excitation voltage. In addition, it eliminates the need for a precision reference. With a 4-wire load cell, the sense pins are not present, and the ADC reference pins are connected to the excitation pins EXC+ and EXC−.

Figure 2. Weigh Scale System Setup Using the AD7195

With this arrangement, the system is not completely ratiometric because there is a voltage drop between the EXC+/EXC− pins and the SENSE+/SENSE− due to wiring resistance.

The AD7195 has separate analog and digital power supply pins. The analog section must be powered from 5 V. The digital power supply is independent of the analog power supply and can be any voltage between 2.7 V and 5.25 V.

The microcontroller uses a 3.3 V power supply. Therefore, DVDD is also powered from 3.3 V. This simplifies the interface between the ADC and microcontroller because no external level shifting is required.

There are several methods to power the weigh scale system. It can be powered from the main power supply bus or battery powered (as shown in Figure 1). A 5 V low noise regulator is used to ensure that the AD7195 and the load cell receive a low noise supply. The ADP3303 (5 V) is used to generate the 5 V supply and is a low noise regulator. The filter network shown inside the dotted box ensures a low noise AVDD for the system. In addition, noise reduction capacitors are placed on the regulator output as recommended in the ADP3303 (5 V) data sheet. To optimize the EMC performance, the regulator output is filtered ahead of the AD7195 and the load cell. The 3.3 V digital supply is generated using the ADP3303 (3.3 V). It is essential that low noise regulators be used to generate all the power supply voltages to the AD7195 and the load cell because any noise on the power supply or ground planes introduces noise into the system and degrades the circuit performance.

If a 2 kg load cell with a sensitivity of 2 mV/V is used, the full-scale signal from the load cell is 10 mV when the excitation voltage is 5 V. A load cell has an offset, or TARE, associated with it. The noise of the system is calculated by the software to be 10 nV rms and 51 nV peak-to-peak. This equates to 196,000

noise-free counts, or 17.5 bits of noise-free code resolution (calculated from the measured peak-to-peak noise). The TARE can have a magnitude that is up to 50% of the load cell full-scale output signal. The load cell also has a gain error that can be up to ±20% of full scale. Some customers use a DAC to remove or null the TARE. When the AD7195 uses a 5 V reference, its analog input range is equal to ±40 mV when the gain is set to 128 and the part is configured for bipolar operation. The wide analog input range of the AD7195 relative to the load cell full-scale signal (10 mV) is beneficial because it ensures that the offset and gain error of the load cell do not overload the ADC's front end.

The AD7195 has an rms noise of 6 nV and a peak-to-peak noise of 40 nV when the first filter notch is programmed to 4.7 Hz. This corresponds to an output data rate of 1.17 Hz when ac excitation is used (sinc^4 filter selected). The number of noise-free counts is equal to

$$\frac{10\text{ mV}}{40\text{ nV}} = 250{,}000 \quad (1)$$

The resolution in grams is, therefore, equal to

$$\frac{2\text{ kg}}{250{,}000} = 0.008\text{ g} \quad (2)$$

The noise free resolution is equal to

$$\log_2(250{,}000) = \frac{\log_{10}(250{,}000)}{\log_{10}(2)} = 17.9\text{ bits} \quad (3)$$

In practice, the load cell itself introduces some noise. Figure 3 shows the measured output performance when a 1 kg weight is placed on the load cell and 500 conversions are gathered.

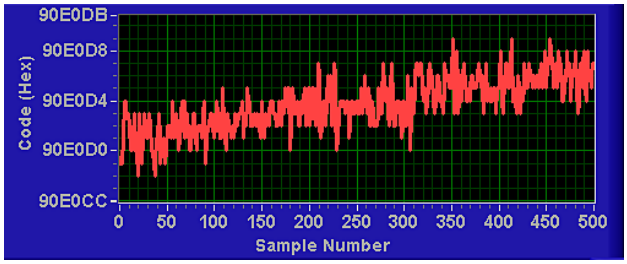

Figure 3. Measured Output Code for 500 Samples Showing the Effects of Noise

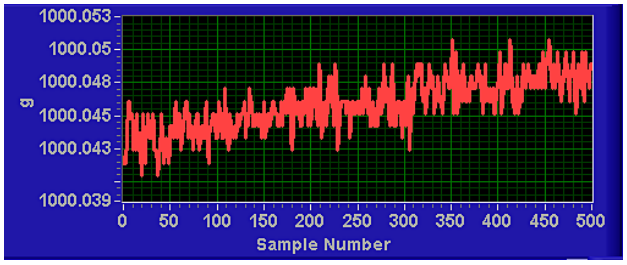

Figure 4. Measured Output in Grams for 500 Samples Showing the Effects of Noise

Figure 4 shows the performance in terms of weight. The peak-to-peak variation in output is 0.01 grams over the 500 codes. Therefore, the weigh scale system achieves an accuracy of 0.01 grams.

The plots show the actual (raw) conversions read back from the AD7195 when the load cell is attached. In practice, a digital post filter is used in a weigh scale system. The additional averaging that is performed in the post filter further improves the number of noise-free counts at the expense of a reduced output data rate.

As with any high accuracy circuit, proper layout, grounding, and decoupling techniques must be employed. See Tutorial MT-031, *Grounding Data Converters and Solving the Mystery of AGND and DGND,* and Tutorial MT-101, *Decoupling Techniques,* for more details.

A complete design support package for this circuit note can be found at http://www.analog.com/CN0155-DesignSupport.

COMMON VARIATIONS

Other weigh scale circuits, which do not require ac excitation, are described in the following Circuit Notes: CN-0102, CN-0107, CN-0108, CN-0118, and CN-0119.

CIRCUIT EVALUATION AND TEST

With the exception of the external load cell and the PC, the circuit shown in Figure 1 is contained on the AD7195 evaluation board (EVAL-AD7195-EBZ).

Interface to the evaluation board is via a standard USB connector, J1. J1 is used to connect the evaluation board to the USB port of a PC. A standard USB connector cable is included with the AD7195 evaluation board to allow the evaluation board to interface with the USB port of the PC. The AD7195 evaluation board can be powered using a 9 V battery, B1, or using an external 9 V dc source connected at J31. The 9 V is regulated down to 5 V using the on-board ADP3303-5, a high precision, low power 5 V output regulator. Using link J1, this regulated 5 V can be used as the supply to the AD7195.To use this option, link J1 should be placed in the 5 VBAT position.

Equipment Needed

The EVAL-AD7195-EBZ evaluation board and a PC running Windows® 2000, Windows XP, or Windows Vista (32-bit) are the only items required other than the external load cell. A Tedea Huntleigh 505H-0002-F070 load cell was used to obtain the results presented in this circuit note. The load cell is not shipped with the evaluation board and must be purchased from the manufacturer by the customer.

Getting Starting

The EVAL-AD7195-EBZ evaluation board is shipped with a CD containing software that can be installed onto a standard PC to control the AD7195. The software communicates with the AD7195 through the USB cable, which accompanies the board. The software allows conversion data to be read from the AD7195 and displayed or stored for later analysis.

The AD7195 evaluation board software should be installed using the supplied AD7195 evaluation board CD before connecting the board to the PC. Complete details can be found in the AD7195 evaluation board user guide (see the CN0155 Design Support Package: http://www.analog.com/CN0155-DesignSupport).

Functional Block

The evaluation board user guide shows the basic functional block diagram of the test setup (see the CN0155 Design Support Package: http://www.analog.com/CN0155-DesignSupport).

Setup and Test

Complete instructions for setup and testing of the AD7195 evaluation board can be found in AD7195 evaluation board user guide (see the CN0155 Design Support Package: http://www.analog.com/CN0155-DesignSupport).

After the software is installed, the AD7195 evaluation board should be configured for use with the external load cell by setting the appropriate links (jumpers) as described in theAD7195 evaluation board user guide (see the CN0155 Design Support Package: http://www.analog.com/CN0155-DesignSupport). Make sure the links are set before applying power to the evaluation board.

The load cell connects to the evaluation board header J4. Operation of the Weighscale Demo is described in the AD7195 evaluation board user guide (see the CN0155 Design Support Package: http://www.analog.com/CN0155-DesignSupport).

LEARN MORE

CN0155 Design Support Package: http://www.analog.com/CN0155-DesignSupport

Kester, Walt. 1999. *Sensor Signal Conditioning.* Sections 2, 3, 4. Analog Devices.

MT-004 Tutorial, *The Good, the Bad, and the Ugly Aspects of ADC Input Noise—Is No Noise Good Noise?* Analog Devices.

MT-022 Tutorial, *ADC Architectures III: Sigma-Delta ADC Basics,* Analog Devices.

MT-023 Tutorial, *ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND,"* Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

AD7195 Data Sheet

AD7195 Evaluation Board

ADP3303 Data Sheet

REVISION HISTORY

11/10—Rev. 0 to Rev. A

Changes to Circuit Note Title 1
Added Evaluation and Design Support Section 1
Changes to Circuit Function and Benefits Section 1
Changes to Circuit Description Section 2
Added Circuit Evaluation and Test Section 3
Changes to Learn More Section 4

7/10—Revision 0: Initial Version

Circuits from the Lab™ Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0185.

Devices Connected/Referenced	
AD7400A	Isolated Sigma-Delta Modulator
ADuM5000	Isolated DC-to-DC Converter
AD8646	Dual, 24 MHz, Rail-to-Rail, I/O Op Amp
ADP121	150 mA, Low Quiescent Current, CMOS Linear Regulator
ADP3301	High Accuracy, 100 mA, Low Dropout Linear Regulator
ADG849	3 V/5 V CMOS 0.5 Ω SPDT/2:1 Mux in SC70
ADR443	Ultralow Noise, LDO XFET® 3.0 V Voltage Reference

A Novel Analog-to-Analog Isolator Using an Isolated Sigma-Delta Modulator, Isolated DC-to-DC Converter, and Active Filter

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0185 Circuit Evaluation Board (EVAL-CN0185-EB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a complete low cost implementation of an analog-to-analog isolator. The circuit provides isolation of 2500 V rms (1 minute per UL 1577).

The circuit is based on the AD7400A, a second-order, sigma-delta (Σ-Δ) modulator with a digitally isolated 1-bit data stream output. The isolated analog signal is recovered with a fourth-order active filter based on the dual, low noise, rail-to-rail AD8646 op amp. With the ADuM5000 as the power supply for the isolated side, the two sides are completely isolated and use only one power supply for the system. The circuit has 0.05% linearity and benefits from the noise shaping provided by the modulator of the AD7400A and the analog filter. The applications of the circuit include motor control and shunt current monitoring, and the circuit is also a good alternative to isolation systems based on optoisolators.

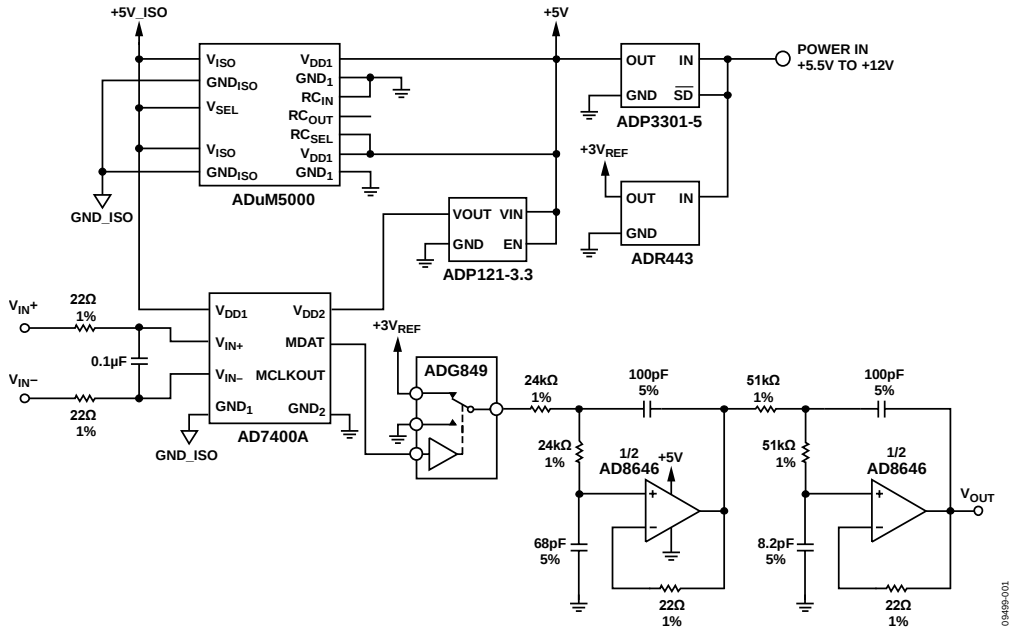

Figure 1. Analog Isolator Using AD7400A (Simplified Schematic: All Connections and Decoupling Not Shown

Rev. B

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CIRCUIT DESCRIPTION

A block diagram of the circuit is shown in Figure 1. The analog input is sampled at 10 MSPS by the AD7400A Σ-Δ modulator. The 22 Ω resistors and 0.1 µF capacitor form a differential input noise reduction filter with a cutoff frequency of 145 kHz. The output of the AD7400A is an isolated 1-bit data stream. The quantization noise is shaped by a second-order Σ-Δ modulator, which shifts the noise to the higher frequencies (see the MT-022 Tutorial).

To reconstruct the analog input signal, follow the data stream by an ADG849 switch connected to a 3 V ADR443 reference to stabilize the peak-to-peak output of the MDAT.

The signal is then filtered by an active filter whose order is higher than the order of the modulator. A fourth-order Chebyshev filter is used for better noise attenuation. Compared to other filter responses (Butterworth or Bessel), the response of the Chebyshev provides the steepest rolloff for a given filter order. The filter is implemented using the dual AD8646, a rail-to-rail, input and output, low noise, single-supply op amp.

The ADuM5000 is an isolated dc-to-dc converter based on Analog Devices, Inc., *i*Coupler® technology. It is used for the power supply to the isolated side of the circuit containing the AD7400A. The *iso*Power® technology of the ADuM5000 uses high frequency switching elements to transfer power through a chip-scale transformer.

The circuit must be constructed on a multilayer printed circuit board (PCB) with a large area ground plane. Proper layout, grounding, and decoupling techniques must be used to achieve optimum performance (see the *MT-031 Tutorial, Grounding Data Converters and Solving the Mystery of "AGND" and "DGND,"* the *MT-101 Tutorial, Decoupling Techniques*, and the ADuC7060/ ADuC7061 evaluation board layout). Ensure that the PCB layout meets the emissions standards and isolation requirements between the two isolated sides (see the AN-0971 Application Note).

In order not to overdrive the AD8646, the input signal must be lower than the power supply (5 V). The output of the AD7400A is a stream of 1s and 0s with an amplitude equal to the AD7400A V_{DD2} supply voltage. Therefore, the V_{DD2} digital supply is 3.3 V supplied by the ADP121 linear regulator. Alternatively, if a 5 V supply is used for V_{DD2}, attenuate the digital output signal before connecting to the active filter. In either case, well regulate the supply because the final analog output is directly proportional to V_{DD2}.

The 5 V supply for the circuit in Figure 1 is supplied from an ADP3301 5 V linear regulator, which accepts an input voltage of 5.5 V to 12 V.

Analog Active Filter Design

The cutoff frequency of the low-pass filter mostly depends on the desired bandwidth of the circuit. There is a trade-off between the cutoff frequency and noise performance, and there is more noise if the cutoff frequency of the filter increases. This is especially true in this design because the Σ-Δ modulator shapes the noise and moves a large portion into the higher frequencies. The cutoff frequency in this design is 100 kHz.

For a given cutoff frequency, the smaller the transition band of the filter is, the smaller the noise is that passes through the filter. Of all the filter responses (Butterworth, Chebyshev, Bessel, and so on), the Chebyshev filter was chosen for this design because it has a smaller transition band for a given filter order. However, this smaller transition band comes at the expense of a slightly worse transient response.

The fourth-order filter is made up of two second-order filters, with a Sallen-Key structure. The Analog Filter Wizard and the NI Multisim were used to design the filter. The parameters used include the following:

- Filter type = low-pass, Chebyshev, 0.01 dB ripple
- Order = 4
- f_C = 100 kHz, Sallen-Key (updated format for clarity)

The recommended values generated by the program were used with the exception of the feedback resistors, which were reduced to 22 Ω.

Measurements

The circuit has a gain of 4.6875 and an output offset voltage of 1.5 V. A differential signal of 0 V results in a digital bit stream of 1s and 0s, where each occurs 50% of the time. The ADR443 output is 3.0 V; therefore, after filtering, there is a 1.5 V dc offset. A differential input of 320 mV ideally results in a stream of all 1s, which after filtering, yields a 3.0 V DC output. Therefore, the effective gain of the circuit is

$$GAIN = (3.0 - 1.5)/0.32 = 4.6875$$

From the measurements, the actual measured offset is 1.504V , and the gain is 4.69. The dc transfer function of the system is shown in Figure 2. Linearity was measured as 0.0465%.

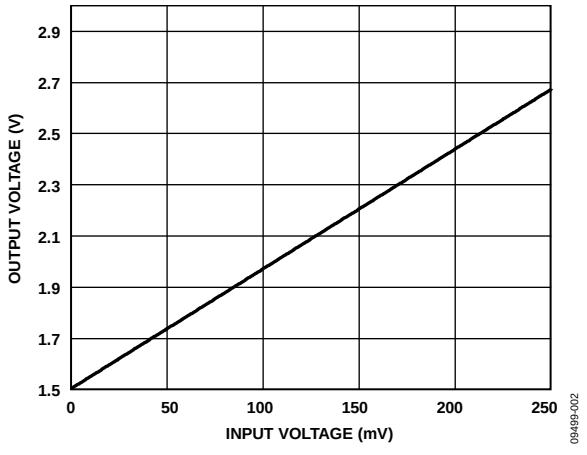

Figure 2. System DC Transfer Function

Figure 3 shows the output voltage with no dc offset voltage vs. the input frequency. The input signal voltage is 40 mV p-p, which causes an output signal of 40 × 4.6875= 190 mV p-p. Note that there is approximately 10 mV of peaking in the frequency response function, corresponding to about 0.42 dB.

The system has good noise performance, with a noise density of 2.50 µV/√Hz at 1 kHz and 1.52 µV/√Hz at 10 kHz.

A complete design support package for this circuit note can be found at www.analog.com/CN0185-DesignSupport.

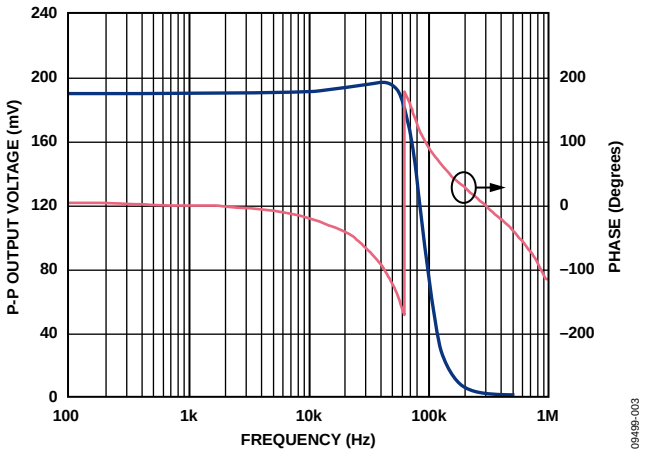

Figure 3. Frequency and Phase Response of the Circuit for a 40 mV Peak-to-Peak Input Signal

COMMON VARIATIONS

The circuit can be used for isolated voltage monitoring and for current sensing applications where the voltage across a shunt resistor is monitored. The requirements of the input signal for the system are detailed in the AD7400A data sheet.

If the ADuM6000 is used instead of the ADuM5000, the entire circuit is rated to 5 kV.

The ADP1720 or ADP7102 linear regulator can be used as a substitute for the ADP3301, if desired.

CIRCUIT EVALUATION AND TEST

The circuit can be easily evaluated using a signal generator and an oscilloscope after powering on the circuit with a 6 V power supply.

Equipment Needed (Equivalents Can Be Substituted)

The following equipment is needed:

- A multifunction calibrator (dc source), Fluke 5700A
- A digital multimeter, Agilent 3458A, 8.5 digits
- A spectrum analyzer, Agilent 4396B
- A function generator, Agilent 33250A
- A power supply, 6 V

Setup and Test

The block diagram of the linearity measurement setup is shown in Figure 4. Connect the 6 V power supply to the EVAL-CN0185-EB1Z power terminal.

The dc input voltage is generated with the Fluke 5700A, and the Agilent 3458A DVM is used to measure the output. The dc output from the Fluke 5700A is stepped, and the data recorded with a 1 mV increase from 1 mV to 250 mV.

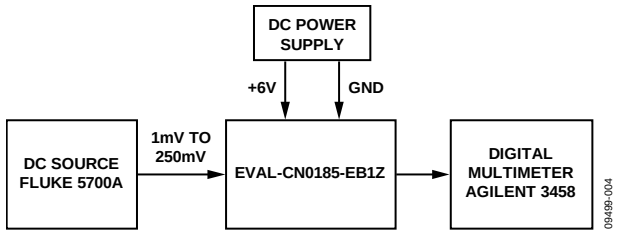

Figure 4. Test Setup for Measuring Linearity

To measure the frequency response, connect the equipment as shown in Figure 5. Set the 33250A function generator for a 40 mV peak-to-peak sine-wave output with a 0 dc offset. Then, sweep the frequency of the signal from 100 Hz to 500 kHz and record the data using the Agilent 4396B spectrum analyzer.

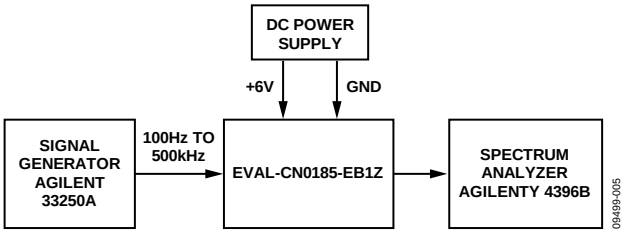

Figure 5. Test Setup for Measuring Frequency Response

LEARN MORE

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Data Sheets and Evaluation Boards

AD7400A Data Sheet

AD7400A Evaluation Board

ADuM5000 Data Sheet

ADuM5000 Evaluation Board

AD8646 Data Sheet

ADP121 Data Sheet

ADP3301 Data Sheet

ADG849 Data Sheet

ADR443 Data Sheet

REVISION HISTORY

9/13—Rev. A to Rev. B

Added ADR443.....Throughrout
Changes to Devices Connected/Referenced Section and Figure 1 1
Changes to Circuit Description Section, Measurements Section, and Figure 2.....2
Changes to Figure 3.....3
Change to Data Sheets and Evaluation Boards Section 4

4/13—Rev. 0 to Rev. A

Changes to Figure 1.....1
Changes to Figure 3 and Common Variations Section 3

4/11—Revision 0: Initial Version

Circuits from the Lab™ Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0187.

Devices Connected/Referenced	
ADL5502	450 MHz to 6 GHz Crest Factor Detector
AD7266	Differential/Single-Ended Input, Dual, Simultaneous Sampling, 2 MSPS, 12-Bit, 3-Channel SAR Analog-to-Digital Converter
ADA4891-4	Low Cost, Quad, CMOS, High Speed, Rail-to-Rail Amplifier
ADP121	150 mA, Low Quiescent Current, CMOS Linear Regulator in 5-Lead TSOT or 4-Ball WLCSP

Crest Factor, Peak, and RMS RF Power Measurement Circuit Optimized for High Speed, Low Power, and Single 3.3 V Supply

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0187 Circuit Evaluation Board (EVAL-CN0187-SDPZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 measures peak and rms power at any RF frequency from 450 MHz to 6 GHz over a range of approximately 45 dB. The measurement results are converted to differential signals in order to eliminate noise and are provided as digital codes at the output of a 12-bit SAR ADC with serial interface and integrated reference. A simple two-point calibration is performed in the digital domain.

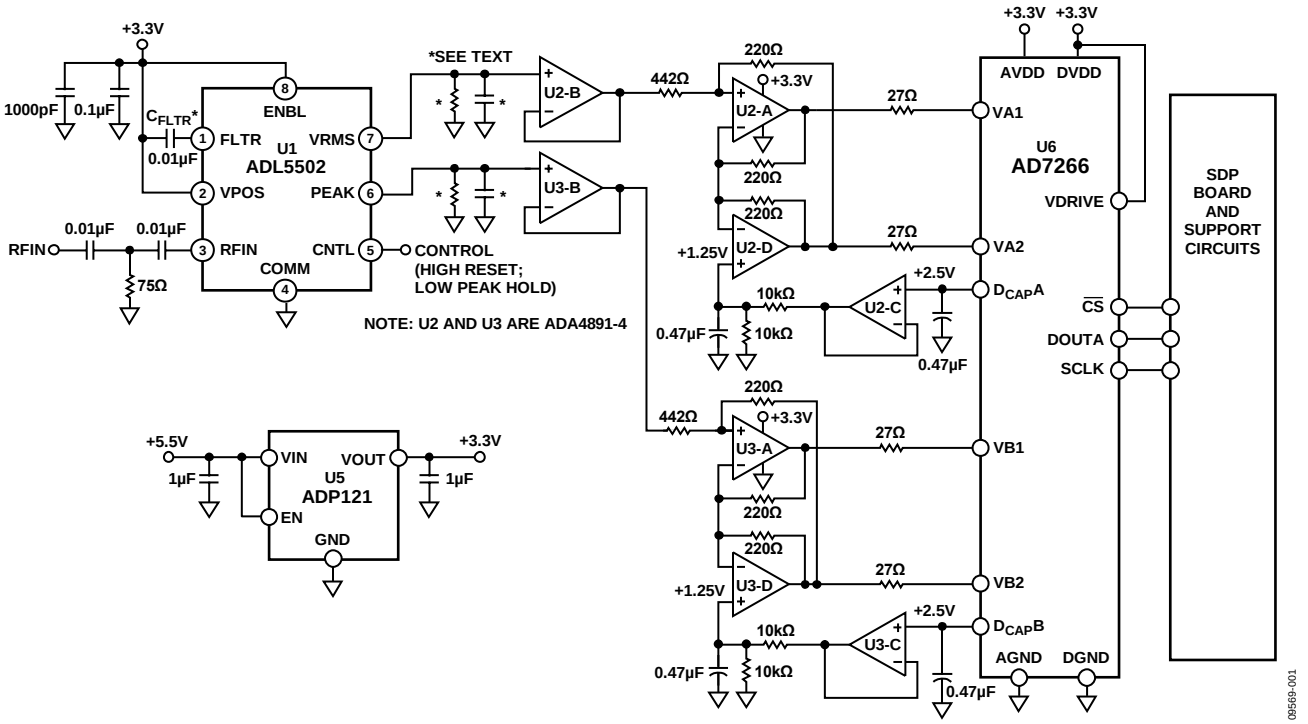

Figure 1. High Speed, Low Power, Crest Factor, Peak, and RMS Power Measurement System (Simplified Schematic: All connections and Decoupling Not Shown)

Rev.0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

The ADL5502 is a mean-responding (true rms) power detector in combination with an envelope detector to accurately determine the crest factor (CF) of a modulated signal. It can be used in high frequency receiver and transmitter signal chains from 450 MHz to 6 GHz with envelope bandwidths over 10 MHz. The peak-hold function allows the capture of short peaks in the envelope with lower sampling rate ADCs. Total current consumption is only 3 mA @ 3 V.

The ADA4891-4 is a high speed, quad, CMOS amplifier that offers high performance at a low cost. Current consumption is only 4.4 mA/amplifier at 3 V. The amplifier features true single-supply capability, with an input voltage range that extends 300 mV below the negative rail. The rail-to-rail output stage enables the output to swing to within 50 mV of each rail, ensuring maximum dynamic range. Low distortion and fast settling time makes it ideal for this application.

The AD7266 is a dual, 12-bit, high speed, low power, successive approximation ADC that operates from a single 2.7 V to 5.25 V power supply and features sampling rates up to 2 MSPS. The device contains two ADCs, each preceded by a 3-channel multiplexer, and a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 30 MHz. Current consumption is only 3 mA at 3 V. It also contains an internal 2.5 V reference.

The circuit operates on a single +3.3 V supply from the ADP121, a low quiescent current, low dropout, linear regulator that operates from 2.3 V to 5.5 V and provides up to 150 mA of output current. The low 135 mV dropout voltage at 150 mA load improves efficiency and allows operation over a wide input voltage range. The low 30 µA of quiescent current at full load makes the ADP121 ideal for battery-operated portable equipment.

The ADP121 is available in output voltages ranging from 1.2 V to 3.3 V. The parts are optimized for stable operation with small 1 µF ceramic output capacitors. The ADP121 delivers good transient performance with minimal board area.

Short-circuit protection and thermal overload protection circuits prevent damage in adverse conditions. The ADP121 is available in tiny 5-lead TSOT and 4-ball, 0.4 mm pitch halide-free WLCSP packages and utilizes the smallest footprint solution to meet a variety of portable applications.

CIRCUIT DESCRIPTION

The RF signal being measured is applied to the ADL5502. A single 75 Ω termination resistor at the RF input in parallel with the input impedance of the ADL5502 provides a broadband match of 50 Ω. More precise resistive or reactive matches can be applied for narrow frequency band use (see the RF Input Interfacing section of the ADL5502 data sheet).

The internal filter capacitor of the ADL5502 provides averaging in the square domain but leaves some residual ac on the output. Signals with high peak-to-average ratios, such as W-CDMA or CDMA2000, can produce ac residual levels on the ADL5502 VRMS dc output. To reduce the effects of these low frequency components in the waveforms, some additional filtering is required. The internal square-domain filter capacitance of the ADL5502 can be augmented by connecting a C_{FLTR} capacitor between Pin 1 (FLTR) and Pin 2 (VPOS). The ac residual can be reduced further by adding capacitance to the VRMS output. The combination of the internal 100 Ω output resistance and the added output capacitance produces a low-pass filter to reduce output ripple of the VRMS output (see the Selecting the Square-Domain Filter and Output Low-Pass Filter section of the ADL5502 data sheet for more details).

To measure the peak of a waveform, the control line (CNTL) must be temporally set to a logic high (reset mode for >1 µs) and then set back to a logic low (peak-hold mode). This allows the ADL5502 to be initialized to a known state. When setting the device to measure peak, peak-hold mode should be toggled for a period in which the input rms power and crest factor (CF) is not likely to change.

If the ADL5502 is in peak-hold mode and the CF changes from high to low or the input power changes from high to low, a faulty peak measurement is reported. The ADL5502 simply keeps reporting the highest peak that occurred when the peak-hold mode was activated and the input power or the CF was high. Unless CNTL is reset, the PEAK output does not reflect the new peak in the signal.

The ADL5502 is capable of sourcing a VRMS output current of approximately 3 mA. The output current is sourced through the on-chip, 100 Ω series resistor; therefore, any load resistor forms a voltage divider with this on-chip resistance. It is recommended that the ADL5502 VRMS output drive high resistive loads to preserve output swing. If an application requires driving a low resistance load (as well as in cases where increasing the nominal conversion gain is desired), a buffering circuit is necessary.

The PEAK output is designed to drive 2 pF loads. It is recommended that the ADL5502 PEAK output drive low capacitive loads to achieve a full output response time. The effects of larger capacitive loads are particularly visible when tracking envelopes during the falling transitions. When the envelope is in a fall transition, the load capacitor discharges through the on-chip load resistance of 1.9 kΩ. If the larger capacitive load is unavoidable, the additional capacitance can be counteracted by putting a shunt resistor to ground on the PEAK output to allow for fast discharge. Such a shunt resistor also makes the ADL5502 run higher current, and it should not be lower than 500 Ω.

Typical measured performance characteristics of the circuit are presented in Figure 2 through Figure 5.

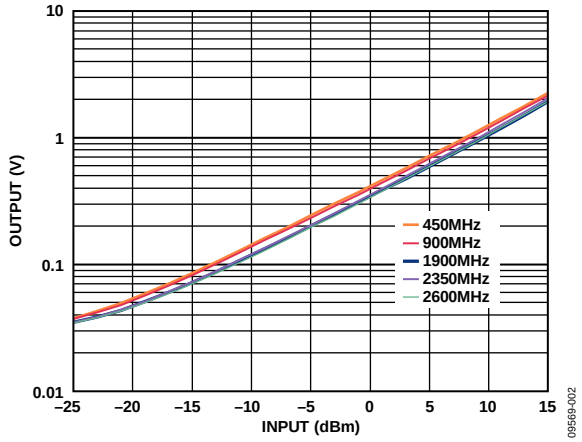

Figure 2. Measured VRMS Output vs. Input Level (Log Scale), 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2600 MHz, Supply +3.3 V

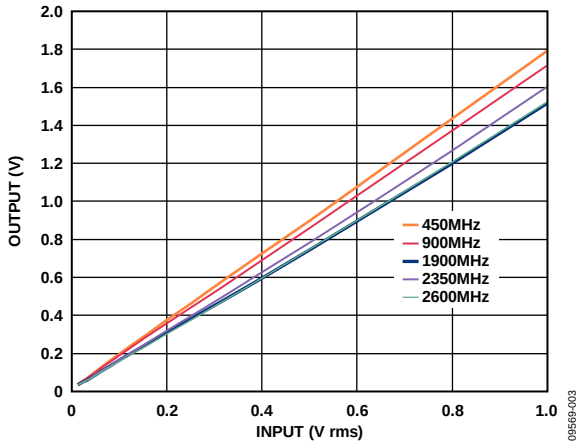

Figure 3. Measured VRMS Output vs. Input Level (Linear Scale), 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2600 MHz, Supply +3.3 V

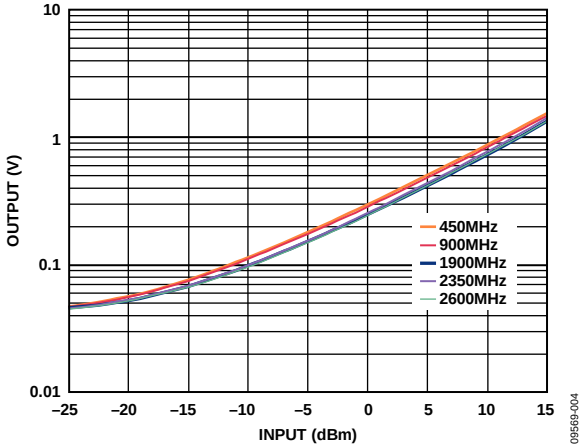

Figure 4. Measured PEAK Output vs. Input Level (Log Scale), 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2600 MHz, Supply +3.3 V

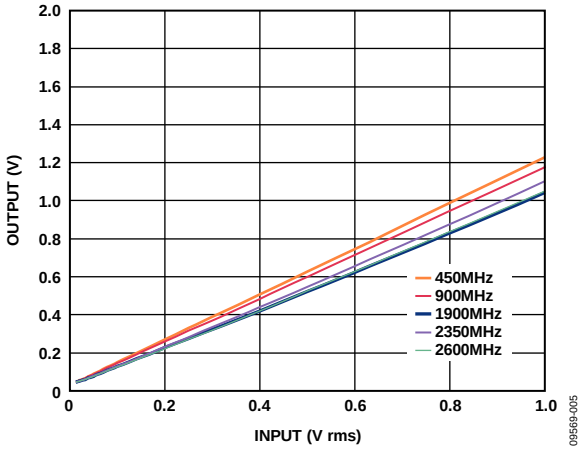

Figure 5. Measured PEAK Output vs. Input Level (Linear Scale), 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2600 MHz, Supply +3.3 V

The turn-on time and pulse response is strongly influenced by the size of the square-domain filter (C_{FLTR}) and output shunt capacitor connected to the VRMS output. Figure 6 (taken from the ADL5502 data sheet) shows a plot of the output response to an RF pulse on the RFIN pin, with a 0.1 µF output filter capacitor and no square-domain filter capacitor (C_{FLTR}). The falling edge is particularly dependent on the output shunt capacitance.

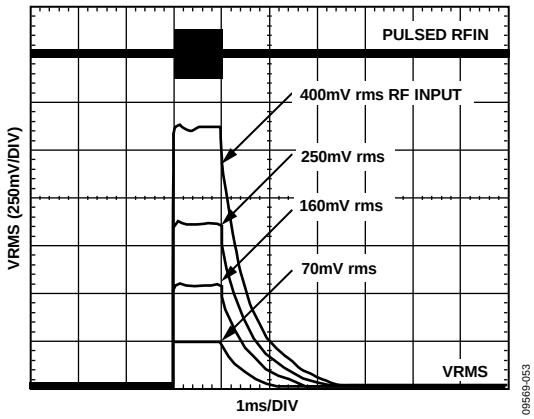

Figure 6. Output Response to Various RF Input Pulse Levels, Supply3 V, 900 MHz Frequency, Square-Domain Filter Open, Output Filter 0.1 µF

To improve the falling edge of the enable and pulse responses, a resistor can be placed in parallel with the output shunt capacitor. The added resistance helps to discharge the output filter capacitor. Although this method reduces the power-off time, the added load resistor also attenuates the output (see the Output Drive Capability and Buffering section of the ADL5502 data sheet). Figure 7 (taken from the ADL5502 data sheet) shows the improvement obtained by adding a parallel 1 kΩ resistor.

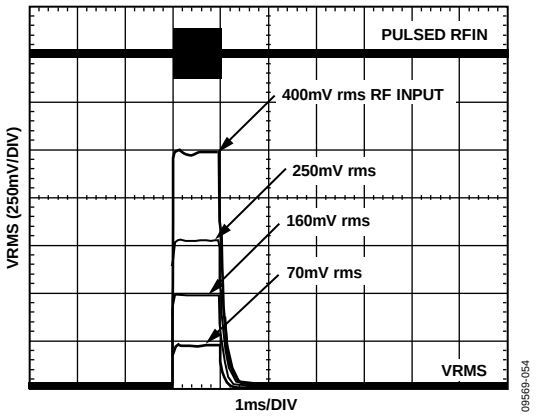

Figure 7. Output Response to Various RF Input Pulse Levels, Supply 3 V, 900 MHz Frequency, Square-Domain Filter Open, Output Filter 0.1 µF with Parallel 1 kΩ

The RMS and PEAK outputs of the ADL5502 pass through unity gain buffers that drive cross-coupled stages for converting the single-ended outputs to differential signals. The internal +2.5 V reference of the AD7266 (via the $D_{CAP}A$ and $D_{CAP}B$ pins) passes through another unity gain buffer and a voltage divider. This sets the common-mode voltage of the network to +1.25 V.

The AD7266 achieves simultaneous samples of the RMS and PEAK outputs and transfers the data within a 1 µs response time. The data is provided on a single serial data line. Because slope and intercept vary from device to device, board-level calibration must be performed to achieve high accuracy. In general, calibration is performed by applying two input power levels to the ADL5502 and measuring the corresponding output voltages. The calibration points are generally chosen to be within the linear operating range of the device. The best-fit line is characterized by calculating the conversion gain (or slope) and intercept using the following equations:

$$Gain = (V_{VRMS2} - V_{VRMS1})/(V_{IN2} - V_{IN1}) \quad (1)$$

$$Intercept = V_{VRMS1} - (Gain \times V_{IN1}) \quad (2)$$

where:

V_{IN} is the rms input voltage to RFIN.

V_{VRMS} is the voltage output at VRMS.

Once gain and intercept are calculated, an equation can be written that allows calculation of an (unknown) input power based on the measured output voltage.

$$V_{IN} = (V_{VRMS} - Intercept)/Gain \quad (3)$$

For an ideal (known) input power, the law conformance error of the measured data can be calculated as

$$ERROR\ (\text{dB}) = 20 \times \log\left(\frac{V_{VRMS,\ MEASURED} - Intercept}{Gain \times V_{IN,\ IDEAL}}\right) \quad (4)$$

Figure 8 and Figure 9 show plots of the VRMS and PEAK error at 25°C, the temperature at which the ADL5502 is calibrated. Note that the error is not zero; this is because the ADL5502 does not perfectly follow the ideal linear equation, even within its operating region. The error at the calibration points is, however, equal to zero by definition.

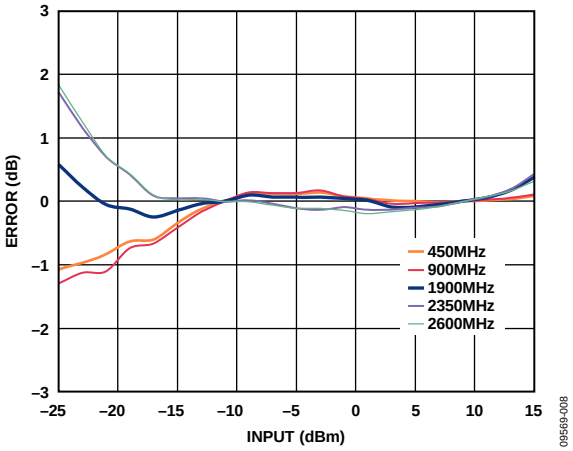

Figure 8. Measured VRMS Linearity Error vs. Input Level, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2600 MHz, Supply +3.3 V

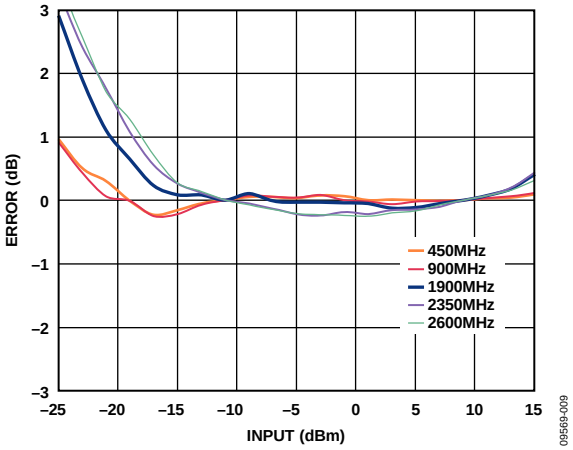

Figure 9. Measured PEAK Linearity Error vs. Input Level, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2600 MHz, Supply +3.3 V

When the characteristics (slope and intercept) of the VRMS and PEAK outputs are known, the calibration for the CF calculation is complete. A three-stage process must be taken to measure and calculate the crest factor of any waveform. First, the unknown signal must be applied to the RF input, and the corresponding VRMS level is measured. This level is indicated in Figure 10 as $V_{VRMS\text{-}UNKNOWN}$. The RF input, V_{IN}, is calculated using $V_{VRMS\text{-}UNKNOWN}$ and Equation 3.

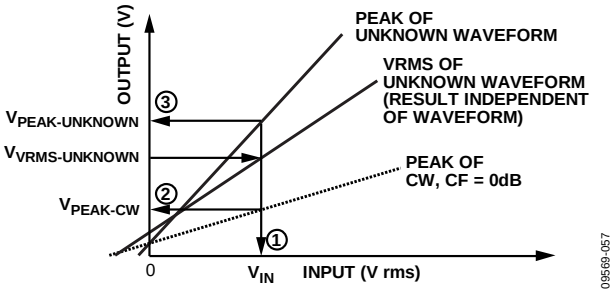

Figure 10. Procedure for Crest Factor Calculation

Next, the CW reference level of PEAK, $V_{PEAK-CW}$, is calculated using V_{IN} (that is, the output voltage that would be seen if the incoming waveform was a CW signal).

$$V_{PEAK-CW} = (V_{IN}\ Gain_{PEAK}) + Intercept_{PEAK} \quad (5)$$

Finally, the actual level of PEAK, $V_{PEAK-UNKNOWN}$, is measured and the CF can be calculated as

$$CF = 20\log_{10}(V_{PEAK-UNKNOWN}/V_{PEAK-CW}) \quad (6)$$

where $V_{PEAK-CW}$ is used as a reference point to compare $V_{PEAK-UNKNOWN}$. If both V_{PEAK} values are equal, then the CF is 0 dB, as shown in Figure 11 with the CW signal (taken from the ADL5502 data sheet). Across the dynamic range, the calculated CF hovers about the 0 dB line. Likewise, for complex waveforms of 3 dB, 6 dB, and 9 dB CFs, the calculations accurately hover about the corresponding CF levels.

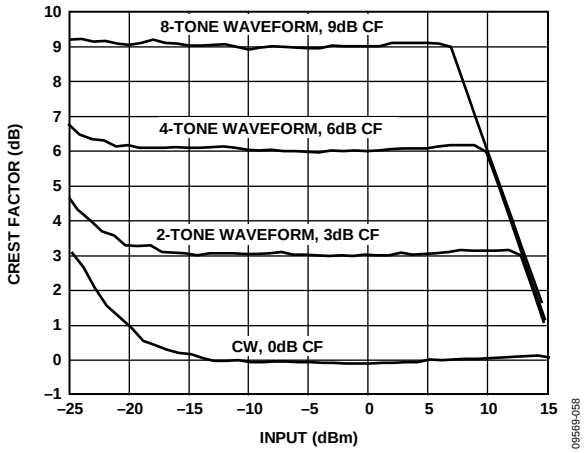

Figure 11. Reported Crest Factor of Various Waveforms

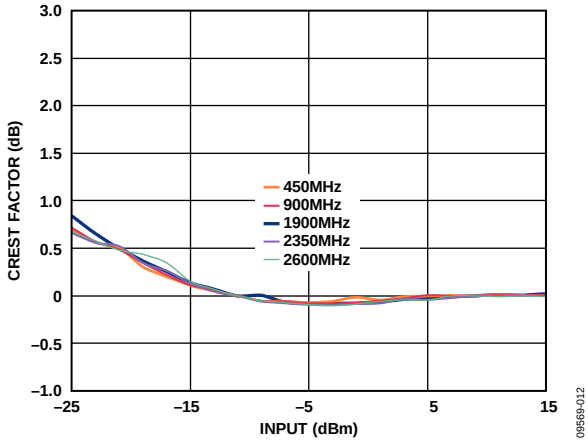

Figure 12. Measured Crest Factor of CW Signals vs. Input Level, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2600 MHz, Supply +3.3 V

The performance of this or any high speed circuit is highly dependent on proper PCB layout. This includes, but is not limited to, power supply bypassing, controlled impedance lines (where required), component placement, signal routing, and power and ground planes. (See MT-031 Tutorial, MT-101 Tutorial, and article, *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, for more detailed information regarding PCB layout.)

A complete design support package for this circuit note can be found at http://www.analog.com/CN0187-DesignSupport.

COMMON VARIATIONS

For applications that require less RF detection range, the AD8363 rms detector can be used. The AD8363 has a detection range of 50 dB and operates at frequencies up to 6 GHz. For non-rms detection applications, the AD8317/AD8318/AD8319 or ADL5513 can be used. These devices offer varying detection ranges and have varying input frequency ranges up to 10 GHz (see CN-0150 for more details).

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0187-SDPZ circuit board and the EVAL-SDP-CB1Z System Demonstration Platform (SDP) evaluation board. The two boards have 120-pin mating connectors, allowing for the quick setup and evaluation of the circuit's performance. The EVAL-CN0187-SDPZ board contains the circuit to be evaluated, as described in this note, and the SDP evaluation board is used with the CN0187 evaluation software to capture the data from the EVAL-CN0187-SDPZ circuit board.

Equipment Needed

- PC with a USB port and Windows® XP or Windows Vista® (32-bit), or Windows® 7 (32-bit)
- EVAL-CN0187-SDPZ circuit evaluation board
- EVAL-SDP-CB1Z SDP evaluation board
- CN0187 evaluation software
- Power supply: +6 V, or +6 V "wall wart"
- RF signal source
- Coaxial RF cable with SMA connectors

Getting Started

Load the evaluation software by placing the CN0187 Evaluation Software disc in the CD drive of the PC. Using "My Computer," locate the drive that contains the evaluation software disc and open the Readme file. Follow the instructions contained in the Readme file for installing and using the evaluation software.

Functional Block Diagram

See Figure 1 of this circuit note for the circuit block diagram, and the "EVAL-CN0187-SDPZ-SCH" pdf file for the circuit schematics. This file is contained in the CN0187 Design Support Package.

Setup

Connect the 120-pin connector on the EVAL-CN0187-SDPZ circuit board to the connector marked "CON A" on the EVAL-SDP-CB1Z evaluation (SDP) board. Nylon hardware should be used to firmly secure the two boards, using the holes provided at the ends of the 120-pin connectors. Using an appropriate RF cable, connect the RF signal source to the EVAL-CN0187-SDPZ board via the SMA RF input connector. With power to the supply off, connect a +6 V power supply to the pins marked "+6 V" and "GND" on the board. If available, a +6 V "wall wart" can be connected to the barrel jack connector on the board and used in place of the +6 V power supply. Connect the USB cable supplied with the SDP board to the USB port on the PC. Note: Do not connect the USB cable to the mini USB connector on the SDP board at this time.

Test

Apply power to the +6 V supply (or "wall wart") connected to EVAL-CN0187-SDPZ circuit board. Launch the evaluation software and connect the USB cable from the PC to the USB mini-connector on the SDP board. The software will be able to communicate to the SDP board if the Analog Devices System Development Platform driver is listed in the Device Manager.

Once USB communications are established, the SDP board can now be used to send, receive, and capture serial data from the EVAL-CN0187-SDPZ board.

The data in this circuit note were generated using a Rohde & Schwarz SMT-03 RF signal source and an Agilent E3631A power supply. The signal source was set to the frequencies indicated in the graphs, and the input power was stepped and data recorded in 1 dB increments.

Information and details regarding how to use the evaluation software for data capture can be found in the CN0187 Evaluation Software Readme file.

Information regarding the SDP board can be found in the SDP User Guide.

LEARN MORE

CN0187 Design Support Package:
http://www.analog.com/CN0187-DesignSupport

SDP User Guide

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, Analog Dialogue 39-09, September 2005.

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MT-077 Tutorial, *Log Amp Basics*, Analog Devices.

MT-078 Tutorial, *High Speed Log Amps*, Analog Devices.

MT-081 Tutorial, *RMS-to-DC Converters*, Analog Devices.

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Data Sheets and Evaluation Boards

CN-0187 Circuit Evaluation Board (EVAL-CN0187-SDPZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

ADL5502 Data Sheet

ADL5502 Evaluation Board

AD7266 Data Sheet

AD7266 Evaluation Board

ADA4891 Data Sheet

REVISION HISTORY

4/11—Revision 0: Initial Version

Circuits from the Lab™ Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0216.

Devices Connected/Referenced	
AD7791	Low Power, Buffered, 24-Bit Sigma-Delta ADC
ADA4528-1	Precision, Ultralow Noise, Rail-to-Rail Input/Output, Zero-Drift Op Amp
ADP3301	High Accuracy anyCAP® 100 mA Low Dropout Linear Regulator

Precision Weigh Scale Design Using the AD7791 24-Bit Sigma-Delta ADC with External ADA4528-1 Zero-Drift Amplifiers

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0216 Circuit Evaluation Board (EVAL-CN0216-SDPZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit in Figure 1 is a precision weigh scale signal conditioning system. It uses the AD7791, a low power buffered 24-bit sigma-delta ADC along with two external ADA4528-1 zero-drift amplifiers. This solution allows for high dc gain with a single supply.

Ultralow noise, low offset voltage, and low drift amplifiers are used at the front end for amplification of the low-level signal from the load cell. The circuit yields 15.3 bit noise-free code resolution for a load cell with a full-scale output of 10 mV.

This circuit allows great flexibility in designing a custom low-level signal conditioning front end that gives the user the ability to easily optimize the overall transfer function of the combined sensor-amplifier-converter circuit. The AD7791 maintains good performance over the complete output data range, from 9.5 Hz to 120 Hz, which allows it to be used in weigh scale applications that operate at various low speeds.

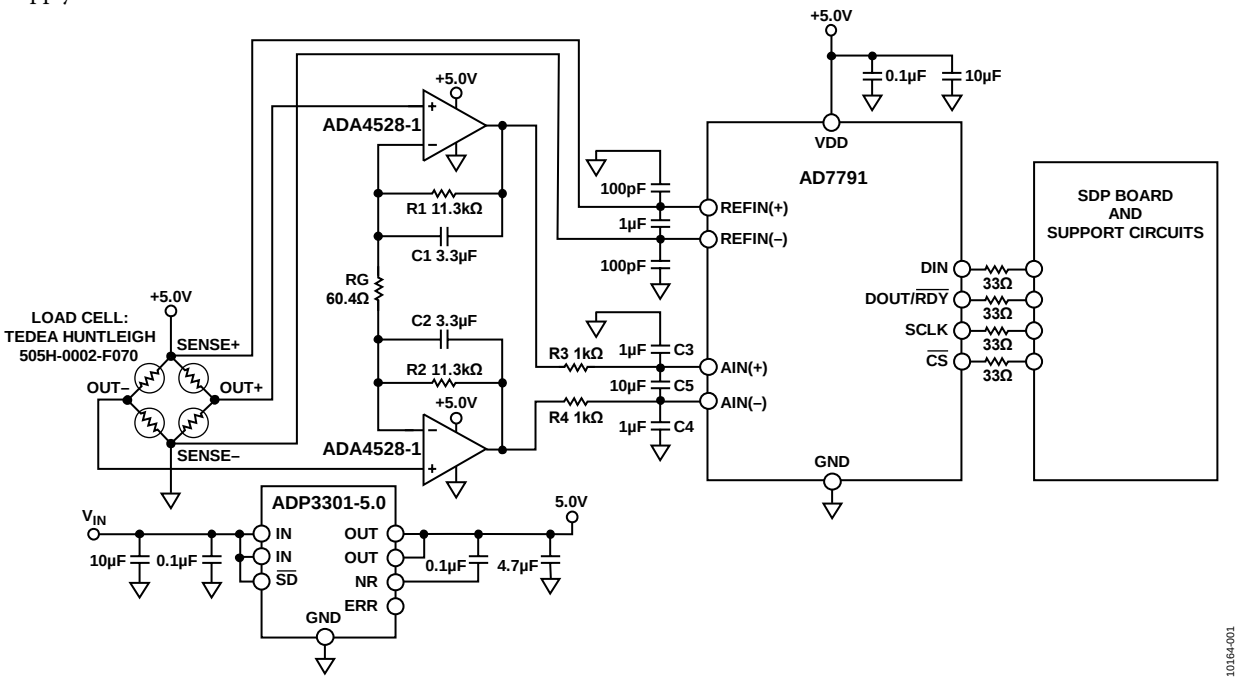

Figure 1. Weigh Scale System Using the AD7791 (Simplified Schematic, All Connections and Decoupling Not Shown)

Rev. 0

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CIRCUIT DESCRIPTION

Figure 2 shows the actual test setup. For testing purposes, a 6-wire Tedea-Huntleigh 505H-0002-F070 load cell is used.

Current flowing through a PCB trace produces an IR voltage drop, and with longer traces, this voltage drop can be several millivolts or more, introducing a considerable error. A 1 inch long, 0.005 inch wide trace of 1 oz copper has a resistance of approximately 100 mΩ at room temperature. With a load current of 10 mA, this can introduce a 1 mV error.

A 6-wire load cell has two sense pins, in addition to the excitation, ground, and two output connections. The sense pins are connected to the high side (excitation pin) and low side (ground pin) of the Wheatstone bridge. The voltage developed across the bridge can be accurately measured regardless of the voltage drop due to wire resistance. In addition, the AD7791 accepts differential analog inputs and a differential reference as well. These two sense pins are connected to the AD7791 reference inputs to create a ratiometric configuration that is immune to low frequency changes in the power supply excitation voltage. The ratiometric connection eliminates the need for a precision voltage reference.

Unlike a 6-wire load cell, a 4-wire load cell does not have sense pins, and the ADC differential reference pins are connected directly to the excitation voltage and ground. With this connection, there exists a voltage difference between the excitation pin and the reference pin on the ADC due to wire resistance. There will also be a voltage difference on the low side (ground) due to wire resistance. The system will not be completely ratiometric.

The Tedea-Huntleigh 2 kg load cell has a sensitivity of 2 mV/V and a full-scale output of 10 mV when the excitation voltage is 5 V. A load cell also has an offset, or TARE, associated with it. In addition, the load cell also has a gain error. Some customers use a DAC to remove or null the TARE. When the AD7791 uses a 5 V reference, its differential analog input range is equal to ±5 V, or 10 V p-p. The circuit in Figure 1 amplifies the load cell output by a factor of 375 (1 + 2R1/RG), so the full-scale input range referred to the load cell output is 10 V/375 = 27 mV p-p. This extra range relative to the 10 mV p-p load cell full-scale signal is beneficial as it ensures that the offset and gain error of the load cell do not overload the ADC's front end.

The low-level amplitude signal from the load cell is amplified by two ADA4528-1 zero-drift amplifiers. A zero-drift amplifier, as the name suggests, has a close to zero offset voltage drift. The amplifier continuously self-corrects for any dc errors, making it as accurate as possible. Besides having low offset voltage and drift, a zero-drift amplfier also exhibits no 1/f noise. This important feature allows precision weigh scale measurement at dc or low frequency.

The two ADA4528-1 op amps are configured as the first stage of a three op amp instrumentation amplifier. A third op amp connected as a difference amplifier would normally be used for the second stage, but in the circuit of Figure 1, the differential input of the AD7791 performs this function.

The gain is equal to 1 + 2R1/RG. Capacitors C1 and C2 are placed in the feedback loops of the op amps and form 4.3 Hz cutoff frequency low-pass filters with R1 and R2. This limits the amount of noise entering the sigma-delta ADC. C5 in conjunction with R3 and R4 form a differential filter with a cutoff frequency of 8 Hz, which further limits the noise. C3 and C4 in conjunction with R3 and R4 form common-mode filters with a cutoff frequency of 159 Hz.

The ADP3301 low noise regulator powers the AD7791, ADA4528-1, and the load cell. In addition to decoupling capacitors, a noise reduction capacitor is placed on the regulator output as recommended in the ADP3301 data sheet. It is essential that the regulator is low noise, because any noise on the power supply or ground plane introduces noise into the system and degrades the circuit performance.

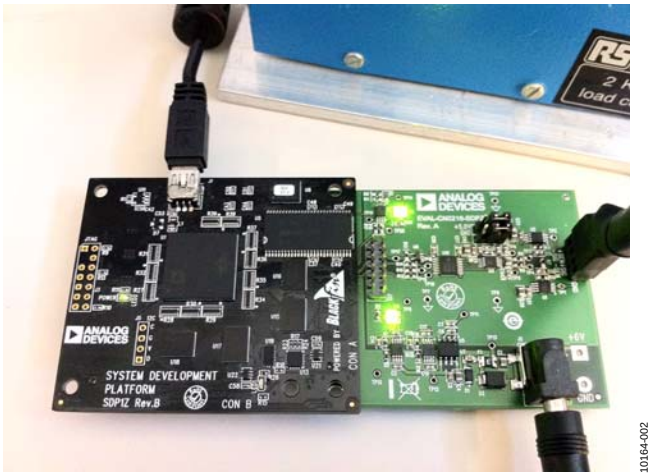

Figure 2. Weigh Scale System Setup Using the AD7791

The 24-bit sigma-delta ADC AD7791 converts the amplified signal from the load cell. The AD7791 is configured to operate in the buffered mode to accommodate the impedance of the R-C filter network on the analog input pins.

Figure 3 shows the AD7791's rms noise for different output data rates. This plot shows that the rms noise increases as the output data rate increases. However, the device maintains good noise performance over the complete range of output data rates.

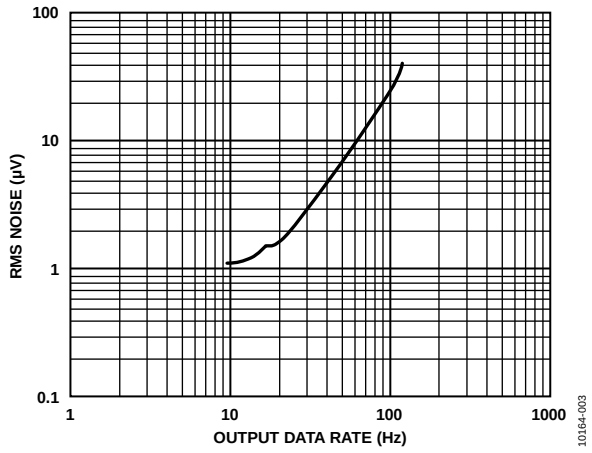

Figure 3. AD7791 RMS Noise for Different Output Data Rates and a 2.5 V Reference (5 V p-p Input Range), Buffer On

The AD7791 rms noise of 1.1 µV for a 9.5 Hz output data rate and a reference of 2.5 V yields the following number of noise-free counts:

$$\frac{5\text{ V}}{6.6 \times 1.1\,\mu\text{V}} = 688{,}705$$

where the factor of 6.6 converts the rms voltage into a peak-to-peak voltage.

The corresponding noise-free code resolution is, therefore:

$$\log_2(688{,}705) = \frac{\log_{10}(688{,}705)}{\log_{10}(2)} = 19.5\text{ bits}$$

Note that this represents the performance of the AD7791 without the load cell or the input amplifier connected.

The ADA4528-1 has 5.9 nV/√Hz of voltage noise density and, therefore, the input amplifiers and resistors will add noise to the system. In addition, the load cell itself will add noise.

In the circuit of Figure 1, a 5 V reference is used, therefore, the peak-to-peak input range is 10 V. The LSB is, therefore, equal to

$$1\text{LSB} = \frac{10\text{ V}}{2^{24}} = 0.596\,\mu\text{V}$$

The 10 mV p-p full-scale signal from the load cell produces a 3.75 V p-p signal into the ADC, which is approximately 38% of the ADC range.

Seven sets of 500 samples each were taken with the load cell connected (no load). The peak-to-peak code spread for each sample set was calculated, and the seven values averaged to yield a code spread of 159 counts. This corresponds to 159 × 0.596 µV = 94.8 µV p-p noise based on a full-scale input to the ADC of 3.75 V p-p.

Therefore, the number of noise-free counts is

$$\frac{3.75\text{ V}}{94.8\,\mu\text{V}} = 39{,}557$$

Therefore, the corresponding noise-free code resolution of the total system is:

$$\log_2(39{,}557) = \frac{\log_{10}(39{,}557)}{\log_{10}(2)} = 15.3\text{ bits}$$

Figure 4 shows a plot of the ADC codes for 500 samples (52.6 sec for 9.5 Hz data rate). Note that the peak-to-peak spread is about 160 codes.

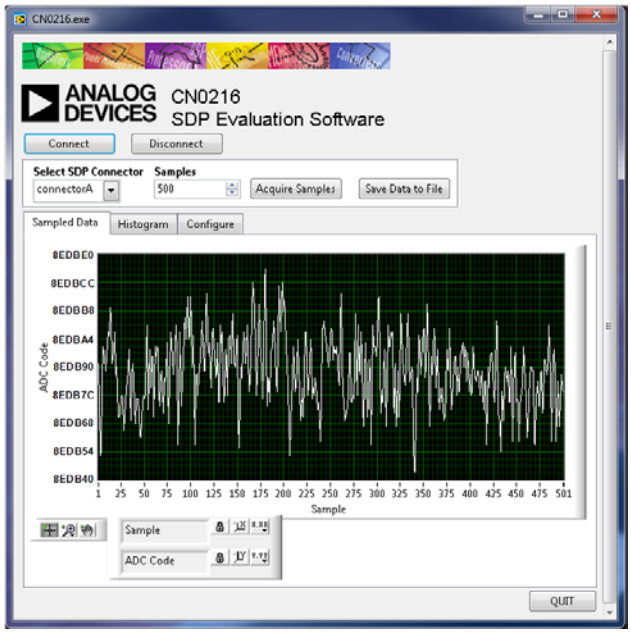

Figure 4. Measured Output Code for 500 Samples Showing the Effects of Noise

Figure 5 shows the same data presented in a histogram. Figure 4 and Figure 5 show the actual (raw) conversions read back from the AD7791. In practice, a digital post filter is typically used in a weigh scale system. The additional averaging that is performed in the post filter will further improve the number of noise-free counts at the expense of a reduced data rate.

The resolution of the system in grams can be calculated by

$$\frac{2\text{ kg}}{39{,}557} = 0.05\ g$$

As with any high accuracy circuit, proper layout, grounding, and decoupling techniques must be employed. See Tutorial MT-031, *Grounding Data Converters and Solving the Mystery of AGND and DGND* and Tutorial MT-101, *Decoupling Techniques* for more details. A complete design support package for this circuit note can be found at www.analog.com/CN0216-DesignSupport.

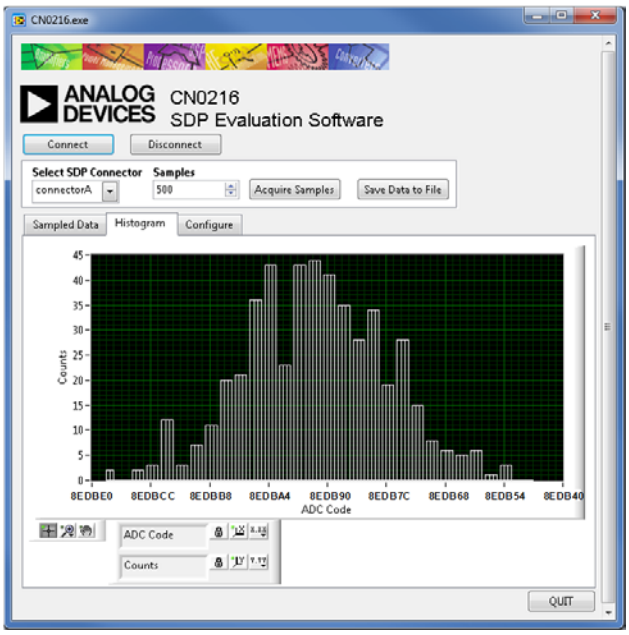

Figure 5. Measured Histogram for 500 Samples Showing the Effects of Noise

COMMON VARIATIONS

Other ADCs and circuits suitable for weigh scale applications are discussed in CN-0102 (AD7190), CN-0107 (AD7780), CN-0108 (AD7781), CN-0118 (AD7191), CN-0119 (AD7192), and CN-0155 (AD7195).

The AD7171 is a 16-bit sigma-delta ADC.

For a lower power consumption solution, use the ADA4051-2. The ADA4051-2 is a dual micropower, zero-drift amplifier with only 20 µA of supply current per amplifier.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0216-SDPZ circuit board and the EVAL-SDP-CB1Z system demonstration platform (SDP) evaluation board. The two boards have 120-pin mating connectors, allowing for the quick setup and evaluation of the circuit's performance. The EVAL-CN0216-SDPZ board contains the circuit to be evaluated, as described in this note, and the SDP evaluation board is used with the CN-0216 evaluation software to capture the data from the EVAL-CN0216-SDPZ circuit board.

Equipment Needed

- PC with a USB port and Windows XP or Windows Vista (32-bit), or Windows 7 (32-bit)
- EVAL-CN0216-SDPZ circuit evaluation board
- EVAL-SDP-CB1Z SDP evaluation board
- CN0216 evaluation software
- Tedea-Huntleigh 505H-0002-F070 load cell or equivalent
- Power supply: +6 V, or +6 V "wall wart"

Getting Started

Load the evaluation software by placing the CN0216 Evaluation Software disc in the CD drive of the PC. Using My Computer, locate the drive that contains the evaluation software disc and open the Readme file. Follow the instructions contained in the Readme file for installing and using the evaluation software.

Functional Block Diagram

See Figure 1 of this circuit note for the circuit block diagram, and the PDF file "EVAL-CN0216-SDPZ-SCH" for the circuit schematics. This file is contained in the CN0216 Design Support Package.

Setup

Connect the 120-pin connector on the EVAL-CN0216-SDPZ circuit board to the connector marked "CON A" on the EVAL-SDP-CB1Z evaluation (SDP) board. Nylon hardware should be used to firmly secure the two boards, using the holes provided at the ends of the 120-pin connectors. Connect the load cell the EVAL-CN0216-SDPZ board.

With power to the supply off, connect a +6 V power supply to the pins marked "+6 V" and "GND" on the board. If available, a +6 V "wall wart" can be connected to the barrel jack connector on the board and used in place of the +6 V power supply. Connect the USB cable supplied with the SDP board to the USB port on the PC. Note: Do not connect the USB cable to the mini USB connector on the SDP board at this time.

Test

Apply power to the +6 V supply (or "wall wart") connected to EVAL-CN0216-SDPZ circuit board. Launch the evaluation software and connect the USB cable from the PC to the USB mini-connector on the SDP board. The software will be able to communicate to the SDP board if the Analog Devices System Development Platform driver is listed in the Device Manager.

Once USB communications are established, the SDP board can now be used to send, receive, and capture serial data from the EVAL-CN0216-SDPZ board.

Information and details regarding how to use the evaluation software for data capture can be found in the CN0216 Evaluation Software Readme file.

Information regarding the SDP board can be found in the SDP User Guide.

Analyzing the Data

At least 500 samples of the ADC output data should be taken. Once the sample set is exported to a spreadsheet program, such as Excel, the samples can be analyzed. The standard deviation of the samples is approximately equal to the rms noise, assuming a Gaussian noise distribution. The peak-to-peak noise is approximately equal to the rms value multiplied by 6.6.

The peak-to-peak noise can also be taken directly from the sample set by simply taking the difference between the largest and smallest sample. In practice, the results obtained using this

method were approximately the same as the value obtained by multiplying the rms value by 6.6.

The values obtained from the sample set are in LSBs, so they must be converted into voltage, where 1 LSB = 0.596 µV for a 5 V reference.

If desired, the results of several sample sets can be averaged to get a more accurate measurement.

Noise-free code resolution is calculated from the peak-to-peak noise as described previously in this circuit note.

LEARN MORE

Kester, Walt. 1999. *Sensor Signal Conditioning*. Section 2. Analog Devices.

Kester, Walt. 1999. *Sensor Signal Conditioning*. Section 3. Analog Devices.

Kester, Walt. 1999. *Sensor Signal Conditioning*. Section 4. Analog Devices.

MT-004 Tutorial, *The Good, the Bad, and the Ugly Aspects of ADC Input Noise—Is No Noise Good Noise?* Analog Devices.

MT-022 Tutorial, *ADC Architectures III: Sigma-Delta ADC Basics,* Analog Devices.

MT-023 Tutorial, *ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-063 Tutorial, *Basic Three Op Amp In-Amp Configuration*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Wong, Vicky, AN-1114 Application Note, *Lowest Noise Zero-Drift Amplifier Has 5.6 nV/√Hz Voltage Noise Density*, Analog Devices.

CN-0102 Circuit Note, *Precision Weigh Scale Design Using the AD7190 24-Bit Sigma-Delta ADC with Internal PGA*, Analog Devices.

CN-0107 Circuit Note, *Weigh Scale Design Using the AD7780 24-Bit Sigma-Delta ADC with Internal PGA*, Analog Devices.

CN-0108 Circuit Note, *Weigh Scale Design Using the AD7781 20-Bit Sigma-Delta ADC with Internal PGA*, Analog Devices.

CN-0118 Circuit Note, *Precision Weigh Scale Design Using the AD7191 24-Bit Sigma-Delta ADC with Internal PGA*, Analog Devices.

CN-0119 Circuit Note, *Precision Weigh Scale Design Using the AD7192 24-Bit Sigma-Delta ADC with Internal PGA*, Analog Devices.

CN-0155 Circuit Note, *Precision Weigh Scale Design Using a 24-Bit Sigma-Delta ADC with Internal PGA and AC Excitation*, Analog Devices.

Data Sheets and Evaluation Boards

AD7791 Data Sheet

ADA4528-1 Data Sheet

ADP3301 Data Sheet

CN-0216 Circuit Evaluation Board (EVAL-CN0216-SDPZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

REVISION HISTORY

9/11—Revision 0: Initial Version

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0237.

Devices Connected/Referenced	
ADA4940-1/ ADA4940-2	Single/Dual, Ultralow Power, Low Distortion Differential ADC Driver
AD7982	18-Bit, 1 MSPS PulSAR ADC
ADR435	Ultralow Noise XFET Voltage Reference with Current Sink and Source Capability

Ultralow Power, 18-Bit, Differential PulSAR ADC Driver

EVALUATION AND DESIGN SUPPORT

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 uses the ultralow power AD7982 18-bit, 1 MSPS analog-to-digital converter (ADC) driven by the ADA4940-1, a low power fully differential amplifier. The ADR435 low noise precision 5.0 V voltage reference is used to supply the 5 V needed for the ADC. All the ICs shown in Figure 1 are available in small packages, either 3 mm × 3 mm LFCSP or 3 mm × 5 mm MSOP, which helps to reduce board cost and space.

Power dissipation of the ADA4940-1 in the circuit is typically 6.25 mW. The 18-bit, 1 MSPS AD7982 ADC consumes only 7 mW at 1 MSPS. This power also scales with the throughput. The ADR435 consumes only 4.7 mW, making the total power dissipated by the system less than 18 mW.

CIRCUIT DESCRIPTION

Modern high resolution SAR ADCs, such as the AD7982 18-bit, 1 MSPS PulSAR® ADC, require a differential driver for optimum performance. In such applications, the ADC driver takes either a differential or single-ended signal and performs the level shifting required to drive the input of the ADC at the right level.

Figure 1 shows the ADA4940-1 differential amplifier level shifting and driving the 18-bit AD7982 differential input successive approximation PulSAR ADC. Using four resistors, the ADA4940-1 can either buffer the signal with a gain of 1 or amplify the signal for more dynamic range. The ac and dc performances are compatible with those of the AD7982 18-bit, 1 MSPS PulSAR® ADC and other 16-bit and 18-bit members of the family, which have sampling rates of up to 2 MSPS. This circuit can also accept a single-ended input signal to generate the same fully differential output signal.

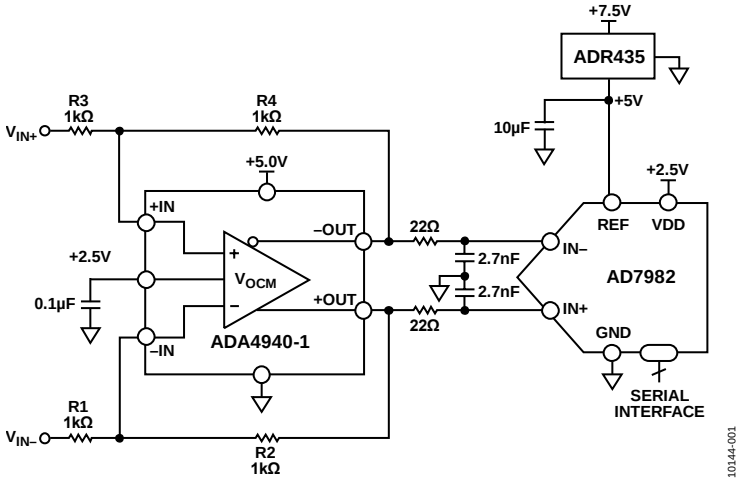

Figure 1. High Performance 18-Bit Differential ADC Driver (Simplified Schematic: All Connections and Decoupling Not Shown)

Rev. A

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The AD7982 operates on a single VDD supply of 2.5 V. It contains a low power, high speed, 18-bit sampling ADC and a versatile serial interface port. The reference voltage (REF) is applied externally from the ADR435 precision low dropout (0.3 V) band gap reference, and can be set independently of the supply voltage.

The ADA4940-1 operates from a 5 V single supply and offers sufficient headroom on the outputs, which swing from 0 V to 5 V with a 2.5 V common-mode and accommodate a full-scale input to the ADC. The ADA4940-1 is dc-coupled on the input and the output, and its outputs drive the inputs of the AD7982. It also allows single-ended to differential conversion if needed.

The gain is set by the ratio of the feedback resistor (R2 = R4) to the gain resistor (R1 = R3). For R1 = R2 = R3 = R4 = 1 kΩ, the single-ended input impedance is approximately 1.33 kΩ. In addition, the circuit can be used to convert either single-ended or differential inputs to a differential output. If needed, a termination resistor in parallel with the input can be used. Whether the input is a single-ended input or differential input, the input impedance of the amplifier can be calculated as shown in the MT-076 Tutorial and in the DiffAmpCalc™ Differential Amplifier Calculator (www.analog.com/DiffAmpCalc).

A single-pole, 2.7 MHz, RC (22 Ω, 2.7 nF) noise filter is placed between the op amp output and the ADC input to help limit the noise at the ADC input and to reduce the effect of kickbacks coming from the capacitive DAC input of the SAR ADC.

For the tests on this circuit, the signal generator provided a 10 V p-p differential output. The V_{OCM} input is bypassed for noise reduction and set externally with 1% resistors to maximize the output dynamic range on the 5 V reference. With an output common-mode voltage of 2.5 V, each ADA4940-1 output swings between 0 V and 5 V, opposite in phase, providing a gain of 1 and a 10 V p-p differential signal to the ADC input.

The FFT performance is shown in Figure 3 and is summarized as follows:

- Dynamic range = 97.33 dB
- SNR = 96.67 dBFS
- SINAD = 96.52 dBFS
- THD = −111.03 dBFS

Figure 2 shows the typical INL and DNL performance of the AD7982.

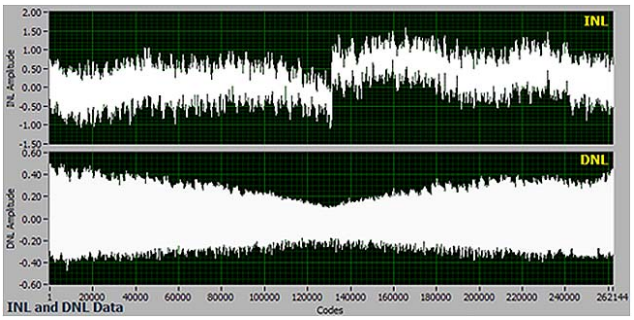

Figure 2. INL and DNL Plot for 20 kHz Signal, with Sampling Frequency of 1 MSPS (Min/Max INL = +1.6 LSB/−1.1 LSB and DNL = ±0.5 LSB)

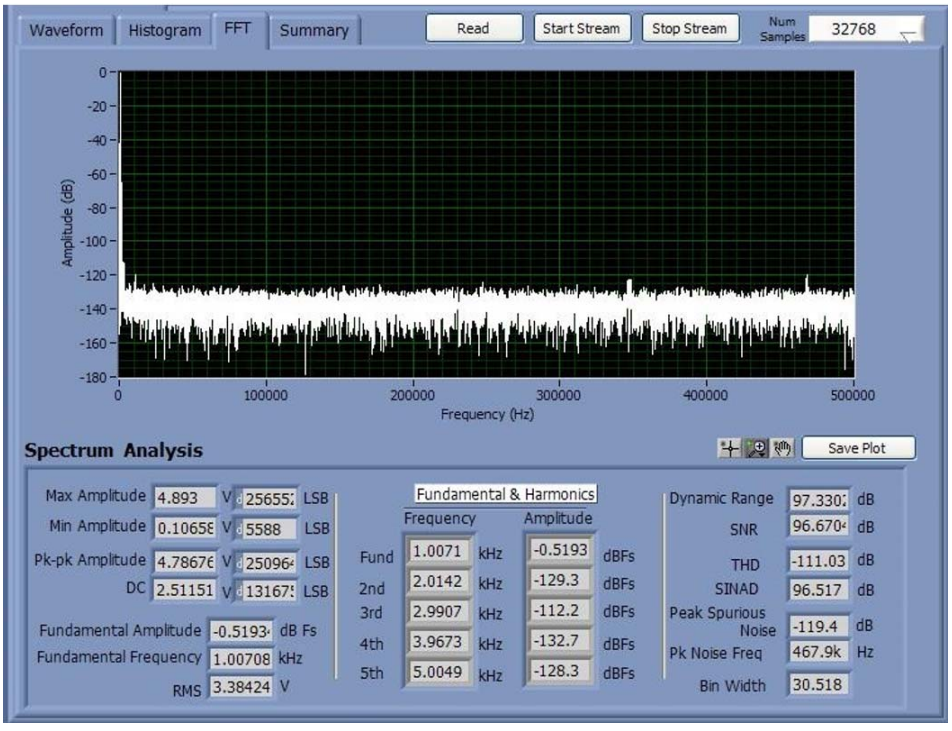

Figure 3. FFT Plot for 1 kHz Signal, 0.5 dB Below Full Scale, with Sampling Frequency of 1 MSPS

COMMON VARIATIONS

The circuit is proven to work with good stability and accuracy with the component values shown. Other ADCs can be used in place of the AD7982 to achieve the maximum desired performance. The ADA4940-1/ADA4940-2 are optimal for driving 16-bit and 18-bit ADCs with minimal degradation in performance. Faster sampling 18-bit ADCs include the AD7984 (1.33 MSPS) and AD7986 (2 MSPS). Differential 16-bit ADCs include the AD7688 (500 kSPS) and the AD7693 (500 kSPS).

The ADA4940-1/ADA4940-2 rail-to-rail outputs can be driven to within 0.5 V of each power rail without significant ac performance degradation. Other differential ADC drivers such as the AD8137 and ADA4941-1 can also be used to replace the ADA4940-1 for applications when speed, input impedance, or other factors dictate.

CIRCUIT EVALUATION AND TEST

This circuit was tested using a EVAL-AD7982SDZ PulSAR AD7982 evaluation board connected to the EVAL-SDP-CB1Z system demonstration platform.

The EVAL-AD7982SDZ is a user evaluation board intended to ease standalone testing of performance and functionality for the 18-bit AD7982 PulSAR ADC.

The EVAL-SDP-CB1Z board is a platform intended for use in evaluation, demonstration, and development of systems using Analog Devices, Inc. precision converters. It provides the necessary communications between the converter and the PC, programming or controlling the device, transmitting or receiving data over a USB link as shown in Figure 4 and Figure 5.

Equipment Needed

In addition to the two evaluation boards, external 5 V power supplies are required for the ADA4940-1. A wall wart supplies the 9 V dc voltage for the EVAL-SDP-CB1Z. Other appropriate voltages are supplied to the AD7982 evaluation board from the EVAL-SDP-CB1Z.

A low distortion signal source, the Audio Precision® SYS-2702, was used to achieve the required performance. A PC with Windows® XP or Windows 7 equipped with an USB port was used to run the PulSAR evaluation software.

Getting Started

Install the evaluation software as described at the EVAL-SDP-CB1Z and EVAL-AD7982SDZ product pages.

Connect the ADA49xx-1 EVAL-BRDZ, EVAL-AD7982SDZ, and EVAL-SDP-CB1Z boards together as shown in Figure 5. Connect a 9 V wall wart to the EVAL-AD7982SDZ, connect the USB cable to EVAL-SDP-CB1Z, and connect the external 5 V power supply to the ADA49xx-1 EVAL-BRDZ.

For more information on differential amplifier evaluation boards like the ADA49xx-1 EVAL-BRDZ, see the UG-132.

Setup and Test

An Audio Precision SYS-2702 source was used to provide the input signal to the EVAL-AD7982SDZ. The PulSAR evaluation software was used to monitor the ADC output results.

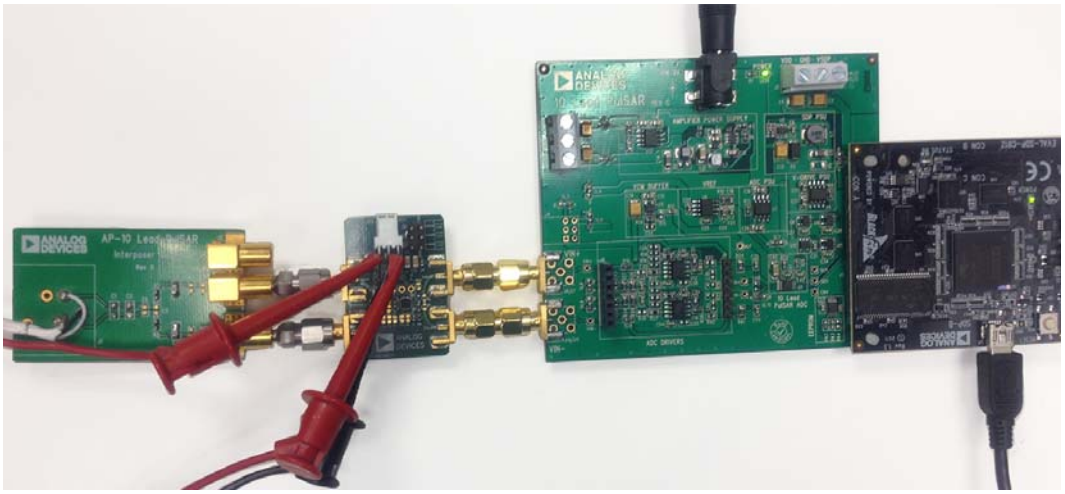

Figure 4. PulSAR ADC Evaluation Platform

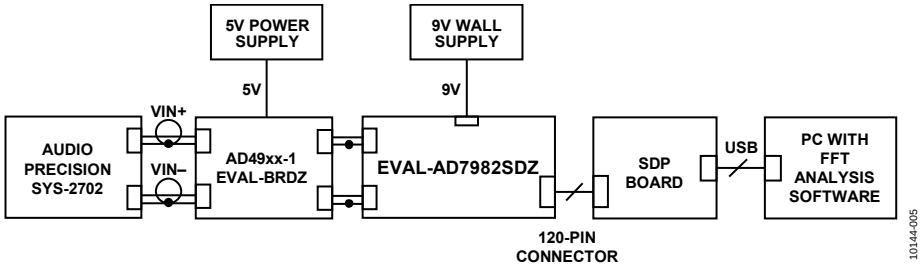

Figure 5. Test Setup Functional Block Diagram

LEARN MORE

CN-0237 Design Support Package:
www.analog.com/CN0237-DesignSupport

DiffAmpCalc™ Differential Amplifier Calculator

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, Analog Dialogue 39-09, September 2005.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*. Analog Devices.

MT-074 Tutorial. *Differential Drivers for Precision ADCs*. Analog Devices.

MT-075 Tutorial. *Differential Drivers for High Speed ADCs Overview*. Analog Devices.

MT-076 Tutorial. *Differential Driver Analysis*. Analog Devices.

MT-101 Tutorial. *Decoupling Techniques*. Analog Devices.

Data Sheets and Evaluation Boards

ADA4940-1 Data Sheet

ADA4940-2 Data Sheet

ADA4940 Evaluation Board

AD7982 Data Sheet

AD7982 Evaluation Board

ADR435 Data Sheet

REVISION HISTORY

2/15—Rev. 0 to Rev. A

Reorganized Layout.....Universal
Changes to Circuit Function and Benefits Section and Figure 1 1
Changes to Circuit Description Section, Figure 2, and Figure 3 2
Changes to Circuit Evaluation and Test Section, Figure 4, and Figure 5.....3

10/11—Revision 0: Initial Version

Circuits from the Lab™ Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0241.

Devices Connected/Referenced	
ADA4096-2	30 V, Micropower, Overvoltage Protection, Rail-to-Rail Input/Output Amplifier
AD7920	250 kSPS, 12-bit, 250 kSPS ADC in 6-Lead SC70
ADP3336	High Accuracy Ultralow I_Q 500 mA anyCAP® Adjustable Low Dropout Linear Regulator

High-Side Current Sensing with Input Overvoltage Protection

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0241 Circuit Evaluation Board (EVAL-CN0241-SDPZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

High-side current monitors are likely to encounter overvoltage conditions from transients or when the monitoring circuits are connected, disconnected, or powered down. This circuit, shown in Figure 1, uses the overvoltage protected ADA4096-2 op amp connected as a difference amplifier to monitor the high-side current. The ADA4096-2 has input overvoltage protection, without phase reversal or latch-up, for voltages of 32 V higher than and lower than the supply rails.

The circuit is powered by the ADP3336 adjustable low dropout 500 mA linear regulator, which can also be used to supply power to other parts of the system, if desired. Its input voltage can range from 5.2 V to 12 V when set for a 5 V output. To save power, the current sensing circuit can be powered down by removing power to the ADP3336; however, the power source, such as a solar panel, can still operate.

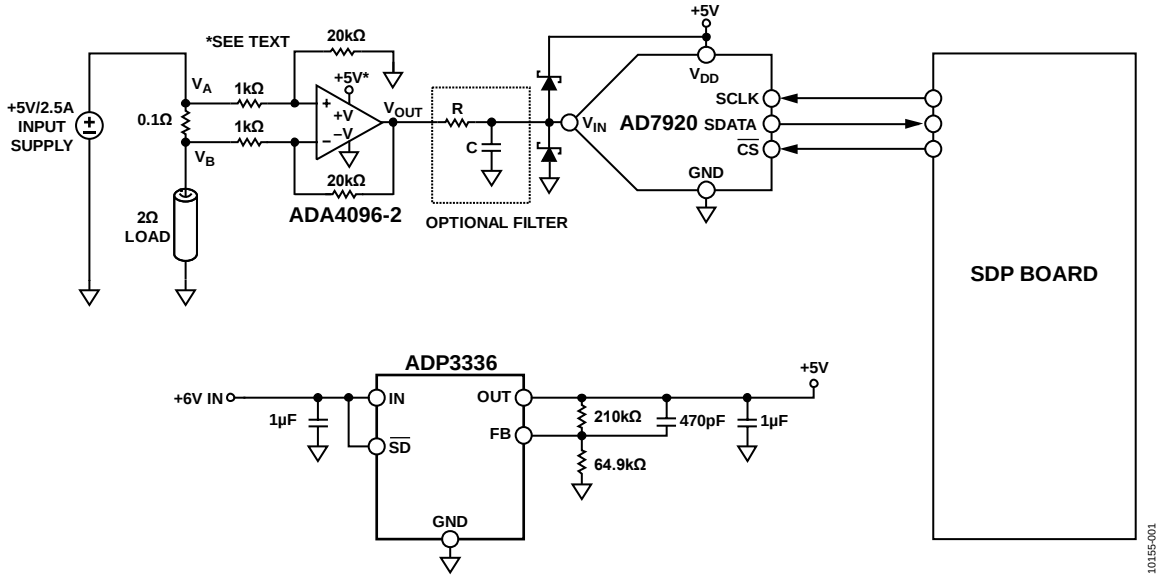

Figure 1. High-Side Current Sensing with Input Overvoltage Protection (Simplified Schematic: All Connections and Decoupling Not Shown)

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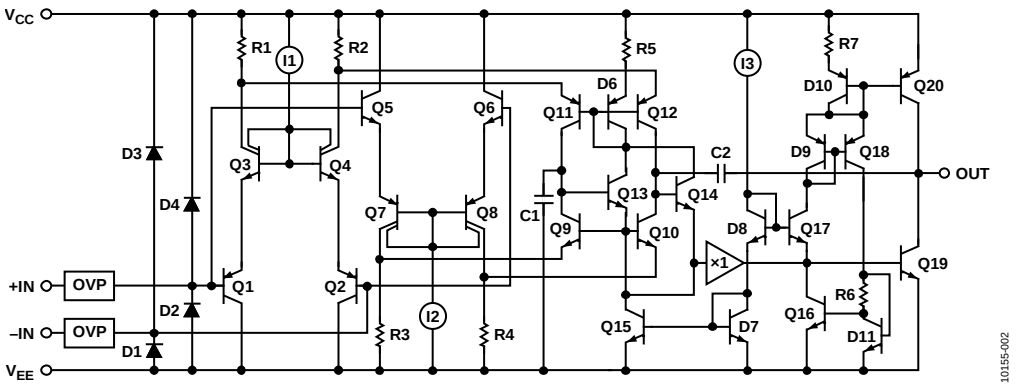

Figure 2. ADA4096-2 Simplfied Schematic

This applies voltage to the inputs of the unpowered ADA4096-2; however, no latch-up or damage occurs for input voltages up to 32 V. If slower throughput rates are required, the AD7920 can also be powered down between samples. The AD7920 draws a maximum of 5 µW when powered down and 15 mW when powered up. The ADA4096-2 requires only 120 µA under operational conditions. When operating at 5 V, this is only 0.6 mW. The ADP3336 draws only 1 µA in the shutdown mode.

CIRCUIT DESCRIPTION

The circuit is a classic high-side current sensing circuit topology with a single sense resistor. The other four resistors (dual 1 kΩ/ 20 kΩ divider) are in a thin film network (for ratio matching) and are used to set the difference amplifier gain. This amplifies the difference between the two voltages seen across the sense resistor and rejects the common-mode voltage.

$$V_{OUT} = (V_A - V_B)\ (20\ k\Omega/1\ k\Omega)$$

Figure 2 shows a simplified schematic of the ADA4096-2. The input stage comprises two differential pairs (Q1 to Q4 and Q5 to Q8) operating in parallel. When the input common-mode voltage approaches V_{CC} – 1.5 V, Q1 to Q4 shut down as I1 reaches its minimum voltage compliance. Conversely, when the input common-mode voltage approaches V_{EE} + 1.5 V, Q5 to Q8 shut down as I2 reaches its minimum voltage compliance. This topology allows for maximum input dynamic range because the amplifier can function with its inputs at 200 mV outside the rail (at room temperature).

As with any rail-to-rail input amplifier, V_{OS} mismatch between the two input pairs determines the CMRR of the amplifier. If the input common-mode voltage range is within 1.5 V of each rail, transitions between the input pairs are avoided, thus improving the CMRR by approximately 10 dB.

The ADA4096-2 inputs are protected from input voltage excursions up to 32 V outside each rail. This feature is of particular importance in applications with power supply sequencing issues that can cause the signal source to be active before the supplies to the amplifier are applied.

Figure 3 shows the input current limiting capability of the ADA4096-2 provided by low RDS_{ON} internal series FETs (green curves) compared to using a 5 kΩ external series resistor with an unprotected op amp (red curves).

Figure 3 was generated with the ADA4096-2 in a unity-gain buffer configuration with the supplies connected to GND (or ±15 V) and the positive input swept until it exceeds the supplies by 32 V. In general, input current is limited to 1 mA during positive overvoltage conditions and 200 µA during negative undervoltage conditions. For example, at an overvoltage of 20 V, the ADA4096-2 input current is limited to 1 mA, providing a current limit equivalent to a series 20 kΩ resistor.

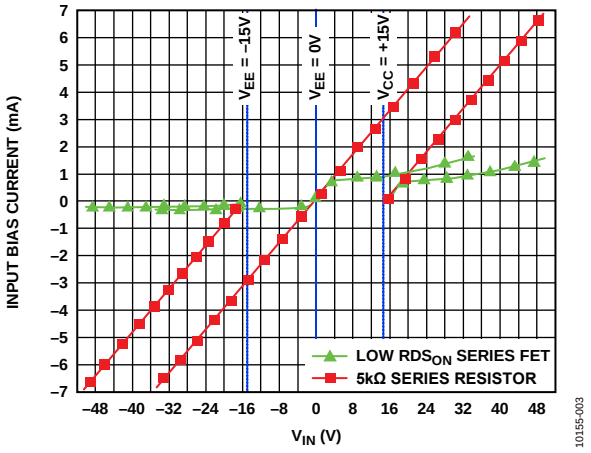

Figure 3. Input Current Limiting Capability

Figure 3 also shows that the current limiting circuitry is active whether the amplifier is powered or not.

Figure 3 represents input protection under abnormal conditions only. The correct amplifier operation input voltage range (IVR) is specified in Table 2 to Table 4 of the ADA4096-2 data sheet.

The AD7920 is a 12-bit, high speed, low power, successive approximation ADC. The part operates from a single 2.35 V to 5.25 V power supply and features throughput rates up to 250 kSPS. The part contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 13 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, SCLK, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$, and the conversion is initiated at this point. There are no pipeline delays associated with the part.

The AD7920 uses advanced design techniques to achieve very low power dissipation at high throughput rates.

To enter power-down mode, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK, and before the tenth falling edge of SCLK. Once $\overline{CS}$ is brought high in this window of SCLKs, the part enters power-down mode, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and SDATA goes back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power down due to glitches on the $\overline{CS}$ line.

To exit this mode of operation and power up the AD7920 again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the tenth SCLK. The device is fully powered up once 16 SCLKs have elapsed, and valid data results from the next conversion.

If $\overline{CS}$ is brought high before the tenth SCLK falling edge, the AD7920 goes back into power-down mode again. This avoids accidental power up due to glitches on the $\overline{CS}$ line or an inadvertent burst of eight SCLK cycles while $\overline{CS}$ is low. Although the device can begin to power up on the falling edge of $\overline{CS}$, it powers down again on the rising edge of $\overline{CS}$ as long as it occurs before the tenth SCLK falling edge.

Further details regarding the timing can be found in the AD7920 data sheet.

Test Results

An important measure of the performance of the circuit is the amount of noise in the final output voltage measurement.

Figure 4 shows a histogram of 10,000 measurement samples. This data was taken with the CN-0241 Evaluation Board connected to the EVAL-SDP-CB1Z SDP-B evaluation board. Details of the setup are described in the Circuit Evaluation and Test section.

The power supply was set to 3.0 V, and 10,000 samples of data were acquired at the maximum rate of 250 kSPS without having turned the output of the LDO off. Figure 4 shows the results of this acquisition. The peak-to-peak noise is approximately 2 LSBs, corresponding to about 0.3 LSB rms.

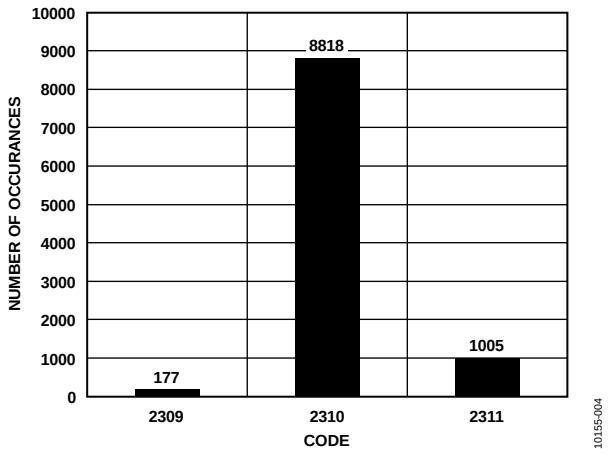

Figure 4. Histogram of Codes for 10,000 Samples Before Power Down

The $\overline{SD}$ shutdown pin connected to the ADP3336 was then asserted low in the software causing the output of the LDO to turn off. After approximately 1 minute, the shutdown pin on the ADP3336 was then asserted high, turning the output back on, and the same number of data samples were acquired. Figure 5 shows the results of this acquisition.

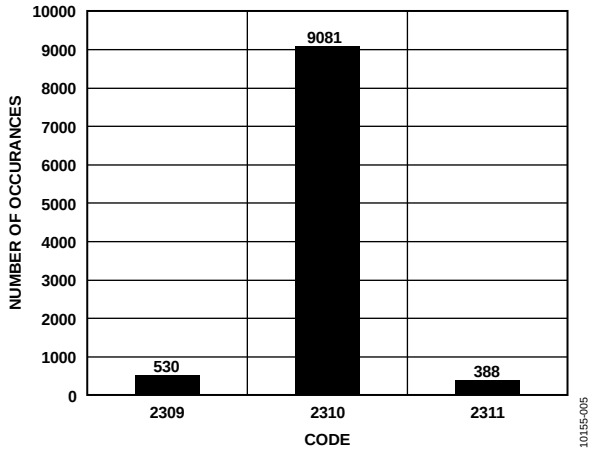

Figure 5. Histogram of Codes for 10,000 Samples After Power Down

Figure 5 shows that the output of the ADA4096-2 did not latch during power down when the input was held high.

A complete design support package for this circuit note can be found at www.analog.com/CN0241-DesignSupport.

COMMON VARIATIONS

The circuit is proven to work with good stability and accuracy. This board is also compatible with the SDP-S controller board (EVAL-SDP-CS1Z).

A slight modification to the circuit shown in Figure 1 allows monitoring the current for input supply voltages up to 30 V. Rather than connect the +V pin of the ADA4096-2 to 5 V from the ADP3336, connect it directly to the input supply being monitored. In this configuration, the ADA4096-2 is powered directly from the input supply.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0241-SDPZ circuit board and the EVAL-SDP-CB1Z SDP-B controller board. The two boards have 120-pin mating connectors, allowing for the quick setup and evaluation of the performance of the circuit. The EVAL-CN0241-SDPZ board contains the circuit to be evaluated, as described in this note, and the SDP-B controller board is used with the CN0241 evaluation software to capture the data from the EVAL-CN0241-SDPZ circuit board.

Equipment Needed

The following equipment is needed:

- A PC with a USB port and Windows® XP, Windows Vista®, or Windows® 7 (32-bit)
- EVAL-CN0241-SDPZ circuit evaluation board
- EVAL-SDP-CB1Z SDP-B controller board
- CN0241 SDP evaluation software
- DC power supply capable of driving 6 V/1 A
- DC power supply capable of driving 5 V/2.5 A
- 2 Ω/12 W load resistor

Getting Started

Load the evaluation software by placing the CN0241 evaluation software CD in the CD drive of the PC. Using **My Computer**, locate the drive that contains the evaluation software.

Functional Block Diagram

See Figure 1 of this circuit note for the circuit block diagram and the EVAL-CN0241-SDPZ-SCH-RevA.pdf file for the circuit schematics. This file is contained in the CN0241 Design Support Package.

Setup

Connect the 120-pin connector on the EVAL-CN0241-SDPZ circuit board to the CON A connector on the EVAL-SDP-CB1Z controller (SDP-B) board. Use Nylon hardware to firmly secure the two boards, using the holes provided at the ends of the 120-pin connectors. With power to the supply off, connect a 6 V power supply to the +6 V and GND pins on the board. If available, a 6 V wall wart can be connected to the barrel connector on the board and used in place of the 6 V power supply. Connect the USB cable supplied with the SDP-B board to the USB port on the PC. Do not connect the USB cable to the mini-USB connector on the SDP-B board at this time.

Connect the 5 V/2.5 A dc supply to +VIN and GND on J1 of the EVAL-CN0241-SDPZ board. Connect the 2 Ω/12 W load resistor to LOAD and GND of the EVAL-CN0241-SDPZ board.

Test

Apply power to the 6 V supply (or wall wart) connected to the EVAL-CN0241-SDPZ circuit board. Launch the evaluation software and connect the USB cable from the PC to the USB miniconnector on the SDP-B board.

Once USB communications are established, the SDP-B board can be used to send, receive, and capture serial data from the EVAL-CN0241-SDPZ board.

Turn the 5 V/2.5 A dc supply on when data is ready to be acquired. Adjust the voltage output accordingly to output the amount of current needed to be measured.

Figure 6 shows a screenshot of the CN0241 SDP evaluation software interface, and Figure 7 shows a screenshot of the EVAL-CN0241-SDPZ evaluation board. Information regarding the SDP-B board can be found in the SDP-B User Guide.

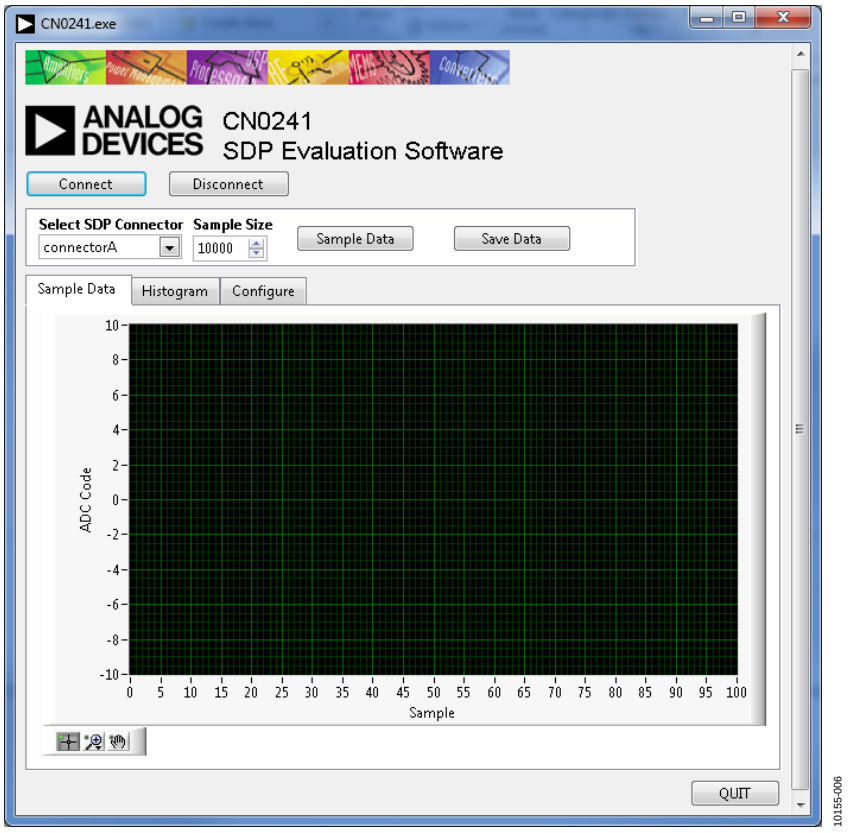

Figure 6. CN-0241 SDP Evaluation Software Interface

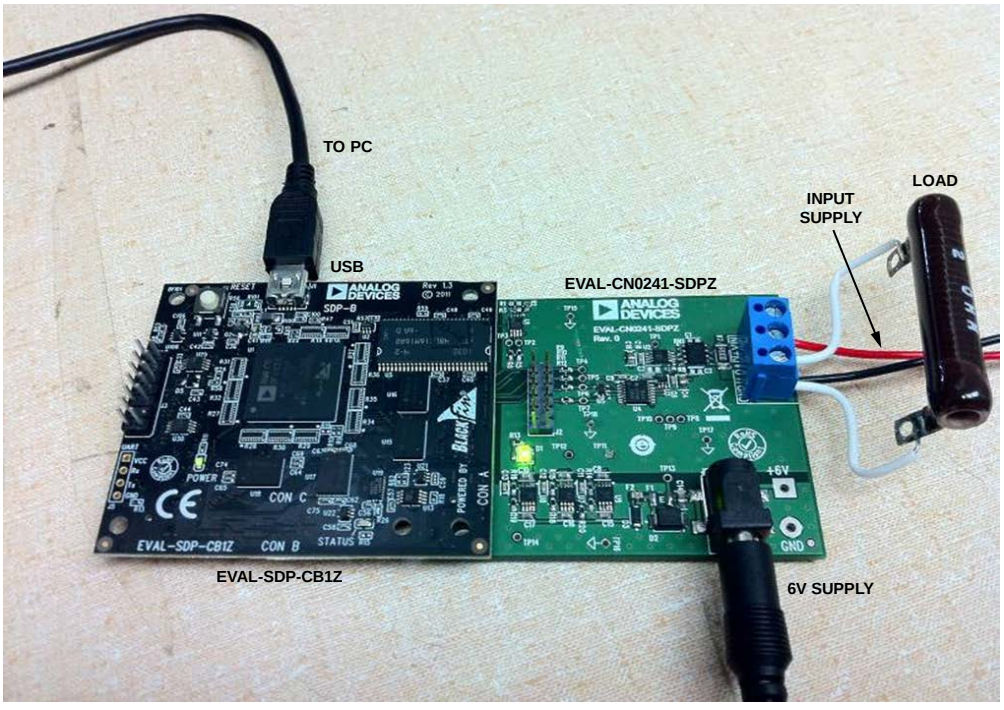

Figure 7. EVAL-CN0241-SDPZ Evaluation Board Connected to the SDP Board

LEARN MORE

CN0241 Design Support Package:
http://www.analog.com/CN0241-DesignSupport

SDP-B User Guide

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, Analog Dialogue 39-09, September 2005.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-035, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*, Analog Devices.

MT-036 Tutorial, *Op Amp Output Phase-Reversal and Input Over-Voltage Protection*, Analog Devices.

MT-068 Tutorial, *Difference and Current Sense Amplifiers*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

CN-0241 Circuit Evaluation Board (EVAL-CN0241-SDPZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

ADA4096-2 Data Sheet

AD7920 Data Sheet

ADP3336 Data Sheet

REVISION HISTORY

5/12—Rev. 0 to Rev. A

Changes to Circuit Function and Benefits Section and Figure 1 1
Changes to Figure 6.....5

1/12—Revision 0: Initial Version

Circuits from the Lab™ Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0326.

Devices Connected/Referenced	
AD7793	3-Channel, Low Noise, Low Power, 24-Bit Sigma Delta ADC
ADuM5401	Quad-Channel Isolators with Integrated DC/DC Converter
AD8603	MicroPower RRIO Low Noise Precision Single CMOS Op Amp

Isolated Low Power pH Monitor with Temperature Compensation

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN0326 Evaluation Board (EVAL-CN0326-PMDZ)
System Demonstration Platform (EVAL-SDP-CB1Z)
SDP PMOD Interposer Board (SDP-PMD-IB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a completely isolated low power pH sensor signal conditioner and digitizer with automatic temperature compensation for high accuracy.

The circuit gives 0.5% accurate readings for pH values from 0 to 14 with greater than 14-bits of noise-free code resolution and is suitable for a variety of industrial applications such as chemical, food processing, water, and wastewater analysis.

This circuit supports a wide variety of pH sensors that have very high internal resistance that can range from 1 MΩ to several GΩ, and digital signal and power isolation provides immunity to noise and transient voltages often encountered in harsh industrial environments.

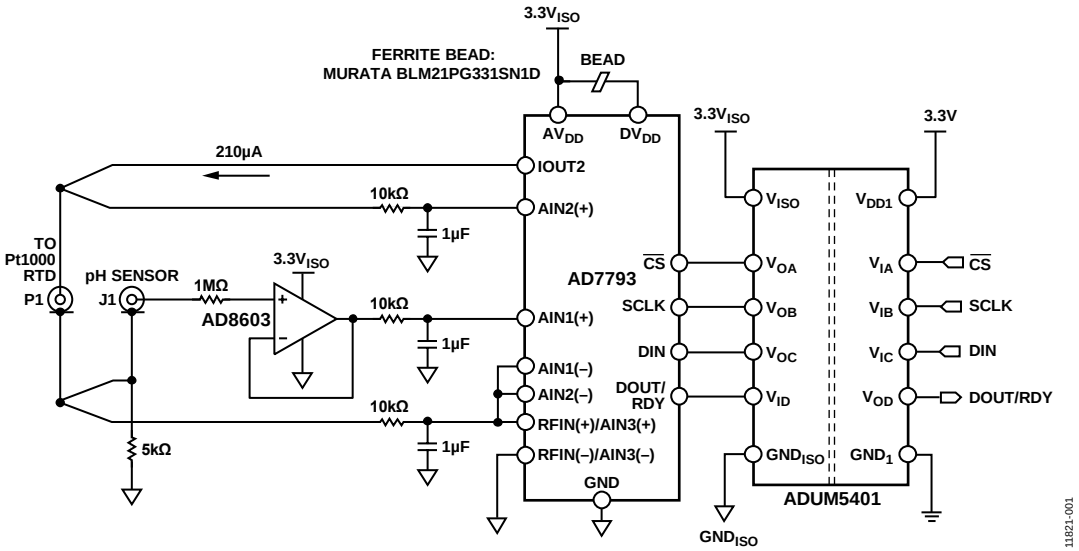

Figure 1. pH Sensor Circuit (Simplified Schematic: All Connections and Decoupling Not Shown)

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CIRCUIT DESCRIPTION

Fundamentals of pH Measurements

The pH value is a measure of the relative amount of hydrogen and hydroxide ions in an aqueous solution. In terms of molar concentrations, water at 25°C contains 1×10^{-7} moles/liter of hydrogen ions and the same concentration of hydroxide ions. A neutral solution is one in which the hydrogen ion concentration exactly equals the hydroxide ion concentration. pH is another way of expressing the hydrogen ion concentration and is defined as follows:

$$pH = -\log(H^+)$$

Therefore, if the hydrogen ion concentration is 1.0×10^{-2} moles/liter, the pH is 2.00.

The pH electrodes are electrochemical sensors used by many industries but are of particular importance to the water and wastewater industry. The pH probe consists of a glass measuring electrode and a reference electrode, which is analogous to a battery. When the probe is place in a solution, the measuring electrode generates a voltage depending on the hydrogen activity of the solution, which is compared to the potential of the reference electrode. As the solution becomes more acidic (lower pH) the potential of the glass electrode becomes more positive (+mV) in comparison to the reference electrode; and as the solution becomes more alkaline (higher pH) the potential of the glass electrode becomes more negative (−mV) in comparison to the reference electrode. The difference between these two electrodes is the measured potential. A typical pH probe ideally produces 59.154 mV/pH units at 25°C. This is expressed in the Nernst equation as follows

$$E = a - \frac{2.303\,R(T + 273.1)}{nF} \times (pH - pH_{ISO})$$

where:
E = voltage of the hydrogen electrode with unknown activity
a = ±30 mV, zero point tolerance
T = ambient temperature in °C
n = 1 at 25 °C, valence (number of charges on ion)
F = 96485 coulombs/mol, Faraday constant
R = 8.314 volt-coulombs /°K mol, Avogadro's number
pH = hydrogen ion concentration of an unknown solution
pH_{ISO} = 7, reference hydrogen ion concentration

The equation shows that the voltage generated is dependent on the acidity or alkalinity of the solution and varies with the hydrogen ion activity in a known manner. The change in temperature of the solution changes the activity of its hydrogen ions. When the solution is heated, the hydrogen ions move faster which result in an increase in potential difference across the two electrodes. In addition, when the solution is cooled, the hydrogen activity decreases causing a decrease in the potential difference. Electrodes are designed ideally to produce a zero volt potential when placed in a buffer solution with a pH of 7.

A good reference on the theory of pH is *pH Theory and Practice*, Radiometer Analytical SAS, Villeurbanne Cedex, France.

Circuit Details

The design provides a complete solution for pH sensor with temperature compensation. The circuit has three critical stages: the pH probe buffer, the ADC, and the digital and power isolator as shown in Figure 1.

The AD8603, a precision micro power (50 µA maximum) and low noise (22 nV/√Hz) CMOS operational amplifier configured as a buffer to the input of one of the channels of the AD7793. The AD8603 has a typical input bias current of 200 fA that provides an effective solution to the pH probe that has high internal resistance.

The pH sensing and temperature compensation system is based on the AD7793, 24-bit sigma-delta (Σ-Δ) with. It has three differential analog inputs and has an on-chip, low noise, programmable gain amplifier (PGA) that ranges from unity gain to 128. The AD7793 consumes only a maximum of 500 µA making it suitable for any low power applications. It has a low noise, low drift internal band gap reference and can accept external differential reference. The output data rate from the part is software programmable and can be varied from 4.17 Hz to 470 Hz.

The ADuM5401, quad-channel digital isolator with an integrated dc-to-dc converter provides the digital signal and power isolation between the microcontroller and the AD7793 digital lines. The *i*Coupler chip-scale transformer technology is used to isolate the logic signals and the power feedback path in the dc-to-dc converter.

Buffer for pH Sensor Interface

The electrode of a typical pH probe is made up of glass that creates an extremely high resistance that can range from 1 MΩ to 1 GΩ and acts as a resistance in series with the pH voltage source as shown in Figure 2.

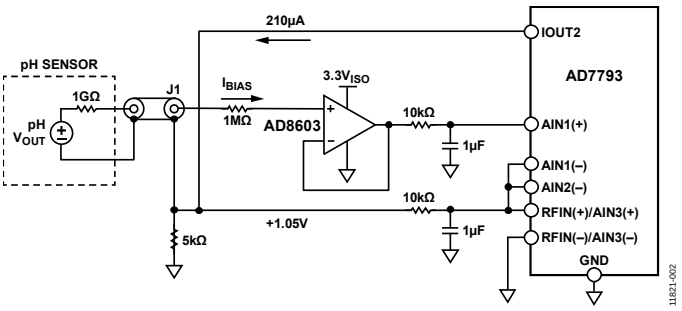

Figure 2. pH Sensor and Buffer Interface to ADC (Simplified Schematic: All Connections, RTD, and Decoupling Not Shown.)

The buffer amplifier bias current flowing through this series resistance introduces an offset error in the system. To isolate the circuit from this high source resistance, a buffer amplifier with high input impedance and very low input bias current is needed for this application. The AD8603 is used as a buffer amplifier for this application as shown in Figure 2. The low input current of the AD8603 minimizes the voltage error produced by the bias current flowing through the electrode resistance.

For 200 fA typical input bias current, the offset error is 0.2 mV (0.0037 pH) for a pH probe that has 1 GΩ series resistance at 25°C. Even at the maximum input bias current of 1 pA, the error is only 1 mV.

The cut-off frequency of the 10 kΩ/1 µF low pass noise filter for the buffer amplifier output is given by f= 1/2πRC, or 16 Hz.

Guarding, shielding, high insulation resistance standoffs, and other such standard picoamp methods must be used to minimize leakage at the high impedance input of the AD8603 buffer.

ADC Channel 1 Configuration, pH sensor

This stage involves measuring the small voltage generated by the pH electrode. Table 1 shows the specifications of a typical pH probe. Based on the Nernst equation, the full range voltage from the probe can range from ±414 mV (±59.14 mV/pH) at 25°C to ±490 mV (±70 mV/pH) at 80°C.

Table 1. Specifications of a Typical pH Probe

Measurement Range	pH 0 to pH 14
pH at zero voltage	pH 7.00 ± 0.25
Accuracy	pH 0.05 in the range from 20°C to 25°C
Resolution	pH 0.01 0.1 mV
Operating Temperature	Maximum 80°C
Reaction time	≤ 1 sec for 95% of final value

When reading the pH probe output voltage, the ADC uses the external 1.05 V reference and is configured with a gain of 1. The full-scale input range is $\pm V_{REF}/G = \pm 1.05$ V, and the maximum signal from the pH probe is ±490 mV at 80°C.

Because the output of the sensor is bipolar, and the AD7793 operates from a single power supply, the signal generated by the pH probe should be biased above ground so that it is within the acceptable common-mode range of the ADC. This bias voltage is generated by injecting the 210 µA IOUT2 current into the 5 kΩ, 0.1% resistor as shown in Figure 2. This generates the 1.05 V common-mode bias voltage that also serves as the ADC reference voltage.

ADC Channel 2 Configuration, RTD

The second channel of the ADC monitors the voltage generated across an RTD being driven by the IOUT2 current output pins of the AD7793. The 210 µA excitation current drives the series combination of the RTD and precision resistor (5 kΩ, 0.1%). (See Figure 1).

The temperature coefficient for pure platinum is 0.003926 Ω/Ω/°C. The normal coefficient for industrial RTDs is 0.00385 Ω/Ω/°C per the DIN Std. 43760-1980 and IEC 751-1983. The accuracy of an RTD is usually stated at 0°C. The DIN 43760 standard recognizes two classes as shown in Table 2, and ASTM E–1137 recognizes two grades as shown in Table 3.

Table 2. Standard RTD Accuracy for DIN-43760

Class	Tolerance
DIN 43760 Class A	±0.06% @ 0°C
DIN 43760 Class B	±0.12% @ 0°C

Table 3. Standard RTD Accuracy for ASTM E-1137

Grade	Tolerance
ASTM E-1137 Grade A	±0.05% @ 0°C
ASTM E-1137 Grade B	±0.10% @ 0°C

The RTD resistance value can be computed as

$$RTD\ Resistance = RTD_0\ (1 + T\,\alpha)$$

where:
RTD Resistance = Resistance value at T
RTD_0 = Resistance value at 0°C
T = ambient temperature
α = 0.00385 Ω/Ω/°C, temperature coefficient defined by DIN Std. 43760-1980 and IEC 751-1983

The RTD resistance varies from 0°C (1000 Ω) to 100°C (1385 Ω), producing a voltage signal range of 210 mV to 290 mV with 210 µA excitation current.

The precision 5 kΩ resistor generates the 1.05 V used as an external reference. With a gain of one, the analog input range is ±1.05 V ($\pm V_{REF}/G$). This architecture gives a ratiometric configuration. Changes in the value of the excitation current do not affect the accuracy of the system.

Although 100 Ω Pt RTDs are popular, other resistances (200 Ω, 500 Ω, 1000 Ω, etc.) and materials (Nickel, Copper, Nickel Iron) can be specified. This application uses a 1 kΩ DIN 43760 Class A RTD for temperature compensation of the pH sensor. A 1000 Ω RTD is less sensitive to wiring resistance errors than a 100 Ω RTD.

A 2-wire connection is made as shown in Figure 3. A constant current is applied through the leads of the RTD, and the voltage across the RTD itself is measured. The measuring device is the AD7793 that exhibits high input impedance and low input bias current. The sources of errors in this scheme are lead resistance, the stability of the constant current source produced by AD7793, and the input impedance and/or bias current in the input amplifier, and the associated drift.

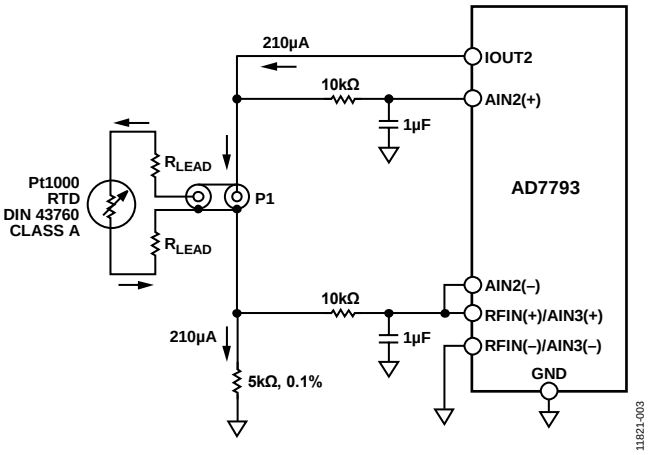

Figure 3. 2-Wire Pt RTD Connections (Simplified Schematic: All Connections and Decoupling Not Shown)

Another possibility for eliminating wiring resistance errors is the 3-wire RTD configuration that is described in detail in Circuit Note CN-0287.

Output Coding

The output code for an input voltage on either channel is

$$Code = 2^{N-1}\left(\frac{AIN \times GAIN}{V_{REF}} + 1\right)$$

where:
AIN is the analog input voltage.
GAIN is the in-amp setting.
N = 24

The EVAL-SDP-CB1Z system demonstration platform board and the PC processes the data output from the AD7793.

Digital and Power Isolation

The ADuM5401 isolates the ADC digital signals and also supplies isolated regulated 3.3 V power to the circuit. The input to the ADuM5401 (V_{DD1}) should be between 3.0 V and 3.6 V. Take care with the layout of the ADuM5401 to minimize EMI/RFI problems. For more details, please refer to Application Note AN-1109, *Recommendations for Control of Radiated Emissions with iCoupler Devices.*

System Calibration

In order to accurately measure the RTD resistance, the ±5% variation in the IOUT2 current must be taken into account. The AIN3(+) input to the AD7793 is used to measure the voltage dropped across the precision 5 kΩ 0.1% resistor. The exact IOUT2 current is then determined by dividing this voltage by 5 kΩ. The RTD resistance is calculated by dividing the voltage across the RTD by the exact IOUT2 current.

A two-point calibration procedure shown in Figure 4 is used to calibrate the pH meter in the EVAL-CN0326-PMDZ evaluation software.

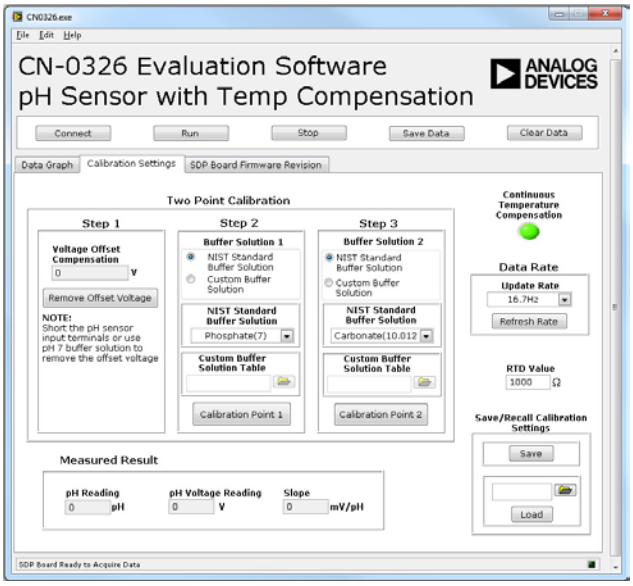

Figure 4. Evaluation Software Calibration Settings Window

The user is required to use a minimum of two buffer solutions, where a neutral pH buffer with a value of pH-7 should be used to remove the offset introduced by the pH probe and by the system. The neutral buffer solution can be used to set the first point for calibration. The pH of the second buffer solution depends on the pH of the solution to be measured. A pH-10 buffer solution can be used when measuring alkaline base solutions, and a pH-4 buffer can be used when measuring acidic solutions. For more precise measurement, a three point calibration can be performed. This can be done by using two different sets of buffer solutions in Step 2 and in Step 3 as shown in Figure 4, where the pH-7 solution is used to remove the offset.

The software includes a list of buffer solution recommended by the NIST. Each buffer solution described in the list has its own temperature coefficient from 0°C to 95°C, which can be found in "pH Theory and Practice" by Radiometer Analytical. The software uses this table to correlate the mV input from the pH probe to the correct pH value that correspond to the temperature read from the RTD sensor using linear interpolation to fill in the gaps in the table. The user is given an option to enable/disable the option for continuous temperature compensation by clicking the green button as shown in Figure 4.

Buffer solutions are commonly found in the market for pH sensor calibration. Other NIST-certified pH reference can also be used for calibration. Because of the variety of buffer solutions available, the software also provides the user an option to use their desired NIST-certified pH reference for calibration as shown in Figure 4.

The software also provides the user an option to use other RTD resistance values, but by default it is set to 1000 Ω.

System Noise Considerations

For an output data rate of 16.7 Hz and a gain of 1, the rms noise of the AD7793 equals 1.96 µV (noise is referred to input, taken from AD7793 data sheet). The peak-to-peak noise is

$$6.6 \times RMS\ Noise = 6.6 \times 1.96\ \mu V = 12.936\ \mu V$$

If the pH meter has a sensitivity of 59 mV/pH, the pH meter should measure the pH level to a noise-free resolution of

$$12.936\ \mu V / (59\ mV/pH) = 0.000219\ pH$$

This includes only the noise contribution of the AD7793. The actual system results are presented in the next section.

Test Data and Results

All data capture was performed using the CN0326 LabVIEW evaluation software. A Yokogawa GS200 precision voltage source was used to simulate the input of a pH sensor.

By sweeping the precision voltage from −420 mV to +420 mV in 1 mV increments, the EVAL-CN0326-PMDZ was able to capture the data according to the user defined calibration option.

The peak-to-peak noise of the AD8603 buffer and the AD7793 in the actual system was determined by shorting the input pH probe BNC connector and acquiring 1000 samples. As seen by the histogram in Figure 5, the code spread is approximately 500 codes, which translates to a peak-to-peak noise of 31.3 µV, with an equivalent pH reading spread of 0.00053 pH peak-to-peak.

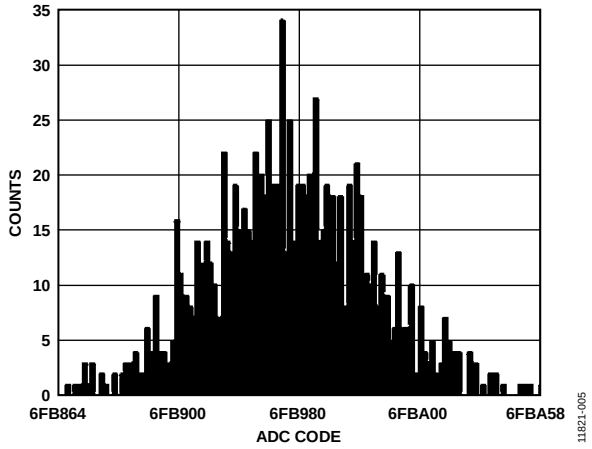

Figure 5. Histogram Showing Output Code Spread with AD7793 Input Pins Shorted Together

The system was tested with three different resistors in series with the ADC input to simulate the different impedances of the high impedance glass electrode. The system was also calibrated to give 60 mV/pH. According to Figure 6, the linearity error increases with the increase of simulated glass electrode impedance. Figure 6 also shows that over the entire simulated pH output voltage range, the linearity error is less than 0.5% with for a 200 MΩ pH probe impedance.

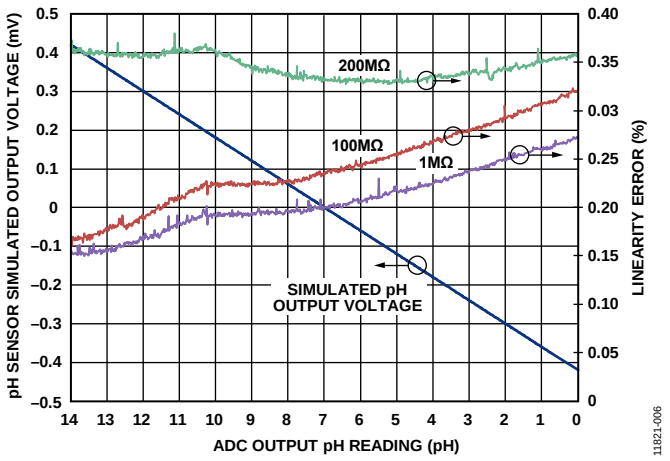

Figure 6. pH Sensor Simulated Output Voltage (with Associated Linearity Error Plot) vs. ADC Output pH Reading (Shown for Probe Resistance of 1 MΩ, 100 MΩ, and 200 MΩ)

The test data was taken using the board shown in Figure 7. Complete documentation for the system can be found in the CN-0326 Design Support package.

Figure 7. Photo of EVAL-CN0326-PMDZ Board

COMMON VARIATIONS

Other suitable ADCs are the AD7792 and AD7785. Both parts have the same feature set as the AD7793. However, the AD7792 is a 16-bit ADC while the AD7785 is a 20-bit ADC.

The AD8607 buffer amplifier is available in an 8-lead MSOP package . It is a dual micropower rail-to-rail input/output amplifier which is in the same family as the AD8603.

Other families of ADuM5401 includes a variety of channel configuration such as the ADuM5402/ADuM5403/ADuM5404 which also provides four independent isolation channels.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0326-PMDZ circuit board, the EVAL-SDP-CB1Z System Demonstration Platform (SDP) evaluation board and the SDP-PMD-IB1Z, a PMOD interposer board for the EVAL-SDP-CB1Z. The SDP and the SDP-PMD-IB1Z boards have 120-pin mating connectors, allowing the quick setup and evaluation of the circuit's performance. In order to evaluate the EVAL-CN0326-PMDZ board using the SDP-PMD-IB1Z and the SDP, the EVAL-CN0326-PMDZ is connected to the SDP-PMD-IB1Z by a standard 100 mil-spaced, 25 mil square, right angle pin-header connector.

Equipment Required

The following equipment is needed:

- A PC with a USB port and Windows® XP and Windows® Vista (32-bit), or Windows® 7 (32-bit)
- EVAL-CN0326-PMDZ circuit evaluation board
- EVAL-SDP-CB1Z circuit evaluation board
- SDP-PMD-IB1Z SDP interposer board
- CN0326 Evaluation Software
- Power supply: 6 V wall wart or equivalent
- Yokogawa 2000 Precision DC Power Supply or equivalent

Getting Started

Load the evaluation software by placing the CN-0326 Evaluation Software disc in the CD drive of the PC. Using "My Computer," locate the drive that contains the evaluation software disc and open the Readme file. Follow the instructions contained in the Readme file for installing and using the evaluation software.

Setup

The CN0326 evaluation kit includes self-installing software on a CD. The software is compatible with Windows® XP (SP2) and Vista (32-bit and 64-bit). If the setup file does not run automatically, you can run the **setup.exe** file from the CD.

Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

1. After installation from the CD is complete, power up the SDP-PMD-IB1Z evaluation board as described in the Power Supplies Configuration section. Connect the SDP board (via either Connector A) to the SDP-PMD-IB1Z evaluation board and then to the USB port of the PC that will be used for evaluation using the supplied cable.
2. Connect the 12-pin right angle male pin header of the EVAL-CN0326-PMDZ to the 12-pin right angle female pin header of the SDP-PMD-IB1Z.
3. Before running the program shown in Figure 9, connect the pH probe at the BNC terminal and the RTD sensor to the terminal jack of the EVAL-CN0326-PMDZ.
4. After all the peripherals and power supply are all connected and turned on, click **Connect** on the GUI shown in Figure 9. When the evaluation system is successfully detected by the PC, the EVAL-CN0326-PMDZ circuit board can now be evaluated using the software shown in Figure 9.

Functional Block Diagram

The functional block diagram of the test set-up is shown in Figure 8. The test set-up should be connected as shown. A screenshot of the main software window is shown in Figure 9.

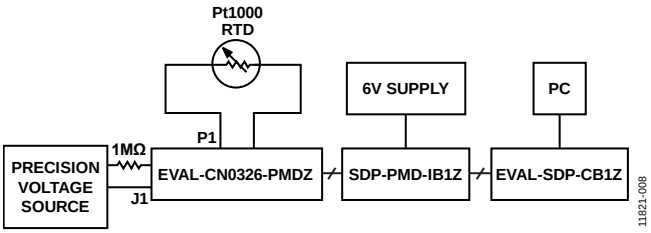

Figure 8. pH Sensor Block Diagram Test Set-up

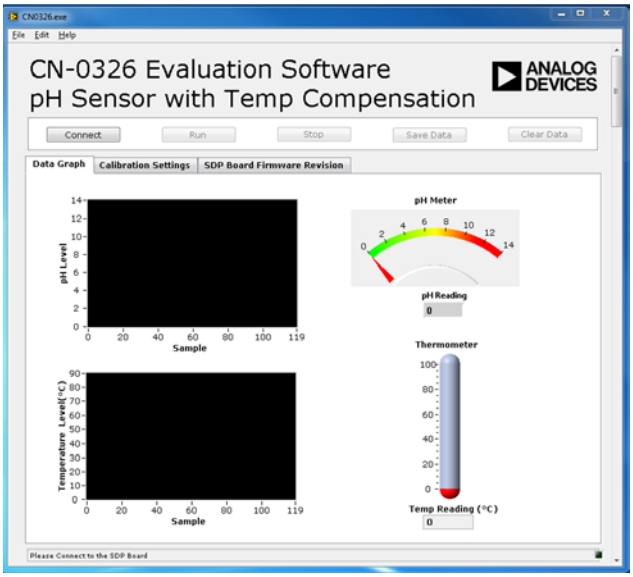

Figure 9. Evaluation Software Main Window

Power Supply Configuration

The SDP-PMD-IB1Z must be supplied with 6 V dc power supply and its jumper, JP1, should be set to 3.3 V to give power to the EVAL-CN0326-PMDZ.

Test

Agilent E3631A and Yokogawa GS200 precision voltage supplies were used to simulate the sensor output. The negative terminal of the Yokogawa is connected to the negative terminal of the ADC for the pH sensor. The positive terminal is in series with the resistor, which is connected to the positive terminal of the ADC as shown in Figure 8. The Yokogawa generates the ±420 mV, which then simulates the pH sensor output, and the series resistor is then varied to simulate the impedance of the glass electrode of the pH probe as shown in Figure 8.

The CN-0326 Evaluation Software is used to capture the data from the EVAL-CN0326-PMDZ circuit board using the setup seen in Figure 8.

Details regarding the use of the software can be found in the CN-0326 Software User Guide.

LEARN MORE

CN-0326 Design Support Package: www.analog.com/CN0326-DesignSupport

MT-004 Tutorial, *The Good, the Bad, and the Ugly Aspects of ADC Input Noise—Is No Noise Good Noise?* Analog Devices.

MT-022 Tutorial, *ADC Architectures III: Sigma-Delta ADC Basics,* Analog Devices.

MT-023 Tutorial, *ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues.* Analog Devices.

MT-037 Tutorial, *Op Amp Input Offset Voltage*.

MT-038 Tutorial, *Op Amp Input Bias Current*

MT-040 Tutorial, *Op Amp Input Impedance*

MT-095 Tutorial, *EMI, RFI, and Shielding Concepts*

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices

Kester, Walt. 1999. *High Impedance Sensors*. Section 5. Analog Devices.

Kester, Walt. 1999. *Temperature Sensors*. Section 7. Analog Devices.

Chen, Baoxing. 2006. *iCoupler® Products with isoPower® Technology: Signal and Power Transfer Across Isolation Barrier Using Microtransformers*. Analog Devices.

Wayne, Scott. 2005. "*i*Coupler® Digital Isolators Protect RS-232, RS-485, and CAN Buses in Industrial, Instrumentation, and Computer Applications." *Analog Dialogue*, Volume 39. Analog Devices (October).

Brian Kennedy and Mark Cantrell, *Recommendations for Control of Radiated Emissions with iCoupler Devices*, Application Note AN-1109, Analog Devices.

pH Theory and Practice, Radiometer Analytical, SAS, Villeurbanne Cedex, France.

Data Sheets and Evaluation Boards

AD7793 Data Sheet

AD7793 Evaluation Board

ADUM5401 Data Sheet

ADuM5401 Evaluation Board

AD8603 Data Sheet

REVISION HISTORY

9/13—Revision 0: Initial Version

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0357.

Devices Connected/Referenced	
ADA4528-2	5.0 V, Ultralow Noise, Zero Drift, RRIO, Dual Op Amp
AD5270-20	1024-Position,1% Resistor Tolerance Error, 50-TP Memory Digital Rheostat
ADR3412	Micropower, 0.1% Accurate,1.2 Voltage Reference
AD8500	Micropower, RRIO, Op Amp
AD7790	Low Power, 16-Bit Sigma-Delta, ADC

Low Noise, Single-Supply, Toxic Gas Detector, Using an Electrochemical Sensor with Programmable Gain TIA for Rapid Prototyping

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0357 Circuit Evaluation Board (EVAL-CN0357-PMDZ)
SDP to Pmod Interposer Board (PMD-SDP-IB1Z)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, and Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a single-supply, low noise, portable gas detector, using an electrochemical sensor. The Alphasense CO-AX carbon monoxide sensor is used in this example.

Electrochemical sensors offer several advantages for instruments that detect or measure the concentration of many toxic gases. Most sensors are gas specific and have usable resolutions under one part per million (ppm) of gas concentration.

The circuit shown in Figure 1 uses the ADA4528-2, dual auto zero amplifier, which has a maximum offset voltage of 2.5 µV at room temperature and an industry leading 5.6 µV/√Hz of voltage noise density. In addition, the AD5270-20 programmable rheostat is used rather than a fixed transimpedance resistor, allowing for rapid prototyping of different gas sensor systems, without changing the bill of materials.

The ADR3412 precision, low noise, micropower reference establishes the 1.2 V common-mode, pseudo ground reference voltage with 0.1% accuracy and 8 ppm/°C drift.

For applications where measuring fractions of ppm gas concentration is important, using the ADA4528-2 and the ADR3412 makes the circuit performance suitable for interfacing with a 16-bit ADC, such as the AD7790.

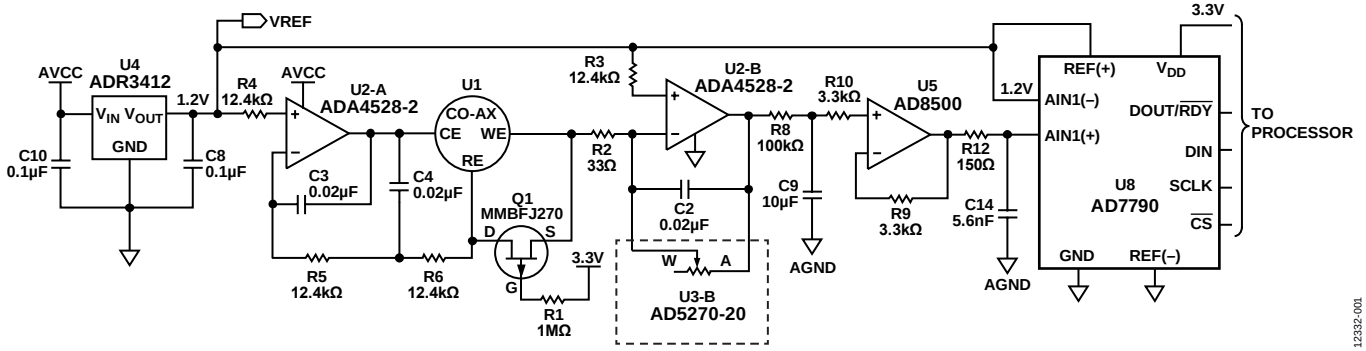

Figure 1. Low Noise Gas Detector Circuit (Simplified Schematic: all Connections and Decoupling not Shown)

Rev. 0

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Fax: 781.461.3113

CIRCUIT DESCRIPTION

Figure 2 shows a simplified schematic of an electrochemical sensor measurement circuit. Electrochemical sensors work by allowing gas to diffuse into the sensor through a membrane and by interacting with the working electrode (WE). The sensor reference electrode (RE) provides feedback to Amplifier U2-A, which maintains a constant potential with the WE terminal by varying the voltage at the counter electrode (CE). The direction of the current at the WE terminal depends on whether the reaction occurring within the sensor is oxidation or reduction. In the case of a carbon monoxide sensor, oxidation takes place; therefore, the current flows into the working electrode, which requires the counter electrode to be at a negative voltage (typically 300 mV to 400 mV) with respect to the working electrode. The op amp driving the CE terminal should have an output voltage range of approximately ±1 V with respect to V_{REF} to provide sufficient headroom for operation with different types of sensors (Alphasense Application Note AAN-105-03, *Designing a Potentiostatic Circuit*, Alphasense, Ltd.).

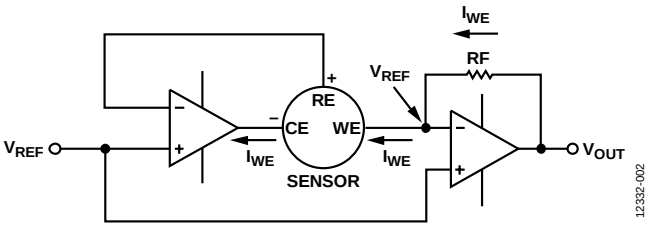

Figure 2. Simplified Electrochemical Sensor Circuit

The current into the WE terminal is less than 100 nA per ppm of gas concentration; therefore, converting this current into an output voltage requires a transimpedance amplifier with a very low input bias current. The ADA4528-2 op amp has CMOS inputs with a maximum input bias current of 220 pA at room temperature, making it a very good fit for this application.

The ADR3412 establishes the pseudo ground reference for the circuit, which allows for single-supply operation while consuming very little quiescent current (100 µA maximum).

Amplifier U2-A sinks enough current from the CE terminal to maintain a 0 V potential between the WE terminal and the RE terminal on the sensor. The RE terminal is connected to the inverting input of Amplifier U2-A; therefore, no current flows in or out of it. This means that the current comes from the WE terminal and it changes linearly with gas concentration. Transimpedance Amplifier U2-B converts the sensor current into a voltage proportional to the gas concentration.

The sensor selected for this circuit is an Alphasense CO-AX carbon monoxide sensor. Table 1 shows the typical specifications associated with carbon monoxide sensors of this general type.

Warning: carbon monoxide is a toxic gas, and concentrations higher than 250 ppm can be dangerous; therefore, take extreme care when testing this circuit.

Table 1. Typical Carbon Monoxide Sensor Specifications

Parameter	Value
Sensitivity	55 nA/ppm to 100 nA/ppm (65 nA/ppm typical)
Response Time (t_{90} from 0 ppm to 400 ppm CO)	<30 seconds
Range (ppm) CO, Guaranteed Performance)	0 ppm to 2,000 ppm
Overrange Limit (Specifications Not Guaranteed)	4,000 ppm

The output voltage of the transimpedance amplifier is

$$V_O = 1.2\ \text{V} + I_{WE} \times R_F \quad (1)$$

where I_{WE} is the current into the WE terminal, and R_F is the transimpedance feedback resistor (shown as the AD5270-20 U3-B rheostat in Figure 1).

The maximum response of the CO-AX sensor is 100 nA/ppm, and its maximum input range is 2000 ppm of carbon monoxide. These values result in a maximum output current of 200 µA and a maximum output voltage determined by the transimpedance resistor, as shown in Equation 2.

$$V_O = 1.2\ \text{V} + 2000\ \text{ppm} \times 100\frac{\text{nA}}{\text{ppm}} \times R_F$$

$$V_O = 1.2\ \text{V} + 200\ \mu\text{A} \times R_F \quad (2)$$

Applying 1.2 V to V_{REF} of the AD7790 allows a usable range of ±1.2 V at the output of the transimpedance amplifier, U2-B. Selecting a 6.0 kΩ resistor for the transimpedance feedback resistor gives a maximum output voltage of 2.4 V.

Equation 3 shows the circuit output voltage as a function of ppm of carbon monoxide, using the typical response of the sensor of 65 nA/ppm.

$$V_O = 1.2\ \text{V} + 390\frac{\mu\text{V}}{\text{ppm}} \quad (3)$$

The AD5270-20 has a nominal resistance value of 20 kΩ. There are 1024 resistance positions, resulting in resistance step sizes of 19.5 Ω. The 5 ppm/°C resistance temperature coefficient of the AD5270-20 is better than that of most discrete resistors, and its 1 µA of supply current is a very small contributor to the overall power consumption of the system.

Resistor R4 keeps the noise gain at a reasonable level. Selecting the value of this resistor is a compromise between the magnitude of the noise gain and the sensor settling time errors, when exposed to high concentrations of gas. For the example shown in Equation 4, R4 = 33 Ω, which results in a noise gain of 183.

$$NG = 1 + \frac{6.0\ \text{k}\Omega}{33\ \Omega} = 183 \quad (4)$$

The input noise of the transimpedance amplifier appears at the output, amplified by the noise gain. For this circuit, only low frequency noise is of interest because the frequency of operation of the sensor is very low. The ADA4528-2 has a 0.1 Hz to 10 Hz input voltage noise of 97 nV p-p; therefore, the noise at the output is 18 µV p-p, as shown in Equation 5.

$$V_{OUTPUTNOISE} = 97\ \text{nV} \times NG = 18\ \mu\text{Vp-p} \quad (5)$$

Because this is a very low frequency 1/f noise, the noise is very hard to filter. However, because the sensor response is also very slow, it is possible to use a very low frequency, low-pass filter (R5 and C6) with a cutoff frequency of 0.16 Hz. Even with such a low frequency filter, its effect on the sensor response time is negligible, when compared to the 30 second response time of the sensor.

The noise free code resolution of the system is determined from the peak-to-peak output noise. The maximum output of the ADA4528-2 is 2.4 V, so the noise free number of counts is

$$\textit{Total Noise Free Counts} = \frac{2.4\ \text{V}}{18\ \mu\text{V p-p}} = 64{,}865 \quad (6)$$

The noise free code resolution becomes

$$\textit{Noise Free Code Resolution} = \log_2(64{,}865) = 15.9\ \text{bits} \quad (7)$$

To take advantage of the entire ADC range available (±1.2 V), the AD8500 micropower, rail-to-rail input/output amplifier is chosen to drive the input of the AD7790. If the entire range is not necessary, the AD8500 can be removed and the internal buffer of the AD7790 can be used in its place.

One important characteristic of electrochemical sensors is their very long time constant. When first powered up, it can take several minutes for the output to settle to its final value. When exposed to a midscale step in concentration of the target gas, the time required for the sensor output to reach 90% of its final value can be in the order of 25 seconds to 40 seconds. If the voltage between the RE terminal and the WE terminal has a sudden change in magnitude, it can take several minutes for the output current of the sensor to settle. This long time constant also applies when cycling power to the sensor. To avoid very long start-up times, P-channel JFET Q1 shorts the RE terminal to the WE terminal when the supply voltage drops below the gate-to-source threshold voltage (~2.0 V) of the JFET.

COMMON VARIATIONS

Electrochemical sensors operate with very small amounts of current, making them well suited for portable, battery-powered instruments. If lower power is required, the ADA4505-2 amplifier has a maximum input bias current of 2 pA and consumes only 10 µA per amplifier. However, the noise of the ADA4505-2 is greater than that of the ADA4528-2.

The ADR291 precision voltage reference consumes only 12 µA and can be substituted for the ADR3412, if lower power is required.

More information can be found in Circuit Note CN-0234.

CIRCUIT EVALUATION AND TEST

The circuit shown in Figure 1 uses the EVAL-CN0357-PMDZ circuit evaluation board, the PMD-SDP-IB1Z interposer board, and the EVAL-SDP-CB1Z system demonstration platform (SDP-B) controller board. In addition, the EVAL-CN0357-PMDZ comes in a Pmod form factor, making it possible to connect the board to any Pmod controller board, allowing for rapid prototyping.

The CN-0357 Evaluation Software communicates with the SDP board to capture data from the EVAL-CN0357-PMDZ circuit evaluation board.

Equipment Needed

The following equipment is needed for evaluating the CN-0357 circuit:

- PC with USB port and Windows® XP, or Windows Vista (32-bit), or Windows 7 (32-bit)
- EVAL-CN0357-PMDZ evaluation board
- PMD-SDP-IB1Z interposer Board
- EVAL-SDP-CB1Z controller board
- CN-0357 Evaluation Software
- Calibration gas (less than 250 ppm)
- EVAL-CFTL-6V-PWRZ or equivalent 6 VDC power supply

Getting Started

Load the evaluation software by placing the CN-0357 Evaluation Software CD into the CD drive of the PC. Using **My Computer**, locate the drive that contains the evaluation software CD and run the **setup.exe**. Follow the on screen prompts for installing and using the evaluation software.

Functional Block Diagram

A functional block diagram of the test setup is shown in Figure 3. There is a complete schematic of the evaluation board contained in the CN-0357 Design Support Package, including printouts of the gerber files, as well as a bill of materials.

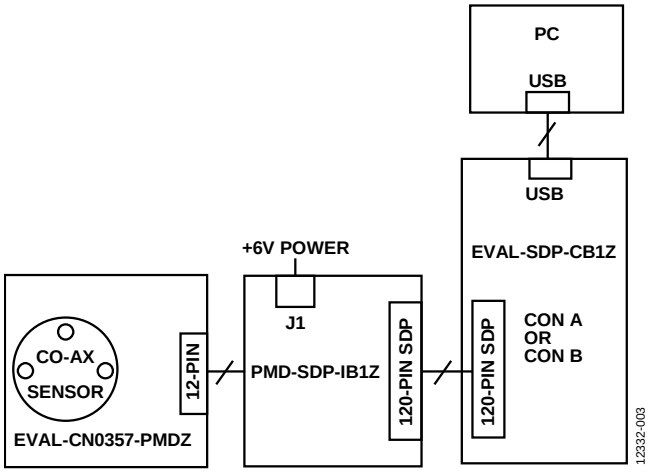

Figure 3. Test Setup Functional Block Diagram

Setup

Connect the electrochemical sensor to the socket on the EVAL-CN0357-PMDZ circuit evaluation board.

Connect the EVAL-CN0357-PMDZ to the interposer board and ensure that the jumper on the interposer board selects **+3.3 V** as the configuration. Next, connect the SDP-B board to the interposer board and apply power to the interposer board via the DC barrel jack.

Connect the USB cable supplied with the SDP-B board to the USB port on the PC and to the SDP-B board.

The software can communicate with the SDP board if the **Analog Devices System Development Platform** driver appears in the **Device Manager**. When USB communications are established, the SDP board can now send, receive, and capture serial data from the EVAL-CN0357-PMDZ circuit evaluation board.

Test

Navigate to the installation location of the CN-0357 Evaluation Software and open the CN0357.exe file. (The file should be located in a folder named Analog Devices in the start menu of the operating system.)

When the application opens, the software automatically connects to the SDP-B board. If multiple SDP-B controller boards are connected, the selected board will have a light emitting diode (LED) blinking.

The CN-0357 Evaluation Software User Guide contains information and details regarding how to use the evaluation software for data capture.

The input signal for this board is gas concentration; therefore, a calibration gas source is required. When testing with carbon monoxide, consider that 250 ppm is the maximum short term exposure limit.

The software is designed to be used with any electrochemical sensor, so it is important to input the correct specifications for the chosen sensor.

The maximum sensor sensitivity and sensor range are needed to calculate and set the resistance of the AD5270-20 digital rheostat. This value is a signed value. Positive values are used to describe sensors than sink current, whereas negative values are used to describe sensors that source current.

The typical sensor sensitivity is used to calculate the system conversion coefficient of ppm/mV.

Pressing the Run button begins acquisition of concentration data at 1 second intervals.

Figure 4 shows the circuit response after rapidly removing the sensor from the 175 ppm CO atmosphere and is a better representation of circuit performance.

A photo of the EVAL-CN0357-PMDZ board is shown in Figure 5.

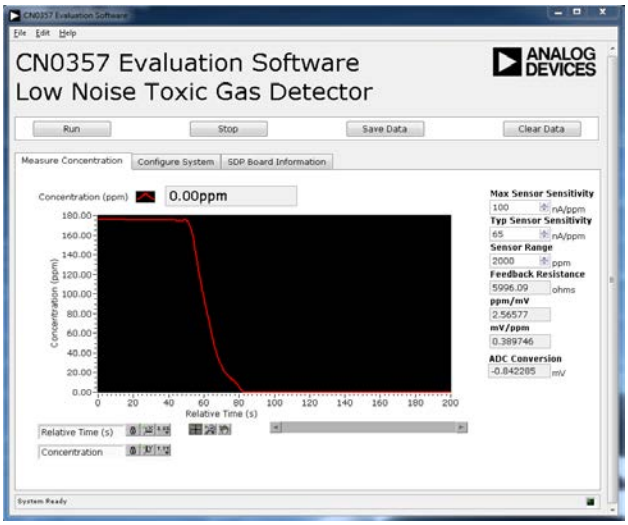

Figure 4. Response to a 175 ppm to 0 ppm Step of Carbon Monoxide

Figure 5. EVAL-CN0357-PMDZ Evaluation Board

LEARN MORE

CN-0357 Design Support Package:
http://www.analog.com/CN0357-DesignSupport

AN-1114, *Lowest Noise Zero-Drift Amplifier Has 5.6 nV/√Hz Voltage Noise Density,* Analog Devices.

MS-2066 Article, *Low Noise Signal Conditioning for Sensor-Based Circuits,* Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*, Analog Devices.

CN-0234 Circuit Note, *Single Supply, Micropower Toxic Gas Detector Using an Electrochemical Sensor,* Analog Devices.

Alphasense Application Note AAN-105-03, *Designing a Potentiostatic Circuit*, Alphasense Limited.

Data Sheets and Evaluation Boards

CN-0357 Circuit Evaluation Board (EVAL-CN0357-PMDZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

ADA4528-2 Data Sheet

AD5270-20 Data Sheet

ADR3412 Data Sheet

AD8500 Data Sheet

AD7790 Data Sheet

REVISION HISTORY

7/14—Revision 0: Initial Version

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0359.

Devices Connected/Referenced			
AD8253	10 MHz, 20 V/µs, G = 1, 10, 100, 1000, *i*CMOS Programmable Gain Instrumentation Amplifier	ADuCM360	Low Power, Precision Analog Microcontroller with Dual Sigma-Delta ADCs, ARM Cortex-M3
ADA4627-1	30 V, High Speed, Low Noise, Low Bias Current, JFET Operational Amplifier	AD8542	CMOS Rail-to-Rail General-Purpose Amplifiers
ADA4000-1	Low Cost, Precision JFET Input Operational Amplifiers	ADP2300	1.2 A, 20 V, 700 kHz/1.4 MHz, Nonsynchronous Step-Down Regulator
ADA4638-1	30 V, Zero-Drift, Rail-to-Rail Output Precision Amplifier	ADP1613	650 kHz/1.3 MHz, Step-Up PWM DC-to-DC Switching Converters
ADA4528-2	Precision, Ultralow Noise, RRIO, Dual, Zero-Drift Op Amp	ADG1211	Low Capacitance, Low Charge Injection, ±15 V/+12 V, iCMOS Quad SPST Switches
ADA4077-2	4 MHz, 7 nV/√Hz, Low Offset and Drift, High Precision Amplifiers	ADG1419	2.1 Ω On Resistance, ±15 V/+12 V/ ±5 V, iCMOS SPDT Switch
AD8592	CMOS, Single-Supply, Rail-to-Rail Input/Output Operational Amplifiers with Shutdown	ADM3483	3.3 V Slew Rate Limited, Half Duplex, RS-485/RS-422 Transceivers

Fully Automatic High Performance Conductivity Measurement System

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0359 Circuit Evaluation Board (EVAL-CN0359-EB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a completely self-contained, microprocessor controlled, highly accurate conductivity measurement system ideal for measuring the ionic content of liquids, water quality analysis, industrial quality control, and chemical analysis.

A carefully selected combination of precision signal conditioning components yields an accuracy of better than 0.3% over a conductivity range of 0.1 µS to 10 S (10 MΩ to 0.1 Ω) with no calibration requirements.

Automatic detection is provided for either 100 Ω or 1000 Ω platinum (Pt) resistance temperature devices (RTDs), allowing the conductivity measurement to be referenced to room temperature.

The system accommodates 2- or 4-wire conductivity cells, and 2-, 3-, or 4-wire RTDs for added accuracy and flexibility.

The circuit generates a precise ac excitation voltage with minimum dc offset to avoid a damaging polarization voltage on the conductivity electrodes. The amplitude and frequency of the ac excitation is user-programmable.

An innovative synchronous sampling technique converts the peak-to-peak amplitude of the excitation voltage and current to a dc value for accuracy and ease in processing using the dual, 24-bit Σ-Δ ADC contained within the precision analog microcontroller.

The intuitive user interface is an LCD display and an encoder push button. The circuit can communicate with a PC using an RS-485 interface if desired, and operates on a single 4 V to 7 V supply.

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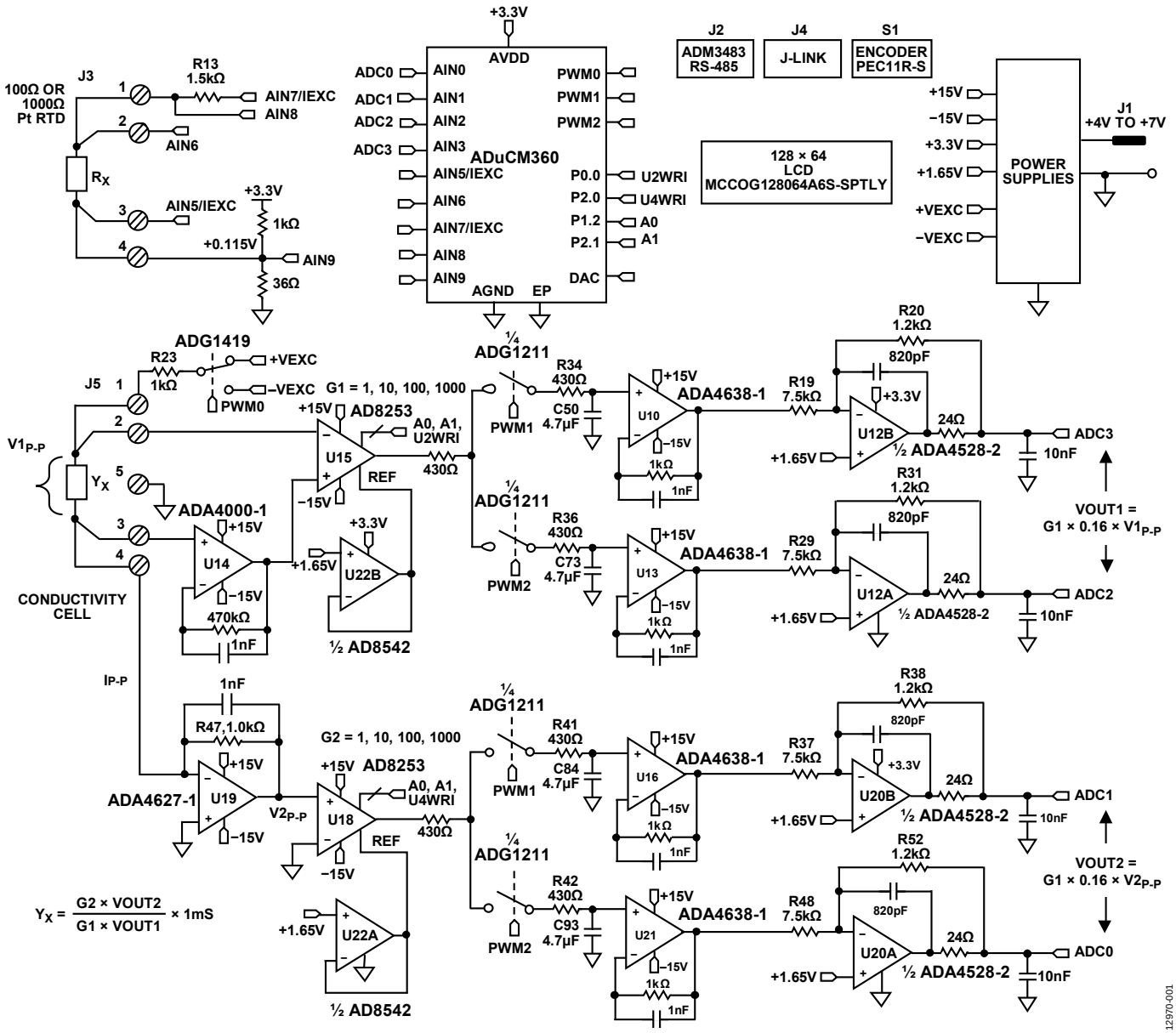

Figure 1. High Performance Conductivity Measurement System (Simplified Schematic: All Connections and Decoupling Not Shown)

CIRCUIT DESCRIPTION

The excitation square wave for the conductivity cell is generated by switching the ADG1419 between the +VEXC and −VEXC voltages using the PWM output of the ADuCM360 microcontroller. It is important that the square wave has a precise 50% duty cycle and a very low dc offset. Even small dc offsets can damage the cell over a period of time.

The +VEXC and −VEXC voltages are generated by the ADA4077-2 op amps (U9A and U9B), and their amplitudes are controlled by the DAC output of the ADuCM360, as shown in Figure 2.

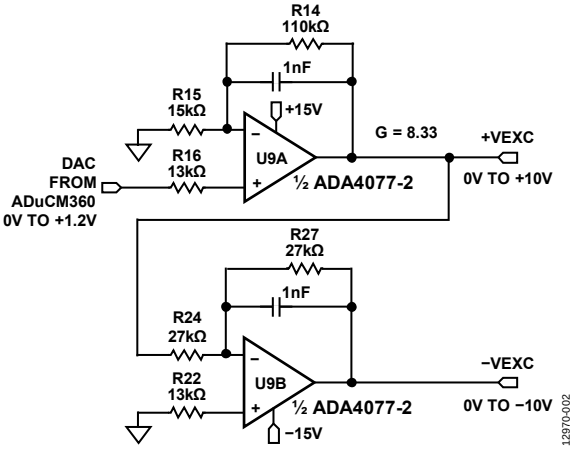

Figure 2. Excitation Voltage Sources

The ADA4077-2 has a typical offset voltage of 15 µV (A grade), a 0.4 nA bias current, a 0.1 nA offset current, and an output current of up to ±10 mA, with a dropout voltage of less than 1.2 V. The U9A op amp has a closed-loop gain of 8.33 and converts the ADuCM360 internal DAC output (0 V to 1.2 V) to the +VEXC voltage of 0 V to 10 V. The U9B op amp inverts the +VEXC and generates the −VEXC voltage. R22 is chosen such that R22 = R24||R27 to achieve first-order bias current cancellation. The error due to the 15 µV offset voltage of U9A is approximately (2 × 15 µV) ÷ 10 V = 3 ppm. The primary error introduced by the inverting stage is therefore the error in the resistor matching between R24 and R27.

The ADG1419 is a 2.1 Ω, on-resistance SPDT analog switch with an on-resistance flatness of 50 mΩ over a ±10 V range, making it ideal for generating a symmetrical square wave from the ±VEXC voltages. The symmetry error introduced by the ADG1419 is typically 50 mΩ ÷1 kΩ = 50 ppm. Resistor R23 limits the maximum current through the sensor to 10 V/1 kΩ = 10 mA.

The voltage applied to the cell, V1, is measured with the AD8253 instrumentation amplifier (U15). The positive input to U15 is buffered by the ADA4000-1 (U14). The ADA4000-1 is chosen because of its low bias current of 5 pA to minimize the error in measuring low currents associated with low conductivities. The negative input of the AD8253 does not require buffering.

The offset voltages of U14 and U15 are removed by the synchronous sampling stage and do not affect the measurement accuracy.

U15 and U18 are AD8253 10 MHz, 20 V/µs, programmable gain (G = 1, 10, 100, 1000) instrumentation amplifiers with gain error of less than 0.04%. The AD8253 has a slew rate of 20 V/µs and a settling time of 1.8 µs to 0.001% for G = 1000. Its common-mode rejection is typically 120 dB.

The U19 (ADA4627-1) stage is a precision current to voltage converter that converts the current through the sensor to a voltage. The ADA4627-1 has an offset voltage of 120 µV (typical, A grade), a bias current of 1 pA (typical), a slew rate of 40 V/µs, and a 550 ns settling time to 0.01%. The low bias current and offset voltage make it ideal for this stage. The symmetry error produced by the 120 µV offset error is only 120 µV/10 V = 12 ppm.

The U22A and U22B (AD8542) buffers supply the 1.65 V reference to the U18 and U15 instrumentation amplifiers, respectively.

The following is a description of the remainder of the signal path in the voltage channel (U17A, U17B, U10, U13, U12A, and U12B). The operation of the current channel (U17C, U17D, U16, U21, U20A, and U20B) is identical.

The ADuCM360 generates the PWM0 square wave switching signal for the ADG1419 switch as well as PWM1 and PWM2 synchronizing signals for the synchronous sampling stages. The cell voltage and the three timing waveforms are shown in Figure 3.

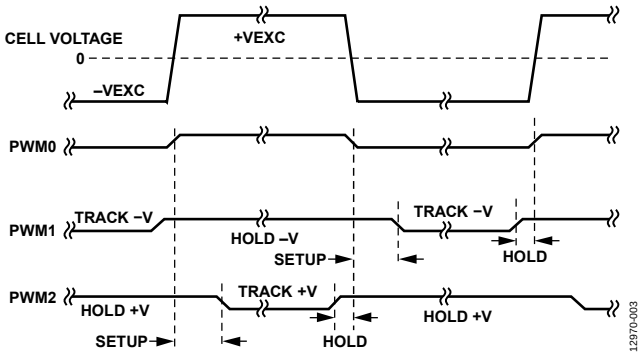

Figure 3. Cell Voltage and Track-and-Hold Timing Signals

The output of the AD8253 in amp (U15) drives two parallel track-and-hold circuits composed of ADG1211 switches (U17A/U17B), series resistors (R34/R36), hold capacitors (C50/C73), and unity-gain buffers (U10/U13).

The ADG1211 is a low charge injection, quad SPST analog switch, operating on a ±15 V power supply with up to ±10 V input signals. The maximum charge injection due to switching is 4 pC, which produces a voltage error of only 4 pC ÷ 4.7 µF = 0.9 µV.

The PWM1 signal causes the U10 track-and-hold buffer to track the negative cycle of the sensor voltage and then hold it until the next track cycle. The output of the U10 track-and-hold buffer is therefore a dc level corresponding to the negative amplitude of the sensor voltage square wave.

Similarly, the PWM2 signal causes the U13 track-and-hold buffer to track the positive cycle of the sensor voltage and then hold it until the next track cycle. The output of the U13 track-and-hold buffer is therefore a dc level corresponding to the positive amplitude of the sensor voltage square wave.

The bias current of the track-and-hold buffers (ADA4638-1) is 45 pA typical, and the leakage current of the ADG1211 switch is 20 pA typical. Therefore, the worst-case leakage current on the 4.7 µF hold capacitors is 65 pA. For a 100 Hz excitation frequency, the period is 10 ms. The drop voltage over one-half the period (5 ms) due to the 65 pA leakage current is (65 pA × 5 ms) ÷ 4.7 µF = 0.07 µV.

The offset voltage of the ADA4638-1 zero-drift amplifier is only 0.5 µV typical and contributes negligible error.

The final stages in the signal chain before the ADC are the ADA4528-2 inverting attenuators (U12A and U12B) that have a gain of −0.16 and a common-mode output voltage of +1.65 V. The ADA4528-2 has an offset voltage of 0.3 µV typical and therefore contributes negligible error.

The attenuator stage reduces the ±10 V maximum signal to ±1.6 V with a common-mode voltage of +1.65 V. This range is compatible with the input range of the ADuCM360 ADC input, which is 0 V to 3.3 V (1.65 V ± 1.65 V) for an AVDD supply of 3.3 V.

The attenuator stages also provide noise filtering and have a −3 dB frequency of approximately 198 kHz.

The differential output of the voltage channel, VOUT1, is applied to the AIN2 and AIN3 inputs of the ADuCM360. The differential output of the current channel, VOUT2, is applied to the AIN0 and AIN1 inputs of the ADuCM360.

The equations for the two outputs are given by

$$VOUT1 = G1 \times 0.16 \times V1_{P-P} \quad (1)$$

$$VOUT2 = G2 \times 0.16 \times V2_{P-P} \quad (2)$$

The cell current is given by

$$I_{P-P} = V1_{P-P} \times Y_X \quad (3)$$

The $V2_{P-P}$ voltage is given by

$$V2_{P-P} = I_{P-P} \times R47 \quad (4)$$

Solving Equation 4 for I_{P-P} and substituting into Equation 3 yields the following for Y_X:

$$Y_X = \frac{V2_{P-P}}{V1_{P-P} \times R47} \quad (5)$$

Solving Equation 1 and Equation 2 for $V1_{P-P}$ and $V2_{P-P}$ and substituting into Equation 5 yields the following:

$$Y_X = \frac{G2 \times VOUT2}{G1 \times VOUT1 \times R47} \quad (6)$$

$$Y_X = \frac{G2 \times VOUT2}{G1 \times VOUT1} \times 1\,\text{mS} \quad (7)$$

Equation 7 shows that the conductivity measurement depends on G1, G2, and R47, and the ratio of VOUT2 to VOUT1. Therefore, a precision reference is not required for the ADCs within the ADuCM360.

The AD8253 gain error (G1 and G2) is 0.04% maximum, and R47 is chosen to be a 0.1% tolerance resistor.

From this point, the resistors in the VOUT1 and VOUT2 signal chain determine the overall system accuracy.

The software sets the gain of each AD8253 as follows:

- If the ADC code is over 93.2% of full scale, the gain of the AD8253 is reduced by a factor of 10 on the next sample.
- If the ADC code is less than 9.13% of full scale, the gain of the AD8253 is increased by a factor of 10 on the next sample.

System Accuracy Measurements

The following four resistors affect the accuracy in the VOUT1 voltage channel: R19, R20, R29, and R31.

The following five resistors affect the accuracy in the VOUT2 current channel: R47, R37, R38, R48, and R52.

Assuming that all nine resistors are 0.1% tolerance, and including the 0.04% gain error of the AD8253, a worst-case error analysis yields approximately 0.6%. The analysis is included in the CN-0359 Design Support Package.

In practice, the resistors are more likely to combine in an RSS manner, and the RSS error due to the resistor tolerances in the positive or negative signal chain is $\sqrt{5} \times 0.1\% = 0.22\%$.

Accuracy measurements were taken using precision resistors from 1 Ω to 1 MΩ (1 S to 1 µS) to simulate the conductivity cell. Figure 4 shows the results, and the maximum error is less than 0.1%.

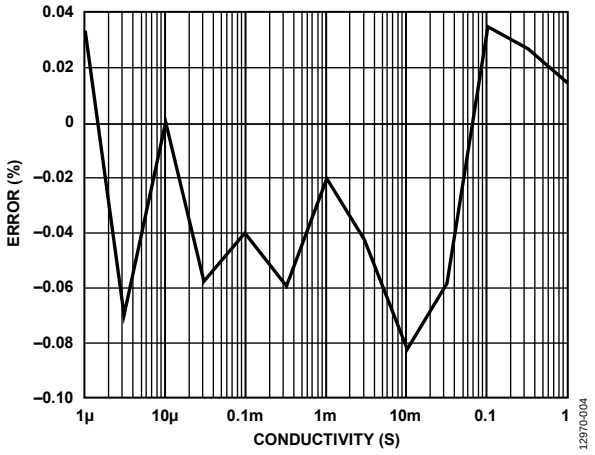

Figure 4. System Error (%) vs. Conductivity of 1 µS to 1 S

RTD Measurement

Conductivity measuring system accuracy is only as good as its temperature compensation. Because common solution temperature coefficients vary in the order of 1%/°C to 3%/°C or more, measuring instruments with adjustable temperature compensation must be used. Solution temperature coefficients are somewhat nonlinear and usually vary with the actual conductivity, as well. Therefore, calibration at the actual measuring temperature yields the best accuracy.

The ADuCM360 contains two matched, software configurable, excitation current sources. They are individually configurable to provide a current output of 10 µA to 1 mA, and matching is better than 0.5%. The current sources allow the ADuCM360 to easily perform 2-wire, 3-wire, or 4-wire measurements for either Pt100 or Pt1000 RTDs. The software also automatically detects if the RTD is Pt100 or Pt1000 during the setup procedure.

The following discussion shows simplified schematics of how the different RTD configurations operate. All mode switching is accomplished in the software, and there is no need to change the external jumper settings.

Figure 5 shows the configuration for 4-wire RTDs.

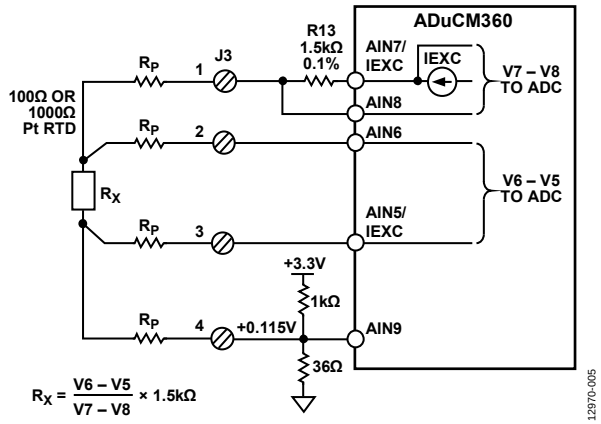

Figure 5. Configuration for 4 Wire RTD Connection

The parasitic resistance in each of the leads to the remote RTD is shown as R_P. The excitation current (IEXC) passes through a precision 1.5 kΩ resistor and the RTD. The on-chip ADC measures the voltage across the resistor (V7 – V8).

It is important that the R13 resistor and the IEXC excitation current value be chosen such that the ADuCM360 maximum input voltage at AIN7 does not exceed AVDD – 1.1 V; otherwise, the IEXC current source does not function properly.

The RTD voltage is accurately measured using the two sense leads that connect to AIN6 and AIN5. The input impedance is approximately 2 MΩ (unbuffered mode, PGA gain = 1), and the current flowing through the sense lead resistance produces minimum error. The ADC then measures the RTD voltage (V6 – V5).

The RTD resistance is then calculated as

$$R_X = \frac{V6 - V5}{V7 - V8} \times 1.5\ \text{k}\Omega \quad (8)$$

The measurement is ratiometric and does not depend on an accurate external reference voltage, only the tolerance of the 1.5 kΩ resistor. In addition, the 4-wire configuration eliminates the error associated with the lead resistances.

The ADuCM360 has a buffered or unbuffered input option. If the internal buffer is activated, the input voltage must be greater than 100 mV. The 1 kΩ/36 Ω resistor divider provides a 115 mV bias voltage to the RTD that allows buffered operation. In the unbuffered mode, Terminal 4 of J3 can be grounded and connected to a grounded shield for noise reduction.

The 3-wire connection is another popular RTD configuration that eliminates lead resistance errors, as shown in Figure 6.

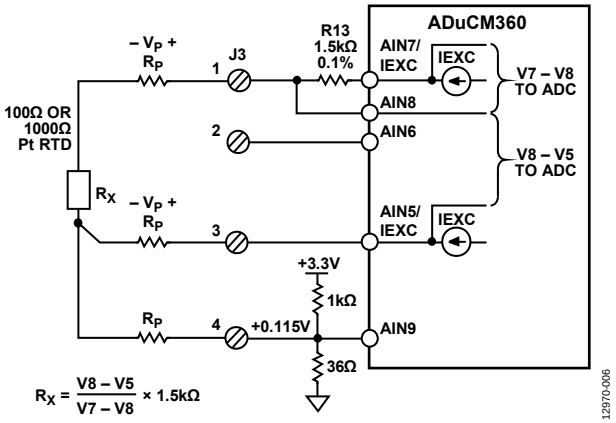

Figure 6. Configuration for 3-Wire RTD Connection

The second matched IEXC current source (AIN5/IEXC) develops a voltage across the lead resistance in series with Terminal 3 that cancels the voltage dropped across the lead resistance in series with Terminal 1. The measured V8 – V5 voltage is therefore free of lead resistance error.

Figure 7 shows the 2-wire RTD configuration where there is no compensation for lead resistance.

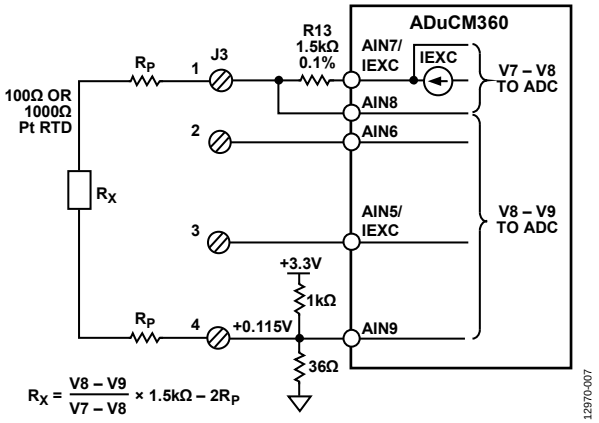

Figure 7. Configuration for 2-Wire RTD Connection

The 2-wire configuration is the lowest cost circuit and is suitable for less critical applications, short RTD connections, and higher resistance RTDs such as Pt1000.

Conductivity Theory

The resistivity, ρ, of a material or liquid is defined as the resistance of a cube of the material with perfectly conductive contacts on opposite faces. The resistance, R, for other shapes can be calculated by

$$R = \rho L/A \quad (9)$$

where:
L is the distance between the contacts.
A is the area of the contacts.

Resistivity is measured in units of Ω cm. A 1 Ω cm material has a resistance of 1 Ω when contacted on opposite faces of a 1 cm × 1 cm × 1 cm cube.

Conductance is the reciprocal of resistance, and conductivity is the reciprocal of resistivity. The unit of measurement of conductance is Siemens (S), and the unit of measurement of conductivity is S/cm, mS/cm, or µS/cm.

All aqueous solutions conduct electricity to some degree. Adding electrolytes such as salts, acids, or bases to pure water increases the conductivity (and decreases resistivity).

For the purposes of this circuit note, Y is the general symbol for conductivity measured in S/cm, mS/cm, or µS/cm. However, in many cases, the distance term is dropped for convenience, and the conductivity is simply expressed as S, mS, or µS.

A conductivity system measures conductivity by means of electronics connected to a sensor called a conductivity cell immersed in a solution, as shown in Figure 8.

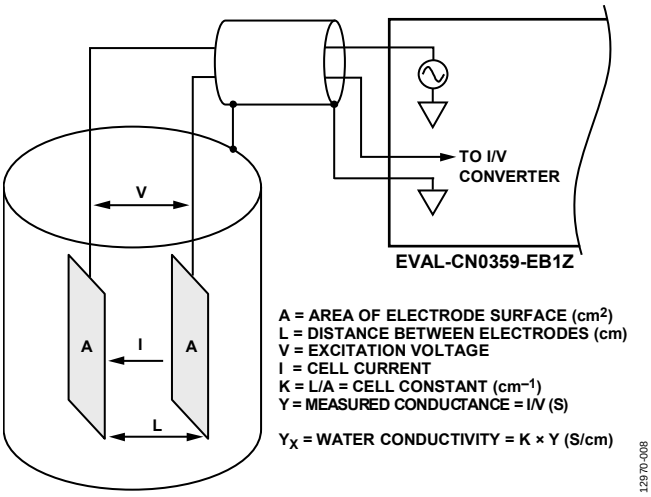

Figure 8. Interface Between Conductivity Cell and EVAL-CN0359-EB1Z

The electronic circuitry impresses an alternating voltage on the sensor and measures the size of the resulting current, which is related to the conductivity. Because conductivity has a large temperature coefficient (up to 4%/°C), an integral temperature sensor is incorporated into the circuitry to adjust the reading to a standard temperature, usually 25°C (77°F). When measuring solutions, the temperature coefficient of the conductivity of the water itself must be considered. To compensate accurately for the temperature, a second temperature sensor and compensation network must be used.

The contacting-type sensor typically consists of two electrodes that are insulated from one another. The electrodes, typically Type 316 stainless steel, titanium palladium alloy, or graphite, are specifically sized and spaced to provide a known cell constant. Theoretically, a cell constant of 1.0/cm describes two electrodes, each sized 1 cm^2 in area, and spaced 1 cm apart. Cell constants must be matched to the measurement system for a given range of operation. For instance, if a sensor with a cell constant of 1.0/cm is used in pure water with a conductivity of 1 µS/cm, the cell has a resistance of 1 MΩ. Conversely, the same cell in seawater has a resistance of 30 Ω. Because the resistance ratio is so large, it is difficult for ordinary instruments to accurately measure such extremes with only one cell constant.

When measuring the 1 µS/cm solution, the cell is configured with large area electrodes spaced a small distance apart. For example, a cell with a cell constant of 0.01/cm results in a measured cell resistance of approximately 10,000 Ω rather than 1 MΩ. It is easier to accurately measure 10,000 Ω than 1 MΩ; therefore, the measuring instrument can operate over the same range of cell resistance for both ultrapure water and high conductivity seawater by using cells with different cell constants.

The cell constant, K, is defined as the ratio of the distance between the electrodes, L, to the area of the electrodes, A:

$$K = L/A \quad (10)$$

The instrumentation then measures the cell conductance, Y:

$$Y = I/V \quad (11)$$

The conductivity of the liquid, Y_X, is then calculated:

$$Y_X = K \times Y \quad (12)$$

There are two types of conductivity cells: those with two electrodes, and those with four electrodes, as shown in Figure 9. The electrodes are often referred to as poles.

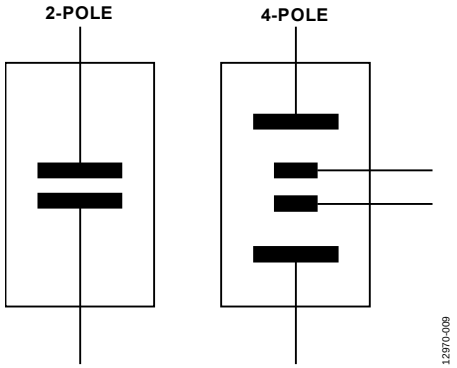

Figure 9. 2-Pole and 4-Pole Conductivity Cells

The 2-pole sensor is more suitable for low conductivity measurements, such as purified water, and various biological and pharmaceutical liquids. The 4-pole sensor is more suitable the high conductivity measurements, such as waste water and seawater analysis.

The cell constants for 2-pole cells range from approximately 0.1/cm to 1/cm, and the cell constants for 4-pole cells range from 1/cm to 10/cm.

The 4-pole cell eliminates the errors introduced by polarization of the electrodes and field effects that can interfere with the measurement.

The actual configuration of the electrodes can be that of parallel rings, coaxial conductors, or others, rather than the simple parallel plates shown in Figure 8.

Regardless of the type of cell, it is important not to apply a dc voltage to any electrode, because ions in the liquid will accumulate on the electrode surface, thereby causing polarization, measurement errors, and damage to the electrode.

Take special care with sensors that have shields, as in the case of coaxial sensors. The shield must be connected to the same potential as the metal container holding the liquid. If the container is grounded, the shield must be connected to Pin 5 of J5, the circuit board ground.

The final precaution is not to exceed the rated excitation voltage or current for the cell. The CN-0359 circuit allows programmable excitation voltages from 100 mV to 10 V, and the R23 (1 kΩ) series resistor limits the maximum cell current to 10 mA.

Power Supply Circuits

To simplify system requirements, all the required voltages (±15 V and +3.3 V) are generated from a single 4 V to 7 V supply, as shown in Figure 10.

The ADP2300 buck regulator generates the 3.3 V supply for the board. The design is based on the downloadable ADP230x Buck Regulator Design Tool.

The ADP1613 boost regulator generates a regulated +15 V supply and an unregulated −15 V supply. The −15 V supply is generated with a charge pump. The design is based on the ADP161x Boost Regulator Design Tool.

Details regarding the selection and design of power supplies are available at www.analog.com/ADIsimPower.

Use proper layout and grounding techniques to prevent the switching regulator noise from coupling into the analog circuits. See the *Linear Circuit Design Handbook*, the *Data Conversion Handbook*, the MT-031 Tutorial, and the MT-101 Tutorial for further details.

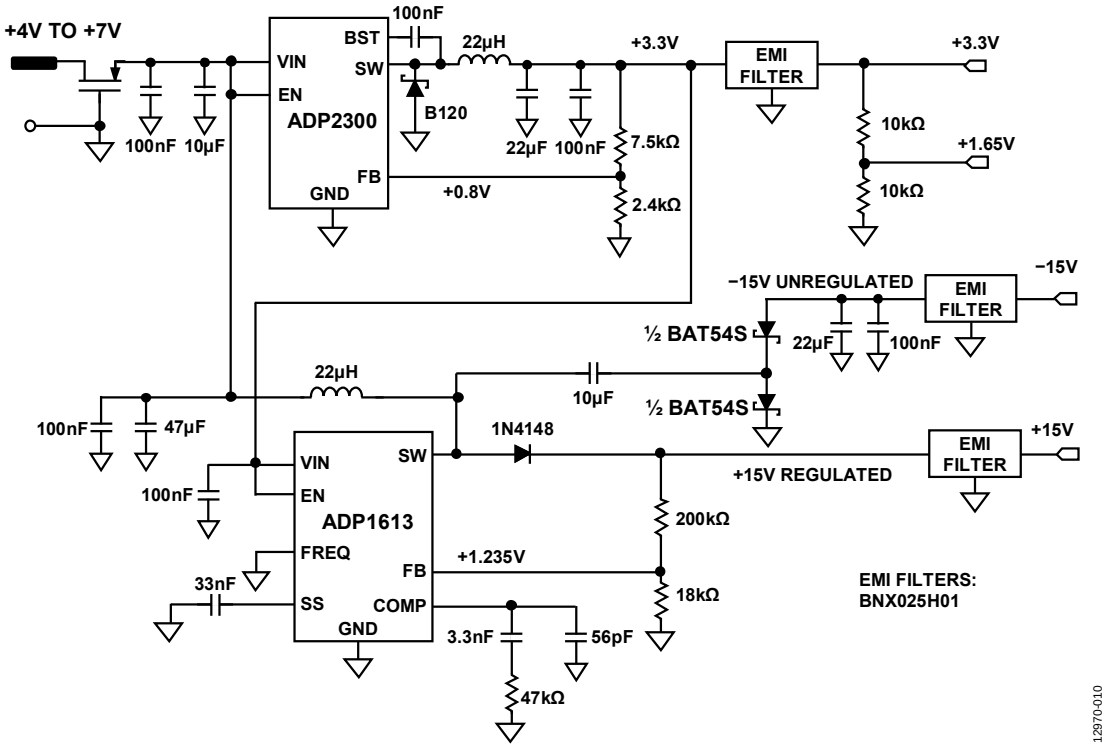

Figure 10. Power Supply Circuits

Figure 11 shows the LCD backlight driver circuit.

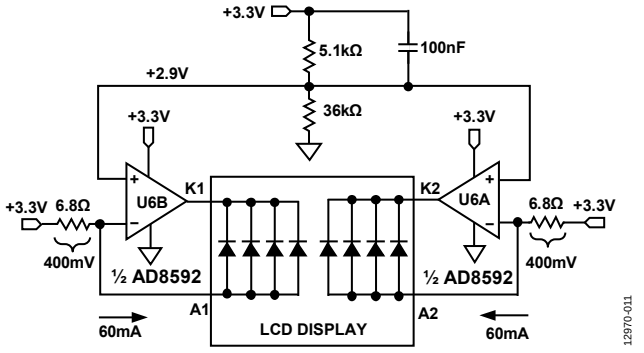

Figure 11. LCD Backlight Drivers

Each half of the AD8592 op amp acts as a 60 mA current source to supply the LCD backlight currents. The AD8592 can source and sink up to 250 mA, and the 100 nF capacitor ensures a soft startup.

Software Operation and User Interface

The EVAL-CN0359-EB1Z comes preloaded with the code required to make the conductivity measurements. The complete system hardware and software operation can be found in the CN-0359 User Guide at www.analog.com/CN0359-UserGuide.

The CN-0359 user interface is intuitive and easy to use. All user inputs are from a dual function push button/rotary encoder knob. The encoder knob can be turned clockwise or counterclockwise (no mechanical stop), and can also be used as a push button.

Figure 12 is a photo of the EVAL-CN0359-EB1Z board that shows the LCD display and the position of the encoder knob.

Figure 12. Photo of EVAL-CN0359-EB1Z Board Showing Home Screen in Measurement Mode

After connecting, the conductivity cell and the RTD the board are powered up. The LCD screen appears as shown in Figure 12.

Push the encoder knob to enter the setting menu, and then input the **EXC Voltage**, **EXC Frequency**, **TEMP Coefficient**, and **Cell Constant**, as shown in Figure 13.

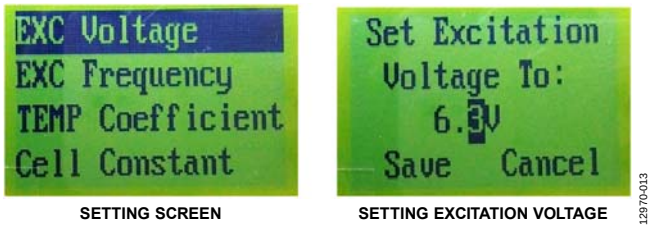

Figure 13. LCD Display Screens

Rotating the knob moves the cursor up and down through the various parameters.

Set the cursor to **EXC Voltage** and push the knob until it clicks**.** Position the cursor over the first digit in the number to be set by rotating the knob. Push the button, and the cursor blinks. Change the number by rotating the knob, and push the knob when the desired number is reached. After setting all the digits in the number, position the cursor on **Save** and push the button to save the setting.

Continue the process and set the **EXC Frequency**, **TEMP Coefficient**, and **Cell Constant**.

After setting all the constants, select **RETURN TO HOME** and push the knob. The system is now ready to make measurements.

If numbers are entered that are outside the allowable range, the buzzer sounds.

If the conductivity cell is incorrectly connected, the screen displays **Sensor Incorrect**.

If the RTD is incorrectly connected, the screen displays **RTD Incorrect use 25°C**. The system can still make measurements without the RTD connected, but uses 25°C as the compensation temperature.

COMMON VARIATIONS

The system shown in the CN-0359 uses the ADuCM360 precision analog microcontroller for a highly integrated conductivity measurement.

If the user desires a discrete ADC, the AD7794 24-bit, Σ-Δ ADC is a good choice.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0359-EB1Z circuit board, an external power supply, conductivity cell, and an RTD.

Equipment Needed

The following equipment is needed:

- The EVAL-CN0359-EB1Z circuit board
- A 6 V power supply or wall wart (EVAL-CFTL-6V-PWRZ)
- A conductivity cell
- Pt100 or Pt1000 2-wire, 3-wire, or 4-wire RTD (if the RTD is not connected, the conductivity measurement is referenced to 25°C)

Setup

Take the following steps to set up the circuit for evaluation:

1. Connect the conductivity cell as follows:
   a. 4-wire cell: connect an outside current electrode to J5 Pin 1 and the closest inner voltage electrode to J5 Pin 2. Connect the second outside current electrode to J5 Pin 4 and the closest inner voltage electrode to Pin 3.
   b. 2-wire cell: connect one electrode to J5 Pin 1 and Pin 2 and connect the second electrode to J5 Pin 3 and Pin 4.
   c. If the conductivity cell has a shield, connect it to J5 Pin 5.
2. Connect the RTD as follows (if used):
   a. 4-wire RTD (see Figure 5): connect the positive current excitation wire to J3 Pin 1 and the positive voltage sense wire to J3 Pin 2. Connect the negative current excitation wire to J3 Pin 4 and the negative voltage sense wire to J3 Pin 3.
   b. 3-wire RTD (see Figure 6): connect the positive current excitation wire to J3 Pin 1. Connect the negative current excitation wire to J3 Pin 4. Connect the negative voltage sense wire to J3 Pin 3.
   c. 2-wire RTD (see Figure 7): connect one RTD wire to J3 Pin 1 and the other wire to J3 Pin 4.
   d. If the RTD wires are shielded, connect the shield to J5 Pin 5.
3. Connect the 6 V power supply (EVAL-CFTL-6V-PWRZ) to J1 of the EVAL-CN0359-EB1Z circuit board.
4. Turn on the power by connecting the EVAL-CFTL-6V-PWRZ, and then push the button on the EVAL-CN0359-EB1Z circuit board.
5. Follow the procedure previously described in the Software Operation and User Interface section and enter the following parameters: **EXC Voltage**, **EXC Frequency**, **TEMP Coefficient**, and **Cell Constant.**
6. Return to the main screen and wait for the ADuCM360 to flush the buffers and display the conductivity and the temperature. If the screen shows an error and the buzzer beeps more than 20 times, check the sensor connections.

Connectivity for Prototype Development

The EVAL-CN0359-EB1Z is designed to be powered with the EVAL-CFTL-6V-PWRZ 6 V power supply. The EVAL-CN0359-EB1Z requires only the power supply and the external conductivity cell and RTD for operation.

The EVAL-CN0359-EB1Z also has an RS-485 connector, J2, that allows an external PC to interface with the board. Connector J4 is a JTAG interface for programming and debugging the ADuCM360.

Figure 14 is a typical PC connection diagram showing an RS-485 to RS-232 adapter.

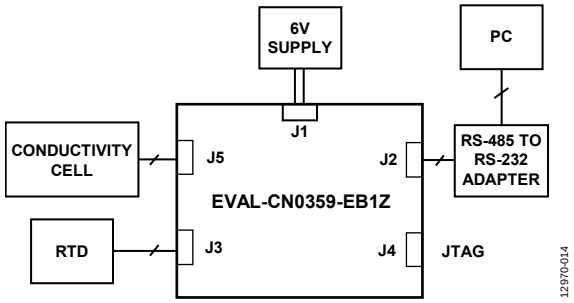

Figure 14. Test Setup Functional Diagram

LEARN MORE

CN-0359 Design Support Package:
www.analog.com/CN0359-DesignSupport

ADIsimPower Design Tool. Analog Devices

Linear Circuit Design Handbook. Analog Devices/Elsevier.

Op Amp Applications Handbook. Analog Devices/Elsevier.

The Data Conversion Handbook. Analog Devices/Elsevier.

A Designer's Guide To Instrumentation Amplifiers, 3rd Edition. Analog Devices.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*. Analog Devices.

MT-101 Tutorial. *Decoupling Techniques*. Analog Devices.

"Section 7: Temperature Sensors" in *Sensor Signal Conditioning*. Analog Devices.

Data Sheets and Evaluation Boards

AD8253 Data Sheet

ADA4627-1 Data Sheet

ADA4000-1 Data Sheet

ADA4638-1 Data Sheet

ADA4528-2 Data Sheet

ADA4077-2 Data Sheet

AD8592 Data Sheet

AD8542 Data Sheet

ADuCM360 Data Sheet

ADP2300 Data Sheet

ADP1613 Data Sheet

ADG1211 Data Sheet

ADG1419 Data Sheet

ADM3483 Data Sheet

REVISION HISTORY

9/2016—Rev. A to Rev. B

Change to Evaluation and Design Support Section.....1
Changes to Figure 3.....3
Changes to Software Operation and User Interface Section and Figure 12.....8

11/2015—Rev. 0 to Rev. A

Change to Setup Section.....9

1/2015—Revision 0: Initial Version

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0363.

Devices Connected/Referenced	
AD7175-2	24-Bit, 250 kSPS, Sigma-Delta ADC with 20 µs Settling and True Rail-to-Rail Buffers
ADA4528-1	Precision, Ultralow Noise, RRIO, Zero-Drift Op Amp
AD8615	Precision, 20 MHz, CMOS, Rail-to-Rail Input/Output Operational Amplifier
AD5201	33-Position Digital Potentiometer
ADA4805-1	0.2 µV/°C Offset Drift, 105 MHz Low Power, Low Noise, Rail-to-Rail Op Amp
ADG633	CMOS, ±5 V/+5 V/+3 V, Triple SPDT Switch
ADG733	CMOS, 2.5 V Low Voltage, Triple SPDT Switch
ADG704	CMOS, Low Voltage, 4 Ω, 4-Channel Multiplexer
ADG819	0.5 Ω, CMOS,1.8 V to 5.5 V, 2:1 Mux/SPDT Switch

Dual-Channel Colorimeter with Programmable Gain Transimpedance Amplifiers and Digital Synchronous Detection

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0363 Circuit Evaluation Board (EVAL-CN0363-PMDZ)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a dual-channel colorimeter featuring a modulated light source transmitter, programmable gain transimpedance amplifiers on each channel, and a very low noise, 24-bit Σ-Δ analog-to-digital converter (ADC). The output of the ADC connects to a standard FPGA mezzanine card. The FPGA takes the sampled data from the ADC and implements a synchronous detection algorithm.

By using modulated light and digital synchronous detection rather than a constant (dc) source, the system strongly rejects any noise sources at frequencies other than the modulation frequency, providing excellent accuracy.

The dual-channel circuit measures the ratio of light absorbed by the liquids in the sample and reference containers at three different wavelengths. This measurement forms the basis of many chemical analysis and environmental monitoring instruments used to measure concentrations and characterize materials through absorption spectroscopy.

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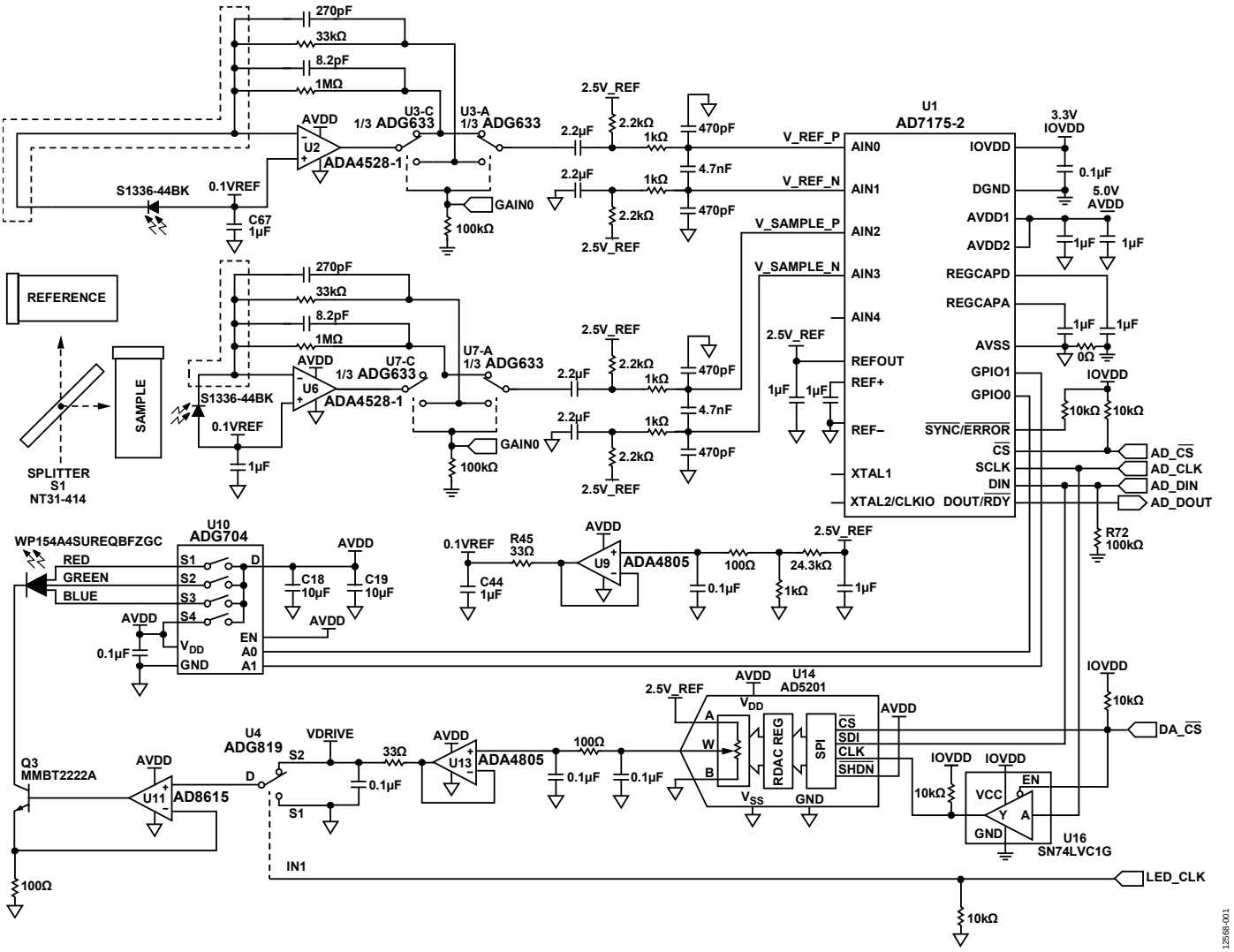

Figure 1. Dual-Channel Colorimeter with Programmable Gain Transimpedance Amplifiers and Lock-In Amplifiers (Simplified Schematic: All Connections and Decoupling Not Shown)

CIRCUIT DESCRIPTION

A clock set to a user-programmable frequency modulates one of the three LED colors with a constant current driver built around the AD8615 op amp, the ADG819 switch, and the AD5201 digital potentiometer. The beam splitter sends half the light through the sample container and half through the reference container. The ADA4528-1, configured as a transimpedance amplifier, then converts the photodiode current into an output voltage square wave, whose amplitude is proportional to the light transmitted through the sample or reference containers. The transimpedance amplifiers use the ADG633 single-pole, double-throw (SPDT) switches to select one of two transimpedance gains. The AD7175-2 Σ-Δ ADC samples the voltage and sends the digital data to an FPGA for digital demodulation.

The FPGA implements synchronous demodulation by first synchronizing a numerically generated sine wave with the LED clock, and then multiplying this sine wave with the sampled ADC data. In addition, a 90° shifted version of this sine wave is also multiplied with the ADC data to obtain the quadrature component of the modulation signal. The result of these operations are two low frequency demodulated signals representing the in-phase and quadrature components of the received light on each channel, respectively. A narrow FIR low pass filter removes all other frequency components, making it easy to calculate the magnitude and phase shift of the amplitude measured at the photodiodes, while rejecting any light or electrical noise at frequencies different from the LED clock. The ADG704 multiplexer connects the power rail to one of the three LED colors, allowing the user to select the test wavelength through a 2-bit address. The AD8615 and an NPN transistor make up a simple current source, with the LED current given by

$$I_{LED} = V_{NON-INVERTING} / R_{EMITTER}$$

where:

$V_{NON-INVERTING}$ is the voltage at the non-inverting input of the AD8615.

$R_{EMITTER}$ is the value of the resistor connected to the emitter of Transistor Q3.

The ADG819 SPDT switch is connected to the set point voltage and to ground, and its control pin is connected to the reference clock. As the clock oscillates between high and low, the set point to the current source changes from 0 mA to the desired output current, thereby generating a square wave signal.

The AD5201 digital potentiometer acts as a programmable resistor divider from the 2.5 V reference, allowing 33 different current output settings for the LED current.

Both the sample and reference containers receive one-half of the LED light energy, and absorb different amounts of light depending on the type and concentration of material in each container. The photodiode on the opposite side of each container generates a small current proportional to the amount of light received.

The first stage of each receiver channel consists of an ADA4528-1 op amp configured as a transimpedance amplifier to convert the output current of the photodiode to a voltage. The ADA4528-1 is an auto-zero amplifier resulting in negligible offset, no 1/f noise, and very low broadband noise (5.9 nV/√Hz). Like all auto-zero amplifiers, there is a noise spike at the auto-zero frequency. For the ADA4528-1, the frequency is approximately 200 kHz, but the circuit signal bandwidth rolls off well before then.

The input bias current of the op amp multiplied by the feedback resistor value appears at the output as an offset voltage. The input offset of the op amp voltage appears at the output with a gain dependent on the feedback resistor and the shunt resistance of the photodiode. In addition, any op amp input voltage offset appears across the photodiode, causing the dark current of the photodiode to increase. The ADA4528-1 is therefore ideally suited for this application because of its low offset voltage (2.5 µV).

Figure 2 shows a typical transimpedance amplifier with a single feedback resistor and its ideal transfer function.

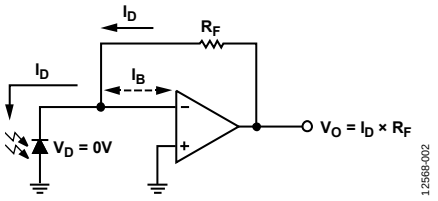

Figure 2. Transimpedance Amplifier Transfer Function

Because some solutions under test can have very strong absorption characteristics, it is sometimes necessary to use large feedback resistors to measure the very small currents generated by the photodiode, while at the same time being able to measure large currents corresponding to highly diluted solutions. To address this challenge, the photodiode amplifiers of Figure 1 include two different selectable gains. One gain is set at 33 kΩ, while the other is set at 1 MΩ. Using a single SPDT switch connected to the output of the op amp to switch feedback resistors results in transimpedance gain error due to the on resistance of the ADG633. To avoid this problem, Figure 3 shows a better configuration where the ADG633 switch inside the feedback loop selects the desired resistor, while a second switch connects the next stage of the system to the selected feedback loop. The voltage at the output of the amplifier is

$$V_{TIA\ OUTPUT} = I_{PHOTODIODE} \times R_{FEEDBACK}$$

instead of

$$V_{TIA\ OUTPUT} = I_{PHOTODIODE} \times (R_{FEEDBACK} + R_{ON\ ADG633})$$

which represents a gain error. However, because one of the ADG633 devices is outside the feedback loop, the output impedance of this stage is the on resistance of the ADG633 (typically 52 Ω), rather than the very low output impedance associated with the output of an op amp in closed-loop operation. The error due to the leakage current of the ADG633 (5 pA typical) is negligible.

Even the best rail-to-rail output amplifiers like the ADA4528-1 cannot swing their output completely to the rails. In addition, the input offset voltage on the ADA4528-1, although very small, can be negative. Rather than including a negative power supply to guarantee that the amplifier never clips, and that it can drive to 0.0 V, an ADA4805-1 op amp provides a buffered 100 mV voltage to bias the anode of the photodiode and the ADA4528-1. The ADA4805-1 is ideally suited as a reference voltage buffer because it maintains unity gain stability when driving large capacitive loads used for decoupling. A second ADA4805-1 is also used to buffer the output of the AD5201 digital potentiometer that sets the LED current.

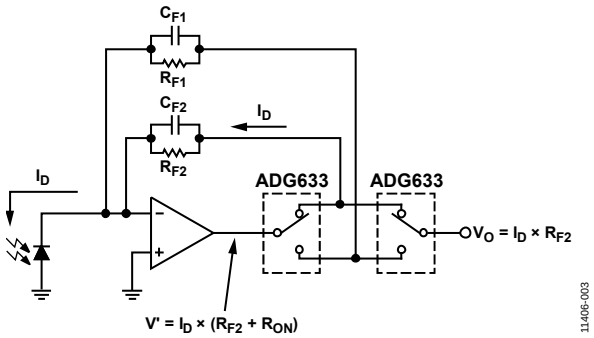

Figure 3. Programmable Gain Transimpedance Amplifier

The output voltage of the photodiode amplifier swings between 0.1 V and 5.0 V. For the 33 kΩ range, the 4.9 V output span corresponds to a full-scale photodiode current of 148.5 µA. For the 1 MΩ range, it corresponds to a full-scale photodiode current of 4.9 µA. When operating in the 1 MΩ gain setting, it is important to shield the photodiode from external light to prevent the amplifier from saturating. Although the synchronous detection scheme described in the following sections strongly attenuates any frequencies that are not synchronous with the LED clock, the detection scheme cannot function properly if the ADC is returning saturated data.

The gain setting for each channel is independently selectable through the FPGA board.

ADC Sampling Rate and Modulation Frequency Selection

The AD7175-2 ADC is configured with the sinc5+sinc1 filter with an output data rate of 250 kSPS to sample both channels with single-cycle settling. This configuration results in an effective sampling rate of 25 kSPS on each channel (data for each channel is output every 40 µs). Any frequencies above 12.5 kHz (such as the odd harmonics of the square wave modulation) alias back into the passband of the ADC; however, the synchronous demodulation stage rejects these frequencies as long as they do not fall right on top of the modulation frequency. To avoid aliases of the modulation waveform folding back into its fundamental, select a modulation frequency according to the following relationship:

$$F_{MODULATION} = \frac{F_{SAMPLE}}{2 \times n + 0.5}$$

where:
$F_{MODULATION}$ is the modulation frequency.
F_{SAMPLE} is the ADC effective output data rate.
n is an integer (corresponding to the harmonics of the modulation frequency).

For example, in this system, the effective output data rate is 25 kSPS; therefore, if a modulation frequency of approximately 1 kHz is desired, the frequency must be 1020 Hz (n = 12) or 943 Hz (n = 13) to avoid alias problems. Using this method to select a modulation frequency eliminates the need for sharp anti-aliasing filters on the front end.

Digital Synchronous Detection

Rather than implementing synchronous detection in the hardware (see the Circuit Note CN-0312), this circuit takes the time-sampled data and uses an FPGA to implement digital synchronous detection. Figure 4 shows a representation of the digital synchronous detection block implemented in the FPGA. The FPGA generates the ac excitation signal to drive the LEDs, and a numerically generated sine wave locks to this signal in a digital phase-locked loop. The input signal is multiplied with the digital sine wave and with a 90° shifted version, resulting in two low frequency demodulated signals proportional to the in-phase and quadrature components of the input signal at the modulation frequency. As shown in Figure 4, the magnitude is the root of the sum of the squares of these two components. For more information on this demodulation technique, see the Learn More section.

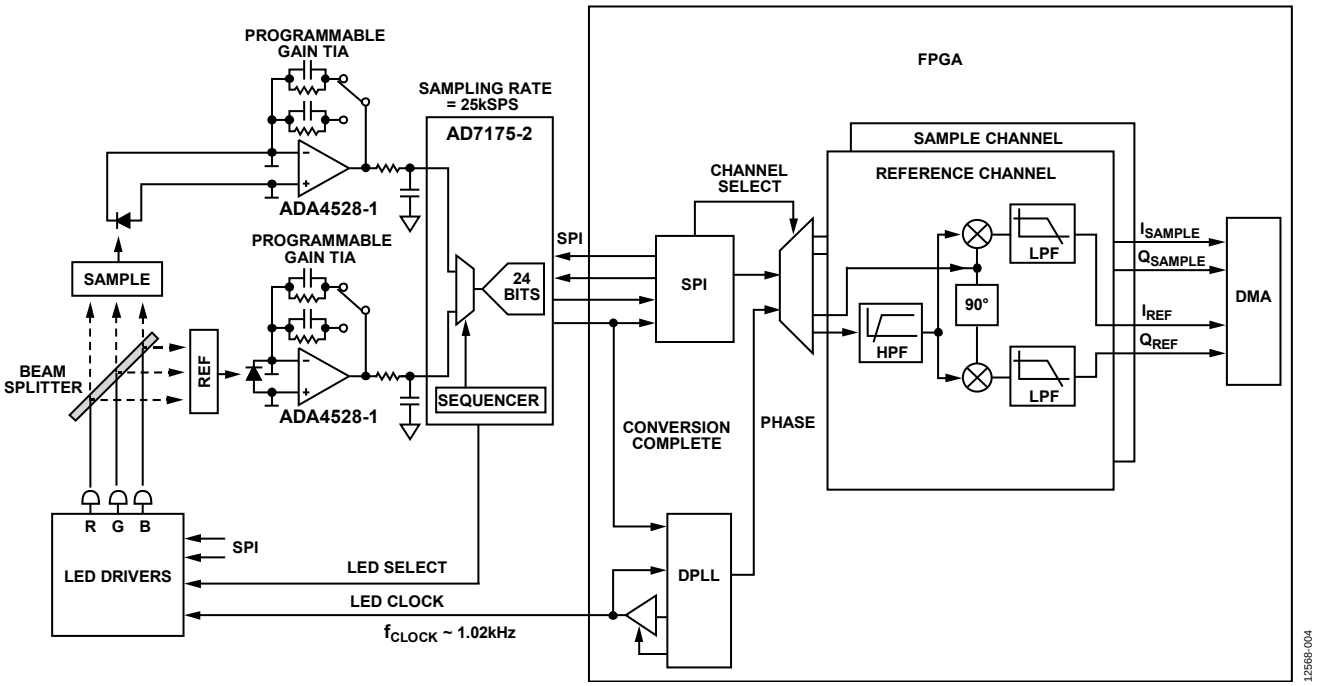

Figure 4. System Block Diagram Including FPGA Synchronous Detector

Power Supplies

The EVAL-CN0363-PMDZ board is powered from an external 6 V to 12 V dc supply. The analog portion of the circuit is supplied by AVDD = 5 V from an ADP7102 low dropout regulator. The digital portion of the circuit is supplied by IOVDD = 3.3 V developed from an ADP1720 low dropout regulator. Alternatively, IOVDD can be supplied from the PMOD connector, VCC, via a link option.

The 2.5 V reference voltage is supplied by the internal 2.5 V reference of the AD7175-2 ADC.

Circuit Performance Measurements

To verify the noise performance of the system, acquire data with all of the LEDs disabled. The synchronous detector still operates at the LED clock frequency, but no light synchronous to this clock is detected; therefore, it removes all dc and ac signals. Table 1 shows the noise-free bit performance.

Table 1. Noise-Free Bit Performance[1]

	ADC Output		Final Filtered Output	
Gain	Reference Channel ADC	Sample Channel ADC	Reference Channel Output	Sample Channel Output
1 MΩ	12.46	12.85	15.91	15.50
33 kΩ	15.58	15.59	18.77	18.85

[1] Sample rate = 25 kSPS, excitation frequency = 1020 Hz, output filter bandwidth = 100 Hz.

COMMON VARIATIONS

Changing the values of the feedback resistors on the photodiode amplifiers changes the amplifier gains, which is an easy way to customize the circuit for a specific application with different light levels. However, the compensation capacitor must also be changed to maintain the same bandwidth and to guarantee that the amplifier is stable.

For systems measuring extremely low levels of light, the cutoff frequency of the synchronous detector's output low-pass filter can be set to a much lower frequency for the highest performance at the expense of long measurement cycle times.

Because the light output of the LEDs changes with temperature, the system makes measurements as a ratio of the sample and the reference channels. The photodiodes have a gain tolerance of up to ±11%; therefore, even ratiometric variations include some drift as the LED output changes with time and temperature. The addition of an optical feedback network to control the LED light output reduces light variations with temperature and makes possible accurate single-ended measurements.

Rather than modulate the LEDs with a square wave, a DDS or PWM in the FPGA can be used to generate a sine wave modulation. Sine wave modulation reduces the harmonic content of the signal, makes filtering easier, and results in lower noise.

CIRCUIT EVALUATION AND TEST

A complete set of documentation for the EVAL-CN0363-PMDZ board including schematics, layout drawings, Gerber files, and bill of materials can be found in the CN-0363 Design Support Package at www.analog.com/CN0363-DesignSupport.

The CN-0363 evaluation software communicates with the FPGA development board to capture and analyze data from the EVAL-CN0363-PMDZ circuit board.

Equipment needed

- EVAL-CN0363-PMDZ circuit evaluation board
- 6 V to 12 V dc, 500 mA power supply or wall wart
- FPGA development board (such as ZedBoard) and a 12 V power supply
- 8 GB SD card, supplied with EVAL-CN0363-PMDZ
- USB keyboard and mouse combination
- HDMI monitor (HD only)
- CN-0363 evaluation software (see the CN-0363 User Guide)
- Distilled water and test liquid samples

Getting Started

Detailed operation of the evaluation hardware and software is available in the CN-0363 User Guide.

HDL software and drivers are provided in the software link to support various FPGA development platforms, such as the Avnet ZedBoard.

The development platforms require an SD card, which is supplied with the CN-0363 hardware. The SD card has been properly partitioned, but must be updated with the latest images. The procedure is described the CN-0363 User Guide.

Functional Diagram

Figure 5 shows a functional block diagram of the test setup.

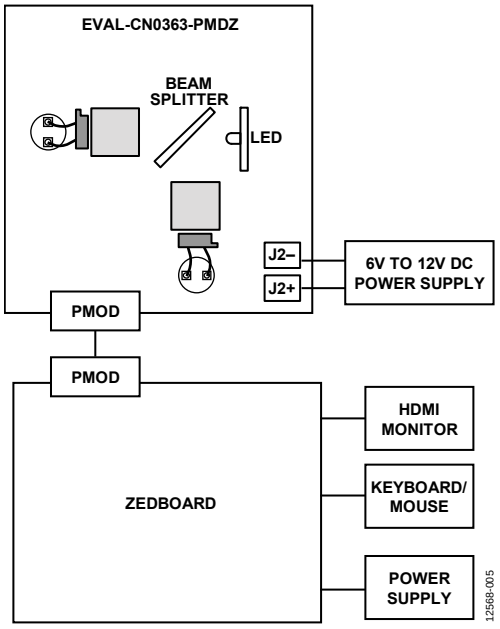

Figure 5. Evaluation System Functional Diagram

Setup

Set up the system as follows:

1. Connect the PMOD cable between the EVAL-CN0363-PMDZ and the ZedBoard, and connect a 6 V to 12 V dc power supply to the J2 power connector. Do not turn on the supply at this time.
2. Connect a USB keyboard/mouse, HDMI monitor, and power supply to the ZedBoard. Do not turn on the supply at this time.

Test

Initialize the system as follows:

1. Turn on the power to the EVAL-CN0363-PMDZ board.
2. Turn on the power to the ZedBoard.
3. Allow the system to boot.
4. If needed, enter the appropriate keyboard commands described in the CN-0363 User Guide.

Calibration

The system requires an initial calibration to compensate for misalignment between the LEDs, beam splitter, and photodiodes, as well as to compensate for any mismatch in the response of the photodiodes. To calibrate the system, fill the two containers with distilled water and insert them into the square holes in the PCB. It is also recommended that the photodiodes be shielded from ambient light during the calibration procedure.

Start the automatic calibration procedure in the software; from the **Menu** bar, open the **Calibration** dialog box, and click **Calibrate**. The full calibration procedure process takes a few seconds, and the progress bar indicates the current step. When the calibration is complete, the calibration values are updated. Calibration removes the zero offset and sets the proper gain for each channel. The calibration data also includes a multiplication factor, K, that expresses the relative relationship between the reference and sample channel values at full-scale excitation.

The software calculates the K multiplier for each LED color, so that

$$\frac{V_{REFERENCE\_CHANNEL}}{V_{SAMPLE\_CHANNEL}} K = 1$$

where K is the calculated calibration constant.

After performing a calibration, the software uses the calibration constants in all subsequent measurements.

In the field of spectroscopy, absorbance is defined as the logarithmic ratio of the light reaching the material under test to the light transmitted through the material. Beer-Lambert's law states that the amount of light transmitted through a material decreases exponentially with increasing path length and concentration. By defining absorbance as a logarithm, absorbance is directly proportional to the concentration of the material (given a constant path length).

$$Absorbance = \log 10\left(\frac{V_{REFERENCE}}{V_{SAMPLE}} K\right)$$

For a simple way to verify this theory without resorting to harmful chemicals, measure the concentration of dye used for food coloring. Figure 6 shows experimental results from different concentrations of Yellow #5 dye when measured with the EVAL-CN0363-PMDZ.

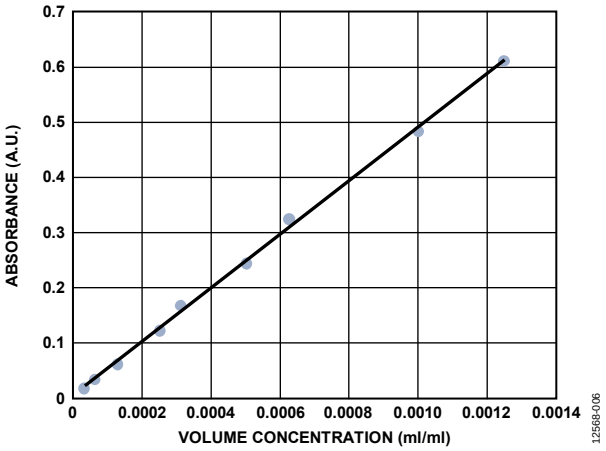

Figure 6. Absorbance Line for Yellow #5 Dye Under 465 nm (Dominant Wavelength) Light

Yellow solutions strongly absorb blue light; therefore, the measurements were taken using the blue (465 nm dominant wavelength) LED as the source. The x-axis shows the volume concentration (which is in terms of milliliters of dye per milliliter of water, hence unitless), and the y-axis shows the absorbance. As predicted by Beer-Lambert's law, the absorbance varies linearly with concentration.

Analyzing a Sample

Click the **Analyze Sample** button in the **Automated Data Collection** tab (see Figure 7) to perform an automated sample analysis that cycles through all three colors and calculates the absorbance factor for each. The analysis takes a few seconds, and a progress bar is updated to indicate the current step. When the process is complete, the absorbance values are displayed. It is then possible to either try to match the sample to an existing sample from the sample library or to save the sample into the sample library for future use.

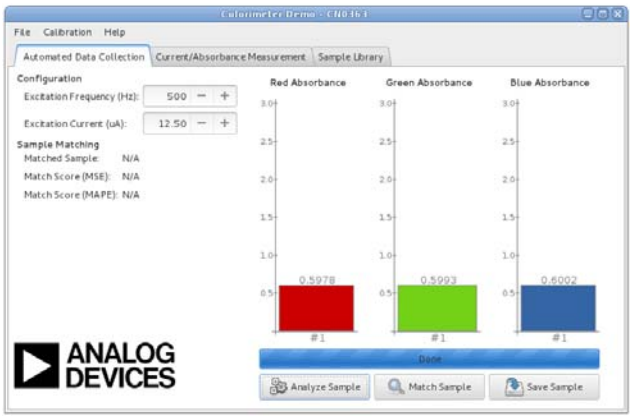

*Figure 7. **Automated Data Collection** Tab Display*

Current/Absorbance Measurement and Manual Settings

The **Current/Absorbance Measurement** tab gives direct manual access to the LED and gain controls, and allows the user to view the raw data (see Figure 8). The following parameters can be set: **Excitation Frequency**, **Excitation Current**, **LED** (**Red**, **Green**, or **Blue**), **Reference Channel Gain**, and **Sample Channel Gain**.

If these values are modified, the initial default values can be restored by running the automatic calibration procedure.

Figure 8. ***Current/Absorbance Measurement*** *Tab Display*

Sample Library

The **Sample Library** tab (see Figure 9) allows the user to manage and compare previously saved sample data. On the left-hand side is a list of all samples. On the right-hand side are the absorbance values for the currently selected samples.

It is possible to select multiple samples by holding down the CTRL key. This feature can be used to directly compare the absorbance of multiple samples to each other. Samples can also be removed from the library by selecting the sample and then clicking **Remove**. A sample that has been removed from the library cannot be restored.

A photo of the EVAL-CN0363-PMDZ board is shown in Figure 10.

Figure 9. ***Sample Library*** *Tab Display*

Figure 10. Photo of EVAL-CN0363-PMDZ

LEARN MORE

CN-0363 Design Support Package: www.analog.com/CN0363-DesignSupport

Orozco, Luis. "Synchronous Detectors Facilitate Precision, Low-Level Measurements." *Analog Dialogue 48-11*, November 2014.

Orozco, Luis. "Programmable-Gain Transimpedance Amplifiers Maximize Dynamic Range in Spectroscopy Systems." *Analog Dialogue 47-05*, May 2013.

Kester, Walt, Scott Wurcer, and Chuck Kitchin. *High Impedance Sensors, Practical Design Techniques for Sensor Signal Conditioning*, Section 5. 1999.

Skoog, Douglas A., F. James Holler, and Stanley R. Crouch. "An Introduction to Spectrometric Methods." *Instrumental Analysis.* USA: Brooks/Cole, Cengage Learning, 2007.

Data Sheets and Evaluation Boards

AD7175-2 Data Sheet

ADA4528-1 Data Sheet

AD8615 Data Sheet

AD5201 Data Sheet

ADA4805-1 Data Sheet

ADG633 Data Sheet

ADG733 Data Sheet

ADG704 Data Sheet

ADG819 Data Sheet

REVISION HISTORY

5/15—Revision 0: Initial Version

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0365.

Devices Connected/Referenced	
AD7981	High Temperature, 16-Bit, 600 kSPS PulSAR ADC
AD8634	High Temperature, Low Power, Dual Operational Amplifier
ADR225	High Temperature, Low Power Reference

16-Bit, 600 kSPS, Low Power Data Acquisition System for High Temperature Environments

EVALUATION AND DESIGN SUPPORT

Evaluation Boards

CN-0365 Circuit Evaluation Board (EVAL-CN0365-PMDZ)
System Demonstration Platform (EVAL-SDP-CB1Z)
PMOD to SDP Interposer Board (SDP-PMD-IB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

A growing number of applications require data acquisition systems that must operate reliably at very high ambient temperature environments, such as downhole oil and gas drilling, avionics, and automotive. The circuit shown in Figure 1 is a 16-bit, 600 kSPS successive approximation analog-to-digital converter (ADC) system using devices rated, characterized, and guaranteed at 175°C. Because many of these harsh environment applications are battery-powered, the signal chain has been designed for low power consumption while still maintaining high performance.

This circuit uses the AD7981, a low power (4.65 mW at 600 kSPS), high temperature PulSAR® ADC, driven directly from the AD8634 high temperature, low power op amp. The AD7981 ADC requires an external voltage reference between 2.4 V and 5.1 V, and in this application, the voltage reference chosen is the micropower ADR225 precision 2.5 V reference, which is also qualified for high temperature operation and has a very low quiescent current of 60 µA maximum at 210°C.

All of the ICs in this design have packaging specially designed for high temperature environments, including monometallic wire bonds. In addition, this reference design describes the selection of the passive components, printed circuit board (PCB) materials, and construction techniques to enable operation at these extreme temperatures. A complete design support package including bill of materials, schematic, assembly, and layout files is also available.

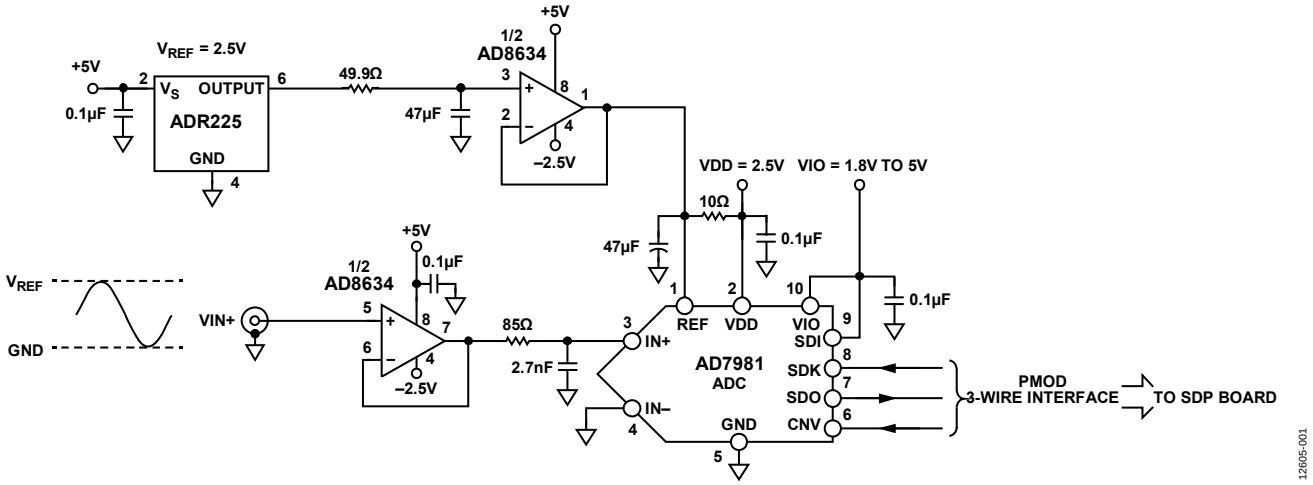

Figure 1. High Temperature Data Acquisition System (Simplified Schematic: All Connections and Decoupling Not Shown)

Rev. 0

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CIRCUIT DESCRIPTION

Analog to Digital Converter

The heart of this circuit is the AD7981, a 16-bit, low power, single supply ADC that uses a successive approximation architecture (SAR) and is capable of sampling up to 600 kSPS. As shown in Figure 1, the AD7981 uses two power supply pins: a core supply, VDD, and a digital input/output interface supply, VIO. The VIO pin allows a direct interface with any logic between 1.8 V and 5.0 V. The VDD and VIO pins can also be tied together to save on the number of supplies needed in the system, and they are independent of power supply sequencing.

The AD7981 powers down automatically between conversions to save power. Therefore, the power consumption scales linearly with the sampling rate, making the ADC well suited for both high and low sampling rates (even as low as a few Hz) and enables very low power consumption for battery-powered systems. Additionally, oversampling techniques can be used to increase the effective resolution for low speed signals.

The AD7981 has a pseudo differential analog input structure that samples the true differential signal between the IN+ and IN− inputs and rejects the signals common to both inputs. The IN+ input can accept the unipolar, single-ended input signal from 0 V to V_{REF}, and the IN− input has a restricted range of GND to 100 mV. The pseudo differential input of AD7981 simplifies the ADC driver requirement and lowers power dissipation. The AD7981 is available in a 10-lead MSOP rated for 175°C. A simplified connection diagram is shown in Figure 2.

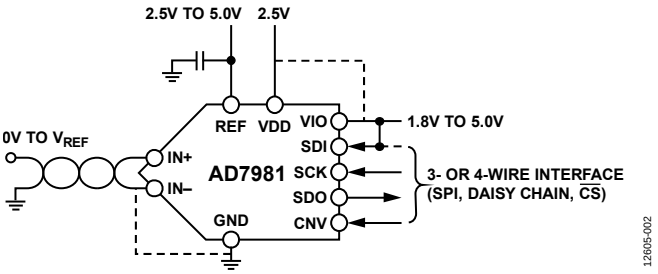

Figure 2. AD7981 Connection Diagram

ADC Driver

The input of AD7981 can be driven directly from low impedance sources; however, high source impedances significantly degrade the ac performance, especially total harmonic distortion (THD). Therefore, it recommended to use an ADC driver or op amp, such as the AD8634, to drive the input of the AD7981 as shown in Figure 3. At the start of the acquisition time, the switch closes, and the capacitive DAC injects a voltage glitch (kickback) on the ADC input. The ADC driver helps to settle this kickback as well as to isolate it from the signal source.

The low power (1.3 mA/amplifier) AD8634 dual precision op amp is suited for this task because its excellent dc and ac specifications are a good fit for sensor signal conditioning and elsewhere in the signal chain. While the AD8634 has rail-to-rail outputs, the input requires 300 mV headroom from the positive and negative rails. This headroom requirement necessitates the negative supply, which was chosen to be −2.5 V.

The AD8634 is available in an 8-lead SOIC rated for 175°C and an 8-lead FLATPACK rated for 210°C.

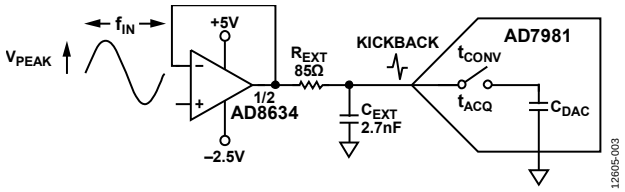

Figure 3. SAR ADC Front End Amplifier and RC Filter

The RC filter between the ADC driver and AD7981 attenuates the kickback injected at the input of the AD7981 and band limits the noise coming to its input. However, too much band limiting can increase settling time and distortion. The calculation of the optimum RC value is primarily based on the input frequency and throughput rate. For the example shown, R = 85 Ω and C = 2.7 nF are the optimum values yielding a cutoff frequency of 693 kHz. Details of the calculations can be found in the Analog Dialogue article, *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter*.

In this circuit, the ADC driver is in unity gain buffer configuration. Adding gain to the ADC driver reduces the bandwidth of the driver and lengthens the settling time. In this case, the throughput of the ADC may need to be reduced or an additional buffer as a driver can be used after the gain stage.

Voltage Reference

The ADR225 2.5 V voltage reference uses only 60 µA maximum of quiescent current at 210°C and has very low drift of 40 ppm/°C typical, making it an ideal device for this low power data acquisition circuit. The ADR225 has an initial accuracy of ±0.4% and can operate over a wide supply range of 3.3 V to 16 V.

The voltage reference input of the AD7981, like other SAR ADCs, has a dynamic input impedance and must therefore be driven by a low impedance source with efficient decoupling between the REF pin and GND, as shown in Figure 4. The AD8634 is well suited as a reference buffer in addition to its ADC driver application.

Another advantage of using a reference buffer is that the noise on the voltage reference output can be further reduced by adding a low pass RC filter. In this circuit, a 49.9 Ω resistor and 47 µF capacitor give a cutoff frequency of approximately 67 Hz.

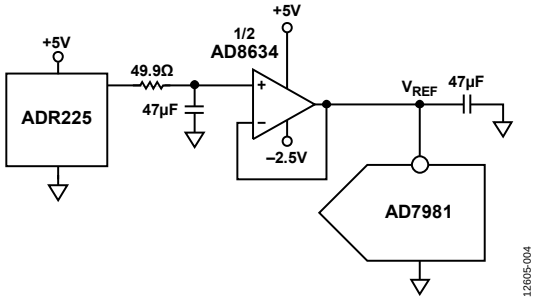

Figure 4. SAR ADC Reference Buffer and RC Filter

During conversions, current spikes as high as 2.5 mA can occur on the AD7981 reference input. A high value reservoir capacitor is placed as close as possible to the reference input to supply that current and to keep the reference input noise low. Typically, a low ESR, 10 µF or more, ceramic capacitor is used; however, for high temperature applications, ceramic capacitors are not available. For this reason, a low ESR, 47 µF tantalum capacitor was chosen that has minimal impact on the performance of the circuit.

Digital Interface

The AD7981 offers a flexible serial digital interface compatible with SPI, QSPI, and other digital hosts. The interface can be configured for a simple 3-wire mode for the lowest input/output count, or 4-wire mode that allows options for the daisy-chained readback and busy indication. The 4-wire mode also allows independent readback timing from the CNV (convert input), which enables simultaneous sampling with multiple converters.

The PMOD interface used on this reference design implements the simple 3-wire mode with SDI tied high to VIO. The VIO voltage is supplied externally from the SDP-PMOD interposer board.

Power Supplies

This reference design requires external, low noise power supplies for the +5 V and −2.5 V rails. Because the AD7981 is low power, it can be supplied directly from the reference buffer, as shown in Figure 5, thereby eliminating the need for an additional power supply rail, saving power and board space.

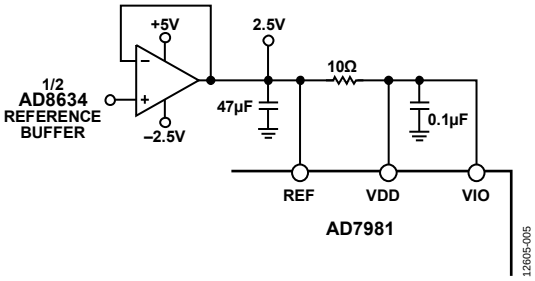

Figure 5. Supplying ADC Reference from Reference Buffer

IC Packaging and Reliability

Devices in the Analog Devices high temperature portfolio go through a special process flow that includes design, characterization, reliability qualification, and production test. Part of this process is special packaging designed specifically for extreme temperatures. A special material is used for the 175°C plastic packages in this circuit.

One of the major failure mechanisms in high temperature packaging is the bond wire-to-bond pad interface, particularly when gold (Au) and aluminum (Al) metals are mixed, as is typical in plastic packages. Elevated temperature accelerates the growth of AuAl intermetallic compounds. It is these intermetallics that are associated with bond failures, such as brittle bonds and voiding, which can occur in a few hundred hours, as shown in Figure 6.

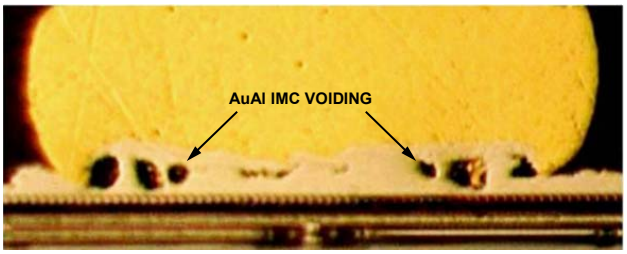

Figure 6. Au Ball Bond on Al Pad, After 500 Hours at 195°C

To avoid these failures, Analog Devices uses an over pad metallization (OPM) process to create a gold bond pad surface for the gold bond wire to attach. This monometallic system does not form intermetallics and has been proven reliable in qualification testing with over 6000 hours soak at 195°C, as shown in Figure 7.

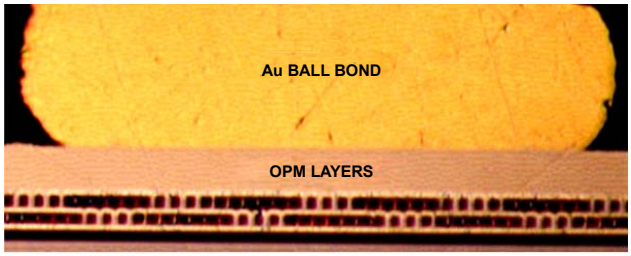

Figure 7. Au Ball Bond on OPM Pad, After 6000 Hours at 195°C

Although Analog Devices has shown reliable bonding at 195°C, the plastic package is rated for operation only up to 175°C due to the glass transition temperature of the molding compound.

In addition to the 175°C rated products used on this circuit, 210°C rated models are also available in a ceramic FLATPACK package. Known good die (KGD) are also available for systems that require custom packaging.

Analog Devices has a comprehensive reliability qualification program for high temperature products that includes high temperature operating life (HTOL), with the devices biased at the maximum operating temperature. High temperature products are data sheet specified for a minimum of 1000 hours at the maximum rated temperature. Full production testing is the last step required to guarantee performance for each device that is manufactured. Each device in the Analog Devices high temperature portfolio is production tested at elevated temperature to ensure that performance is met.

Passive Components

Passive components chosen must be rated for high temperatures. For this design, 175°C+ thin film, low TCR resistors were used. COG/NPO capacitors were used for low value filter and decoupling applications and have a very flat coefficient over temperature. High temperature rated tantalum capacitors are available in larger values than ceramic capacitors and are commonly used for power supply filtering. The SMA connector used on this board is rated for 165°C; therefore, it must be removed for long duration testing at elevated temperatures. Similarly, the insulation material on the 0.1" header connectors (J2 and P3) is only rated for short durations at high temperature and must also be removed for prolonged high temperature testing.

PCB Layout and Assembly

The PCB for this circuit is designed so that the analog signals and digital interface are on opposites sides of the ADC, with no switching signals running under the IC or near analog signal paths. This design minimizes the amount of noise that is coupled into the ADC die and supporting analog signal chain. The pinout of the AD7981, with all its analog signals on the left side and all its digital signals on the right side, eases this task. The voltage reference input, REF, has a dynamic input impedance and must be decoupled with minimal parasitic inductances, which is achieved by placing the reference decoupling capacitor as close as possible to the REF and GND pin and making the connection to the pin with a wide, low impedance trace. The layout of this board was purposely designed with components only on the top side of the board, to facilitate testing over temperature where heat is applied from the bottom of the board. For further layout recommendations, see the AD7981 data sheet.

For high temperature circuits, special circuit materials and assembly techniques must be used to ensure reliability. FR4 is a common material used for PCB laminates; however, commercial grade FR4 has a typical glass transition temperature of approximately 140°C. Above 140°C, the PCB begins to break down, delaminate, and cause stress on components. A widely used alternative for high temperature assemblies is polyimide, which typically has a glass transition temperature of greater than 240°C. A 4-layer polyimide PCB was used in this design.

The PCB surface is also a concern, especially when used with solders containing tin, because of the tendency of the solder to form intermetallics with copper traces. A nickel-gold surface finish is commonly used, where the nickel provides a barrier, and the gold provides a good surface for the solder joint bonding. High melting point solder must also be used with a good margin between the melting point and maximum operating temperature of the system. SAC305 lead free solder was chosen for this assembly. With a melting point of 217°C, there is a margin of 42°C from the highest operational temperature of 175°C.

Performance Expectations

The AD7981 is specified for 91 dB SNR typical with a 1 kHz input tone and a 5 V reference. However, when using low reference voltages, as is common in low power/low voltage systems, some degradation in SNR is expected. From the AD7981 data sheet typical performance curves, approximately 86 dB of SNR is expected at room temperature with a 2.5 V reference. This SNR value compares well with the performance achieved when the circuit was tested at room temperature with approximately 86 dB SNR, as shown in Figure 8.

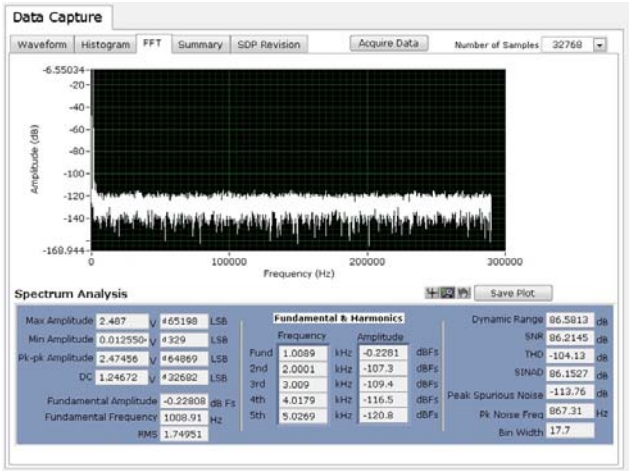

Figure 8. AC Performance with 1 kHz Input Tone, 580 kSPS, 25°C

When this circuit is evaluated over temperature, SNR performance only degrades to approximately 84 dB at 175°C, as shown in Figure 9. THD remains better than −100 dB, as shown in Figure 10. The FFT summary for the circuit at 175°C is shown in Figure 11.

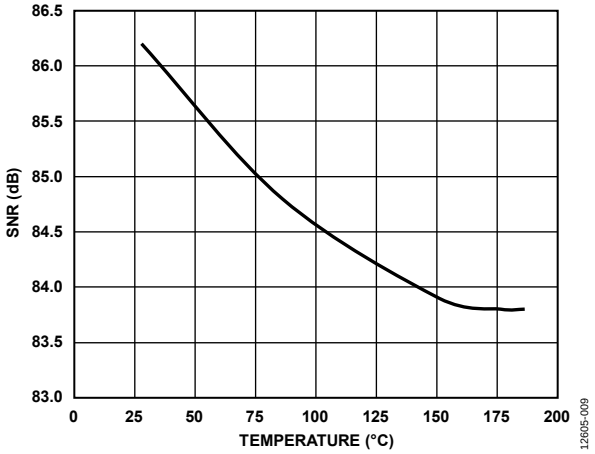

Figure 9. SNR over Temperature, 1 kHz Input Tone, 580 kSPS

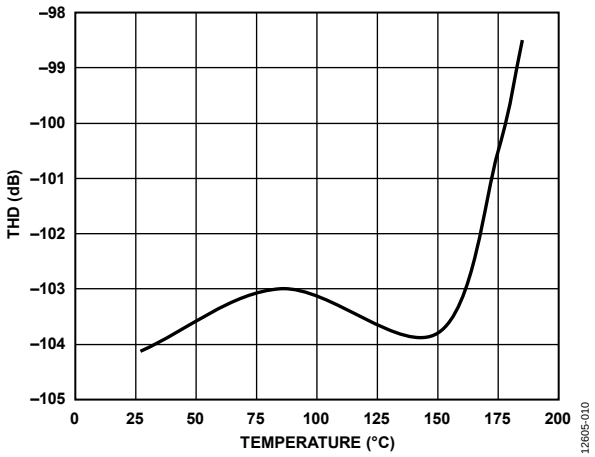

Figure 10. THD over Temperature, 1 kHz Input Tone, 580 kSPS

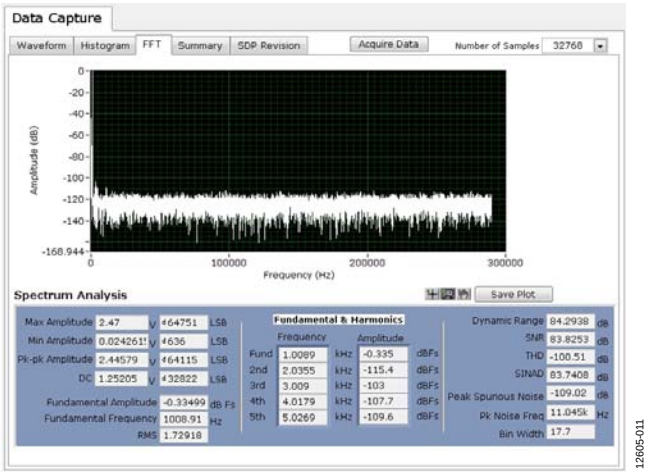

Figure 11. AC Performance with 1 kHz Input Tone, 580 kSPS, 175°C

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0365-PMDZ circuit board, the SDP-PMD-IB1Z interposer board, and the EVAL-SDP-CB1Z system demonstration platform (SDP) board. The interposer board and the SDP board have 120-pin mating connectors. The interposer board and the EVAL-CN0365-PMDZ board have 12-pin PMOD matching connectors, allowing quick setup and evaluation of the circuit performance. The EVAL-CN0365-PMDZ board contains the circuit to be evaluated, as described in the CN-0365, and the SDP evaluation board is used with the CN-0365 Evaluation Software.

Equipment Needed

The following equipment is needed:

- EVAL-CN0365-PMDZ board
- System Demonstration Platform (EVAL-SDP-CB1Z)
- PMOD to SDP Interposer Board (SDP-PMD-IB1Z)
- CN-0365 Evaluation Software
- Function generator/signal source, such as the Audio Precision SYS-2522 used in these tests
- Power supplies: +5 V and −2.5 V
- Power supply: +6 V wall wart (EVAL-CFTL-6V-PWRZ)
- PC operating Windows® XP (SP2), Windows Vista or Windows 7 Business/Enterprise/Ultimate editions (32-bit/64-bit systems) with USB port and USB cable

Getting Started

To get started, take the following steps:

1. Download the CN-0365 Evaluation Software to the PC from ftp://ftp.analog.com/pub/cftl/CN0365.
2. Install the software prior to connecting the SDP board to the USB port of the PC, to ensure that the SDP board is recognized when it connects to the PC.
3. Unzip the downloaded file.
4. Run the **setup.exe** file.
5. Follow the on-screen prompts to finish the installation. It is recommended to install all software components to the default locations.

Functional Block Diagram

Figure 12 shows the functional diagram of the test setup.

Setup

To set up the circuit, take the following steps:

1. Connect the EVAL-CFTL-6V-PWRZ (+6 V dc power supply) to the SDP-PMD-IB1Z interposer board via the dc barrel jack.
2. Connect the SDP-PMD-IB1Z interposer board to the EVAL-SDP-CB1Z SDP board via the 120-pin CON A connector.
3. Connect the EVAL-SDP-CB1Z SDP board to the PC via the USB cable.
4. Connect the EVAL-CN0365-PMDZ evaluation board to the SDP-PMD-IB1Z interposer board via the 12-pin header PMOD connector.
5. Connect the +5 V (V_S+) and −2.5 V (V_S−) power supplies to the EVAL-CN0365-PMDZ P3 header. The VDD voltage (2.5 V) does not need an external connection in the default configuration because it is generated on-board.
6. Connect the signal source to the EVAL-CN0365-PMDZ via the SMA connector.
7. Set the Audio Precision SYS-2522 (or equivalent signal generator) for a 1 kHz frequency and a 2.5 V p-p sine wave with a 1.25 V dc offset.

Test

Launch the evaluation software. The software communicates to the SDP board if the Analog Devices System Development Platform drivers are listed in Windows Device Manager. After USB communications are established, the evaluation software can be used to test, view, and save circuit performance metrics.

Further details on the operation of the software can be found in the UG-340 and at the *Evaluating 14-/16-/18-Bit ADCs from the 8/10 LEAD PulSAR® Family* wiki page.

For testing over temperature in an environmental chamber, extension harnesses (not supplied) can be used for the analog input, power supply, and PMOD connections. These harnesses must be as short as possible, and best practices must be used to avoid noise. The SMA connector used on this board is rated for 165°C; therefore, it must be removed for long duration testing at elevated temperatures. Similarly, the insulation material on the 0.1" header connectors (J2 and P3) is only rated for short durations at high temperature and must also be removed for prolonged high temperature testing.

A photo of the EVAL-CN0365-PMDZ board is shown in Figure 13.

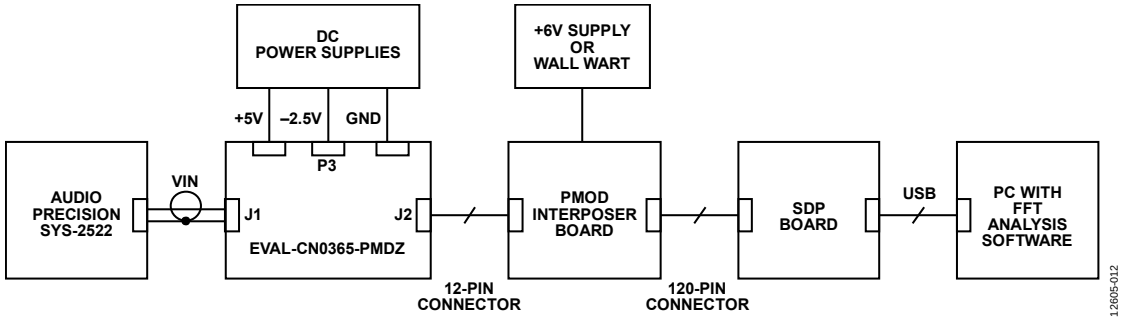

Figure 12. Circuit Test Setup for Measuring AC Performance

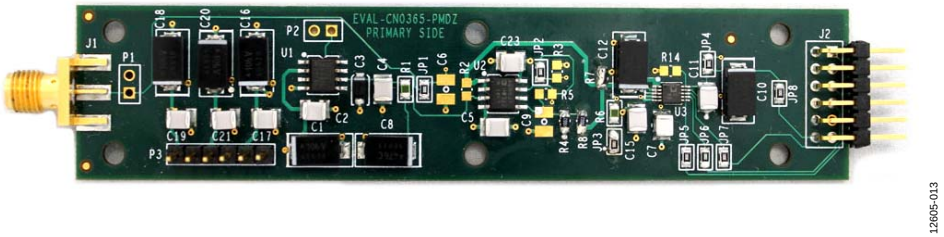

Figure 13. Photo of EVAL-CN0365-PMDZ Circuit Board

LEARN MORE

CN-0365 Design Support Package: www.analog.com/CN0365-DesignSupport

System Demonstration Platform (SDP)

UG-340 User Guide

Evaluating 14-/16-/18-Bit ADCs from the 8/10 LEAD PulSAR® Family Wiki Page

High Temperature Products from Analog Devices

Watson, Jeff and Gustavo Castro, "High Temperature Electronics Pose Design and Reliability Challenges," Analog Dialogue, Volume 46, April 2012.

Watson, Jeff and Maithil Pachchigar, "Harsh Environments Conquered—Lower Power, Precision, High Temperature Components for Extreme Temperature Applications," MS-2707, Analog Devices.

Walsh, Alan, "Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter," Analog Dialogue, Vol. 46, December 2012.

Walsh, Alan "Voltage Reference Design for Precision Successive-Approximation ADCs," Analog Dialogue, Vol. 47, June 2013.

MT-021 Tutorial, *Successive Approximation ADCs*, Analog Devices

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND,"* Analog Devices.

Data Sheets and Evaluation Boards

CN-0365 Circuit Evaluation Board (EVAL-CN0365-PMDZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

SDP-PMOD Interposer Board (SDP-PMD-IB1Z)

AD7981 Data Sheet

AD8634 Data Sheet

ADR225 Data Sheet

REVISION HISTORY

6/15—Revision 0: Initial Version

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0370.

Devices Connected/Referenced	
AD5542A	Serial-Input, Voltage Output, Unbuffered 16-Bit DAC
ADA4500-2	Rail-to-Rail Input/Output, Zero Input Crossover Distortion Amplifier
ADR4525	Ultralow Noise, High Accuracy, 2.5 V Voltage Reference

16-Bit, Single-Supply LED Current Driver with Less than ±1 LSB Integral and Differential Nonlinearity

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0370 Circuit Evaluation Board (EVAL-CN0370-PMDZ)
System Demonstration Platform (EVAL-SDP-CB1Z)
PMOD to SDP Interposer Board (SDP-PMD-IB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit in Figure 1 is a complete single-supply, low noise LED current source driver controlled by a 16-bit digital-to-analog converter (DAC). The system maintains ±1 LSB integral and differential nonlinearity and has a 0.1 Hz to 10 Hz noise of less than 45 nA p-p for a full-scale output current of 20 mA.

The innovative output driver amplifier eliminates the crossover nonlinearity normally associated with most rail-to-rail input op amps that can be as high as 4 LSBs or 5 LSBs for a 16-bit system.

This industry-leading solution is ideal for pulse oximetry applications where 1/f noise superimposed on the LED brightness levels affects the overall accuracy of the measurement.

Total power dissipation for the three active devices is less than 20 mW typical when operating on a single 5 V supply.

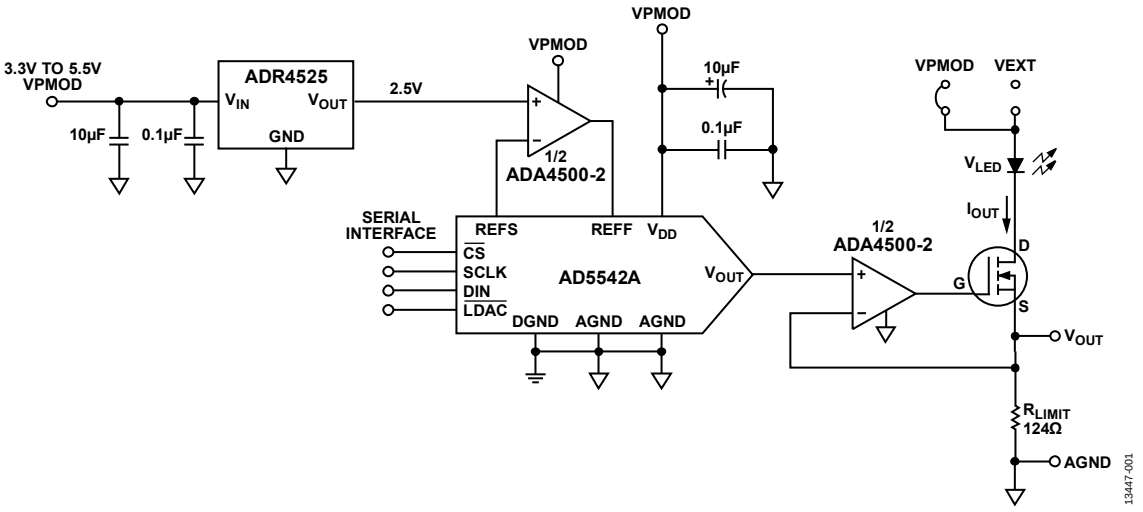

Figure 1. ±1 LSB Linear 16-Bit LED Current Source Driver (Simplified Schematic: All Connections and Decoupling Not Shown)

Rev. 0

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CIRCUIT DESCRIPTION

In a typical pulse oximetry application, an LED is pulsed from a high level of current (for example, 3/4 scale) to a lower level of current (for example, 1/4 scale). The on-time of these pulses is typically in the order of several hundred microseconds. Peak-to-peak 1/f noise superimposed on the LED brightness levels during the on-time affects the accuracy of the overall measurement and must be minimized.

Figure 1 shows the single-supply signal chain that consists of a voltage reference, a DAC, a DAC output buffer, and a current source.

The DAC is the AD5542A 16-bit, serial input, voltage output segmented R-2R CMOS DAC. The output voltage of the DAC is dependent on the reference voltage, as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:
D is the decimal data word loaded in the DAC register.
N is the number of bits.

For a reference of 2.5 V and N = 16, the equation simplifies to the following:

$$V_{OUT} = \frac{2.5 \times D}{2^{16}} = \frac{2.5 \times D}{65{,}536}$$

This gives a V_{OUT} of 1.25 V at mid scale, and 2.5 V at full scale.

The LSB size is 2.5 V/65,536 = 38.1 µV.

One LSB at 16 bits is also 0.0015% of full scale or 15 ppm full scale.

The DAC reference pin is driven by an 2.5 V ADR4525 voltage reference buffered with the ADA4500-2. The ADR4525 voltage reference provides a high precision, low noise (1.25 µV p-p, 0.1 Hz to 10 Hz), and stable reference to the DAC. The ADR4525 uses an innovative core topology to achieve high accuracy while offering industry-leading temperature stability and noise performance. The low output voltage temperature coefficient (2 ppm/°C maximum) and low long-term output voltage drift of the device also improve system accuracy over time and temperature variations. The initial room temperature error of the ADR4525B is ±0.02% maximum, which is approximately 13 LSBs at 16 bits.

The dual ADA4500-2 is selected as the DAC output buffer as well as the voltage reference buffer. The ADA4500-2 is a high precision amplifier with maximum offset voltage of 120 µV, offset drift of less than 5.5 µV/°C, 0.1 Hz to 10 Hz noise of 2 µV p-p, and maximum input bias current of 2 pA. Its innovative rail-to-rail input structure eliminates crossover distortion and therefore makes it an excellent choice as a DAC buffer.

A typical rail-to-rail input amplifier uses two differential pairs (PNP and NPN, or PMOS and NMOS) to achieve rail-to-rail input swing (see the MT-035 Tutorial). One differential pair is active at the low range of the input common-mode voltage, and the other pair is active at the high end. This classic complementary dual differential pair topology introduces crossover distortion during the transition between one differential pair to the other. The change in offset voltage causes nonlinearity when the amplifier is used as a DAC buffer.

The ADA4500-2 uses an integrated charge pump in its input structure to achieve rail-to-rail input swing without the need for a second differential pair. Therefore, it does not exhibit crossover distortion. Using a zero crossover distortion amplifier in this single-supply system provides wide dynamic output range while maintaining linearity over the entire input common-mode range. Details of the operation of the ADA4500-2 can be found in the ADA4500-2 data sheet.

The output impedance of the DAC is constant (typically 6.25 kΩ) and code independent. The output buffer must therefore have a high input impedance and low input bias current to minimize errors. The ADA4500-2 is a suitable candidate with high input impedance and 2 pA maximum of input bias current at room temperature, and 190 pA maximum of input bias current over temperature. This results in 1.2 µV worst-case error due to input bias current flowing through the 6.25 kΩ DAC impedance, which is significantly less than 1 LSB.

The output of the DAC is buffered and used to drive the power MOSFET (IRLMS2002TRPBF). The MOSFET converts the DAC output voltage into current that drives the LED. The MOSFET in the circuit is able to handle currents up to 6.5 A; however, the current is limited to 20 mA, which is the maximum rated current of the LED supplied on the EVAL-CN0370-SDPZ board. The board has provisions to easily change the full-scale current to the LED by changing the R_{LIMIT} resistor. The maximum current can be calculated by

$$I_{MAX} = 2.5\ V/R_{LIMIT}$$

Jumper options allow the LED to be connected to either the PMOD voltage (VPMOD) or an external voltage (VEXT).

The VEXT option is required to provide sufficient headroom for the MOSFET when operating with VPMOD = 3.3 V. For example, if V_{OUT} = 2.5 V, V_{DS} = 0.7 V, and V_{LED} = 0.7 V, then VEXT must be greater than 2.5 V + 0.7 V + 0.7 V = 3.9 V.

An alternative that allows 3.3 V supply operation is to limit the full-scale output voltage to approximately 1.9 V and only use 76% of the DAC output range. The R_{LIMIT} resistor must be changed to approximately 95 Ω to maintain 20 mA full-scale output current at 1.9 V output.

The AD5542A is available in a 10-lead MSOP or 10-lead LFCSP. The ADR4525 is available in an 8-lead SOIC, and the ADA4500-2 is available in an 8-lead MSOP or 8-lead LFCSP.

Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) Measurements

INL is the deviation in LSB of the actual DAC transfer function from an idealized transfer function. DNL is the difference between an actual step size and the ideal value of 1 LSB. This system solution provides a 16-bit resolution with ±1 LSB DNL and INL. Figure 2 and Figure 3 show the DNL and INL performance of the circuit.

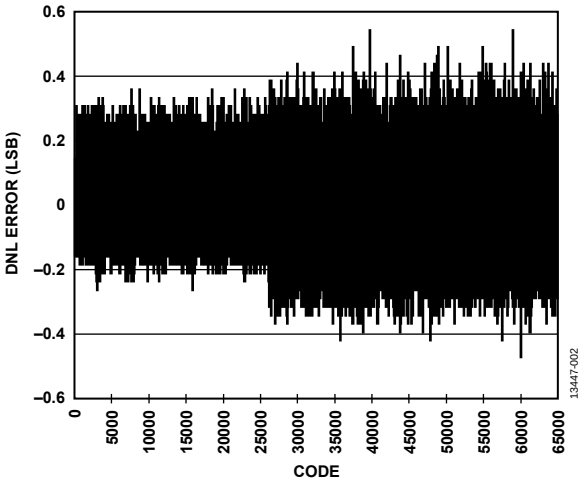

Figure 2. Differential Nonlinearity (DNL)

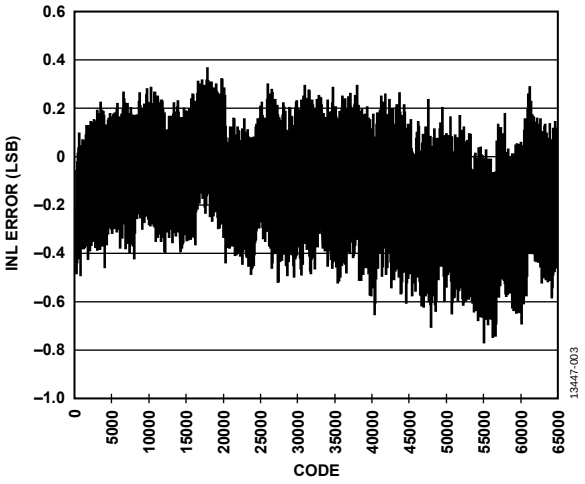

Figure 3. Integral Nonlinearity (INL)

Note that the DNL and INL measurements exclude the 100 codes (approximately 4 mV) from the lower end of the range. This is because the MOSFET leakage current causes the output voltage to become nonlinear in this region.

Figure 4 shows the nonlinearity introduced using an op amp with a traditional rail-to-rail input stage. This plot shows the crossover distortion when the active differential pair changes from the PNP pair to the NPN pair. The error swings from +4 LSB to −15 LSB in this region.

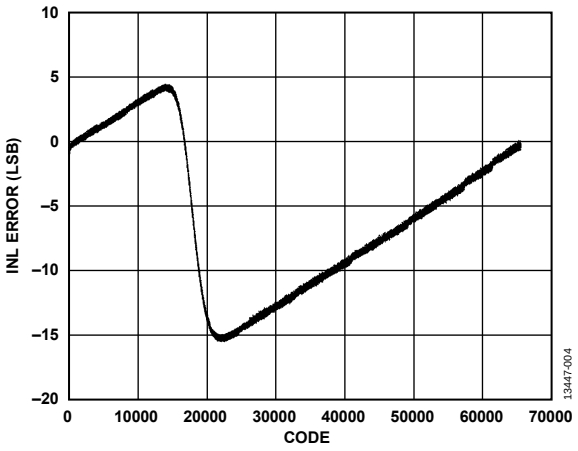

Figure 4. DAC Nonlinearity when Using Op Amp Buffer with Traditional Rail-to-Rail Input Stage

Noise Measurements

The targeted 0.1 Hz to 10 Hz noise for the complete system was less than 14 µV p-p measured at V_{OUT}. The noise of the three components can be combined in a root-sum-squares (RSS) manner to estimate the total system noise. The 0.1 Hz to 10 Hz values are

- AD5542A: 0.134 µV p-p
- ADR4525: 1.25 µV p-p
- ADA4500-2 (reference buffer): 2 µV p-p
- ADA4500-2 (DAC buffer): 2 µV p-p

The RSS value of the above contributors is 3.1 µV p-p.

The true noise of the circuit is measured by using a noise measuring box with a gain of 10,000 combined with a 0.1 Hz to 10 Hz filter. Figure 5 shows the noise test setup.

The EVAL-SDP-CB1Z System Development Platform (SDP) and SDP-PMD-IB1Z interposer boards were removed from the setup, and the supply was taken from a 4.5 V battery.

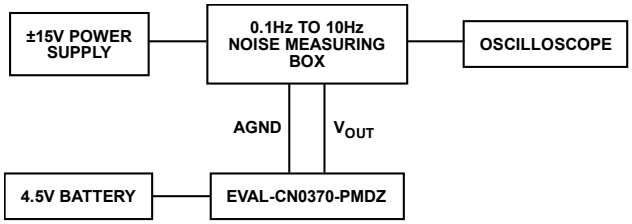

Figure 5. Test Setup for Measuring 0.1 Hz to 10 Hz Noise with Gain of 10,000

The noise output of the box with the input shorted and the noise with the circuit connected were measured and were 7.81 µV p-p and 9.6 µV p-p, respectively, as shown in Figure 6 and Figure 7. The noise of the two systems is uncorrelated and therefore combines in an RSS manner, and the system noise is calculated as follows:

$$System\ Noise = \sqrt{(9.6)^2 - (7.81)^2} = 5.58\ \mu V\ p\text{–}p$$

The corresponding noise current driving the LED is 5.58 µV ÷ 124 Ω = 45 nA for a full-scale current of 20 mA.

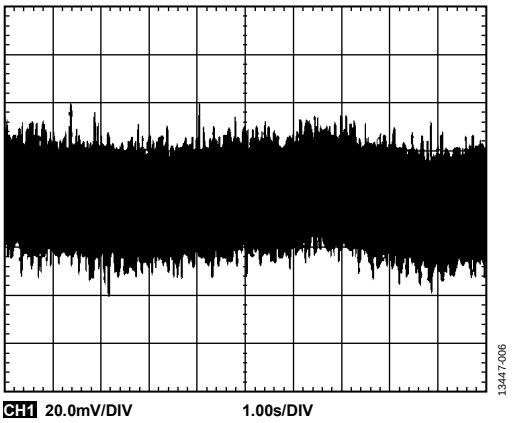

Figure 6. Output Noise with Input to Noise Measuring Box Shorted Measures 78.1 mV p-p (7.81 µV p-p Referenced to Input)

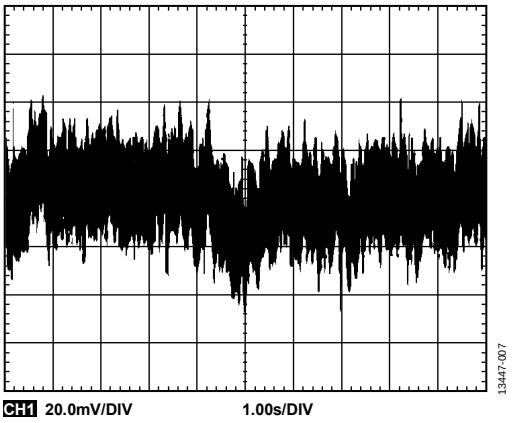

Figure 7. Output Noise with EVAL-CN0370-PMDZ Connected Measures 96 mV p-p (9.6 µV p-p Referenced to Input)

Board Layout Considerations

It is important to carefully consider the power supply and ground return layout on the board. The printed circuit board must have separate analog and digital sections. If the circuit is used in a system where multiple devices require an analog ground to digital ground connection, make the connection at only one point. Power supplies to all components must be bypassed with at least 0.1 µF capacitors. These bypass capacitors must be as physically close as possible to the device, with the capacitor ideally right up against the device. Choose the 0.1 µF capacitor to have low effective series resistance (ESR) and low effective series inductance (ESL), such as ceramic capacitors. This 0.1 µF capacitor provides a low impedance path to ground for transient currents. The power supply line must also have as large a trace as possible to provide a low impedance supply path. Use proper layout, grounding, and decoupling techniques to achieve optimum performance (see the the MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND* and the MT-101 Tutorial, *Decoupling Techniques*).

A complete design support package including layout files, schematics, and bill of materials, is available at www.analog.com/CN0370-DesignSupport.

COMMON VARIATIONS

For a lower power consumption solution (at lower speed), use the ADA4505-1/ADA4505-2/ADA4505-4 as the output buffer. The ADA4505-1/ADA4505-2/ADA4505-4 are micropower, zero crossover distortion amplifiers with low input bias current. The ADR441 and ADR421are suitable candidates to provide the 2.5 V reference. They feature high accuracy, low noise and accept input voltages up to 18 V.

The AD5063 is a 16-bit, unbuffered voltage output DAC that allows bipolar mode operation in a dual-supply application.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0370-PMDZ circuit board and the EVAL-SDP-CB1Z SDP board with the SDP-PMD-IB1Z interposer board. The SDP board and the interposer boards have 120-pin mating connectors, allowing quick setup and evaluation of the circuit performance. The EVAL-CN0370-PMDZ board is connected via the PMOD connector J3. The EVAL-CN0370-PMDZ contains the circuit to be evaluated, as described in this circuit note. The SDP board and the interposer board are used with the CN-0370 evaluation software to capture the data from the EVAL-CN0370-PMDZ circuit board. The software user guide is available at www.analog.com/wiki-CN0370.

Equipment Needed

The following equipment is needed:

- PC with a USB port and Windows® XP, Windows Vista (32-bit), or Windows 7 (32-bit)
- EVAL-CN0370-PMDZ circuit evaluation board
- EVAL-SDP-CB1Z SDP board
- SDP-PMD-IB1Z interposer board
- CN-0370 evaluation software (download from ftp://ftp.analog.com/pub/cftl/CN0370/)
- Power supply: 6 V wall wart or EVAL-CFTL-6V-PWRZ
- Agilent 34401A multimeter or equivalent
- GPIB to USB cable (required only when making linearity measurements on the circuit)

Getting Started

Download the CN-0370 evaluation software and install it on the PC.

Functional Block Diagram

Figure 8 shows the functional block diagram of the test setup.

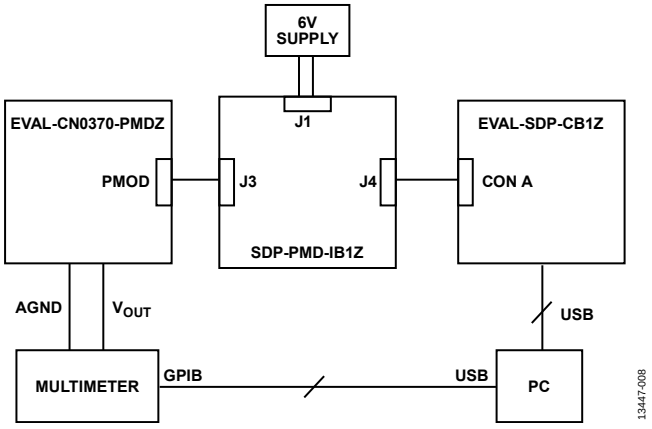

Figure 8. Test Setup Functional Block Diagram

Setup

Connect the 120-pin connector on the SDP-PMD-IB1Z interposer board to the connector marked CON A on the EVAL-SDP-CB1Z SDP board. Use nylon hardware to secure the two boards firmly, using the holes provided at the ends of the 120-pin connectors. Connect the EVAL-CN0370-PMDZ to the J3 PMOD connector.

With power to the supply off, connect a 6 V wall wart power supply to the J1 connector. Connect the USB cable supplied with the SDP board to the USB port on the PC. Do not connect the USB cable to the mini USB connector on the SDP board at this time.

Test

Apply power to the interposer board then connect the USB cable from the PC to the USB mini connector on the SDP board and launch the evaluation software. The software communicates with the EVAL-CN0370-PMDZ if the EVAL-SDP-CB1Z System Development Platform is listed in Windows **Device Manager**.

After USB communications are established, the SDP board can be used to write date to the EVAL-CN0370-PMDZ circuit evaluation board.

Figure 9 shows a photograph of the EVAL-CN0370-PMDZ circuit evaluation board.

Information and details regarding test setup and how to use the evaluation software for data capture can be found in the CN-0370 Software User Guide.

Information regarding the SDP board is available in the SDP User Guide (UG-277).

Figure 9. EVAL-CN0370-PMDZ Circuit Evaluation Board

LEARN MORE

CN-0370 Design Support Package: www.analog.com/CN0370-DesignSupport

Kester, Walt. *The Data Conversion Handbook*, Chapter 3 and Chapter 7. Analog Devices, 2005.

AN-1212 Application Note. *Single-Supply Low Noise LED Current Source Driver Using a Current Output DAC in the Reverse Mode*. Analog Devices.

Circuit Note CN-0348. *16-Bit Single-Supply Buffered Voltage Output Digital-to-Analog Conversion with Less Than ±1 LSB and Differential Nonlinearity*. Analog Devices.

MT-015 Tutorial. *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-016 Tutorial. *Basic DAC Architectures III: Segmented DACs*. Analog Devices.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-035 Tutorial. *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*. Analog Devices.

MT-101 Tutorial. *Decoupling Techniques*. Analog Devices.

Data Sheets and Evaluation Boards

AD5542A Data Sheet

ADA4500-2 Data Sheet

ADR4525 Data Sheet

REVISION HISTORY

9/15—Revision 0: Initial Version

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0373.

Devices Connected/Referenced	
ADM3252E	2.5 kV, Signal and Power Isolated, Dual Channel, RS-232 Line Driver/Receiver
ADM2587E	2.5 kV, Signal and Power Isolated, ±15 kV ESD Protected, Full/Half-Duplex, RS-485 Transceiver
ADuM3160	Full/Low Speed, 2.5 kV, USB Digital Isolator
ADuM3070	2.5 kV, Isolated Switch Regulator With Integrated Feedback
ADP190	Logic Controlled, High-Side Power Switch
ADP7102	20 V, 300 mA, Low Noise, CMOS LDO

Isolated USB to Isolated RS-485/Isolated RS-232 Interface

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0373 Circuit Evaluation Board (EVAL-CN0373-EB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 provides a completely isolated connection between the popular USB bus and an RS-485 or RS-232 bus. Both signal and power isolation ensures a safe USB device interface to an industrial bus or debug port, allowing TIA/EIA-485/232 bus traffic monitoring and the convenience of sending and receiving commands to and from a PC that is not equipped with an RS-485 or RS-232 port.

Isolation in this circuit increases system safety and robustness by providing protection against electrical line surges and breaks the ground connection between bus and digital pins, thereby removing possible ground loops within the system.

The TIA/EIA RS-485 bus standard is one of the most widely used physical layer bus designs in industrial and instrumentation applications. RS-485 offers differential data transmission between multiple systems, often over very long distances. RS-485 communication offers additional robustness through differential communication when compared to the RS-232 standard.

TIA/EIA RS-232 devices are widely used in industrial machines, networking equipment, and scientific instruments. In modern personal computers, which are often used for debugging network problems, USB has displaced RS-232 from most of its peripheral interface roles, and many computers do not come equipped with RS-232 ports. The circuit in Figure 1 offers a robust and compact solution for both RS-232 and RS-485 interfaces.

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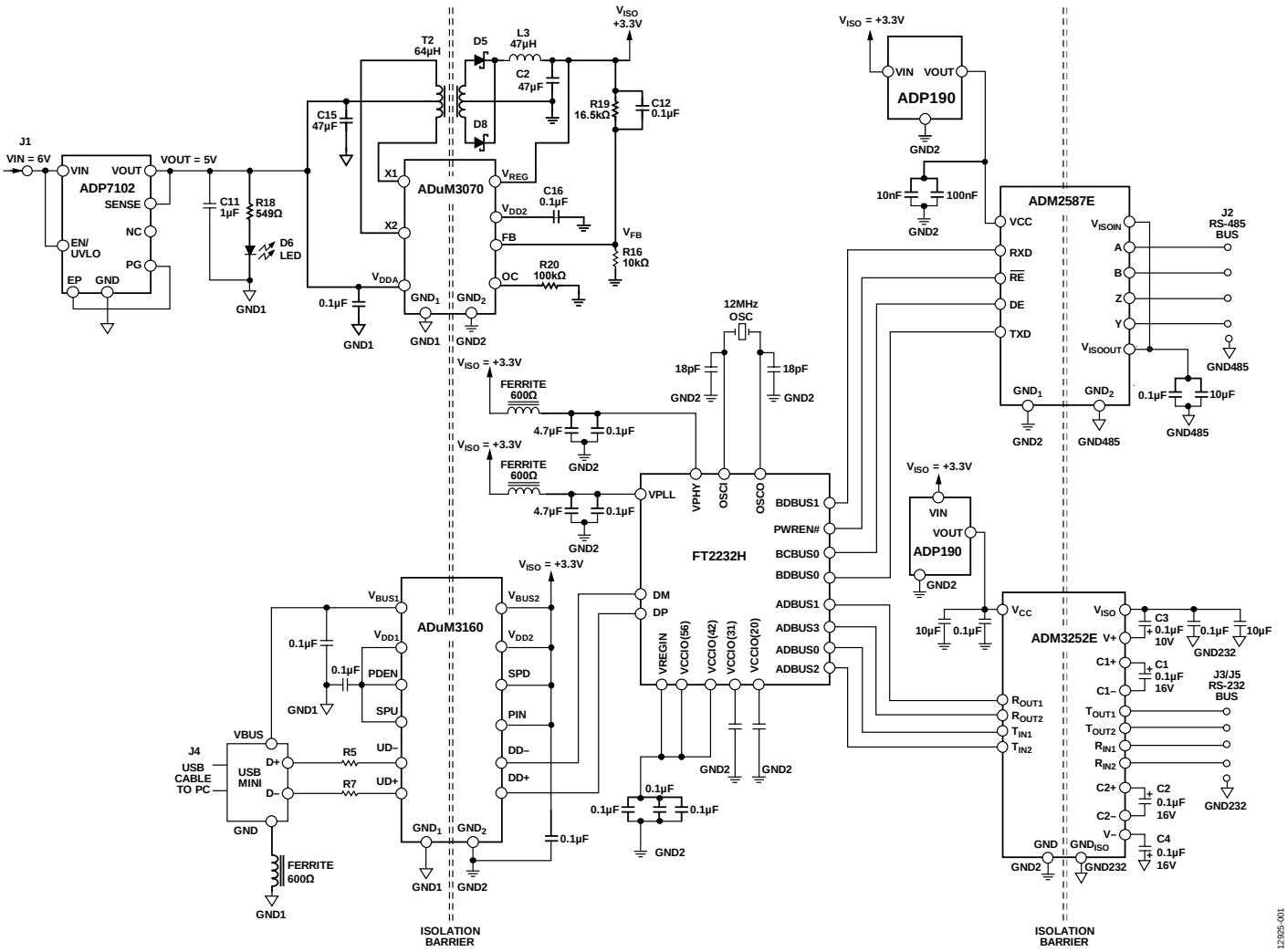

Figure 1. Isolated USB to FTDI Isolated RS-232/Isolated RS-485 Circuit (Simplified Schematic, All Connections Not Shown)

CIRCUIT DESCRIPTION

The circuit in Figure 1 provides highly integrated and robust isolation of fully TIA/EIA-485/232 compliant transceivers. The ADM3252E 2.5 kV rms isolated RS-232 and the ADM2587E 2.5 kV rms isolated RS-485 solutions are the smallest available in the industry. The ADuM3160 provides market-leading USB port 2.5 kV rms isolation, and is easily integrated with low and full speed USB-compatible peripheral devices. The FTDI FT2232H (USB to UART converter) facilitates transmission via UART to RS-485 or RS-232 bus ports. TIA/EIA RS-232 devices are widely used in industrial machines, networking equipment, and scientific instruments. Applications for RS-485 include process control networks; industrial automation; remote terminals; building automation, such as heating, ventilation, air conditioning (HVAC) and security systems; motor control; and motion control.

In these real-world systems, lightning strikes and power source fluctuations can cause damage to communications ports by generating large transient voltages. Isolation in the Figure 1 circuit increases system safety by providing protection against these electrical line surges.

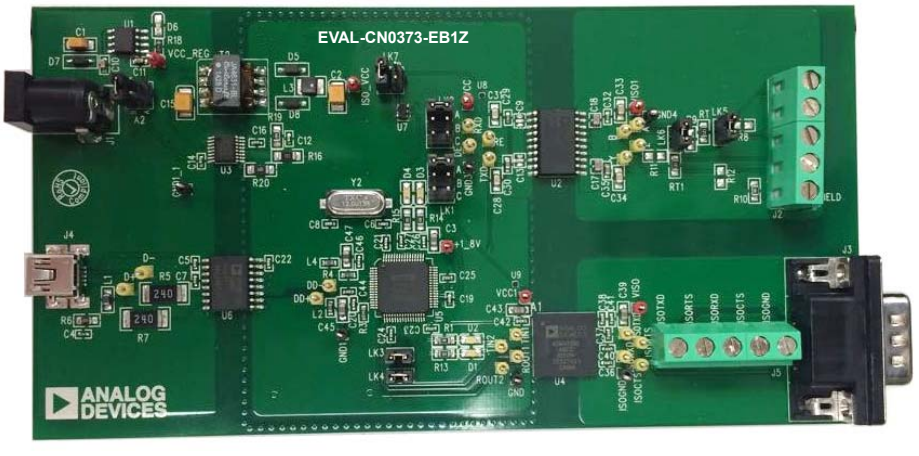

Figure 2. EVAL-CN0373-EB1Z Board

Figure 2 shows a photo of the isolated USB to FTDI isolated RS-232/isolated RS-485 circuit. It is possible to transmit from the USB port to both RS-485 and RS-232 ports simultaneously, if required, or to just one port.

The ADuM3160 provides 2.5 kV rms digital isolation of the data signals on the D+ and D− USB bus input to the FTDI FT2232H (USB to UART converter). The isolated USB output DD− and DD+ signals are connected to the DM and DP pins of the FTDI, respectively. The FTDI FT2232H can transmit data via UART to RS-232/RS-485 depending on which PC virtual COM port (VCP) is chosen. The ADuM3160 V_{BUS1} power is supplied via the USB cable connection. The ADuM3070 provides a regulated isolated power source. Power (+6 V) and ground for the ADuM3070 are connected via the J1 barrel socket connector. The ADuM3160 V_{BUS2} pin is supplied with 3.3 V isolated power by the ADuM3070. The ADuM3070 3.3 V output also supplies the primary power for the ADM3252E 2.5 kV rms isolated RS-232 and the ADM2587E 2.5 kV rms isolated RS-485 transceiver.

The ADM2587E 2.5 kV rms isolated RS-485 transceiver is the industry-leading signal and power isolated solution. This transceiver is capable of operating at 3.3 V or 5 V. Data transmits on the TxD pin, and it is received on the RxD pin. Both the driver and receiver outputs can be enabled or disabled, that is, put into a high impedance state, by changing the logic levels on the DE and $\overline{RE}$ pins, respectively.

The FTDI output pin BDBUS0 is connected to the TxD data input pin of the ADM2587E. The FTDI output pins BCBUS0, PWREN#, and BDBUS1 are connected to the DE, $\overline{RE}$, and RxD input pins of the ADM2587E, respectively. The DE and $\overline{RE}$ pin state can also be configured via the LK1 and LK2 jumpers. For each link, Position A connects the logic pin to 3.3 V, Position B connects the logic pin to GND, and Position C connects the logic pin to the FTDI output pins.

The ADM2587E can transmit and receive bus data via the A, B, Y, and Z RS-485 inputs/outputs. An RS-485 bus cable can be connected via the J2 five-way connector. Disconnecting the LK5 and LK6 jumpers places the ADM2587E in a full duplex configuration, where data can be transmitted via the Y and Z pins, and received via the A and B pins. Connecting the LK5 and LK6 jumpers places the ADM2587E inputs/outputs in a half duplex configuration, which is where bus data can only be transmitted or received, but not simultaneously.

The ADM3252E is a high speed, 2.5 kV, fully isolated, dual channel RS-232/V.28 transceiver device that is operational from a single 3.3 V or 5 V power supply. The RS-232 interface supports full-duplex communication and provides CTS and RTS for hardware handshaking via the J5 five-way connector or the J3 connector. J3 provides an RS-232 cable connector for connecting to industrial equipment.

The ADM3252E transmitter inputs (T_{INx}) accept TTL/CMOS input levels from the ADBUS0 and ADBUS2 output pins of the FTDI. The T_{INx} inputs are inverted and coupled across the isolation barrier, where they are transmitted as EIA/TIA-232E bus signals via the J3 or J5 connector. The ADM3252E receiver inputs (R_{INx}) accept EIA/TIA-232E signal levels from the J3 or J5 connector. The R_{INx} inputs are inverted and coupled across the isolation barrier to appear at the R_{OUTx} pins. The R_{OUTx} pins are connected to the ADBUS1 and ADBUS3 inputs to the FTDI.

Two separate ADP190 circuits are used as soft start circuitry to power the ADM2587E and ADM3252E after the FTDI FT2232H has fully powered up. Jumper LK7 links the FTDI FT2232H PWREN# pin to the EN pin of the ADP190 circuits via the 74AHC1G14W5-7 inverter. The ADP190 EN pin must be high to turn on the power switch; drive EN low to turn off the power switch. Connecting LK7 in Position A (Position B disconnected) means that the ADP190 EN pin is always high/enabled. Connecting LK7 in Position B (Position A disconnected) means that the ADP190 EN pin is triggered via the inverted PWREN# signal.

The FTDI FT2232H data sheet provides a comprehensive listing of the pin functions for RS-232 communications. The LK3 and LK4 jumpers allow handshaking options for RS-232. When LK3 is connected, ADBUS4 (DTR#) is connected to ADBUS5 (DSR#). When LK4 is connected, ADBUS4 (DTR#) is connected to ADBUS6 (DCD#).

CIRCUIT EVALUATION AND TEST

Apply 6 V to the J1 barrel socket connector to power the EVAL-CN0373-EB1Z board. The voltage can be checked on the VCC_REG test point at the output of the ADP7102 regulator. The ADP7102 output voltage should measure 5 V. The 5 V is routed to the ADuM3070 and T2 transformer, which supply the 3.3 V outputs to power the RS-485, RS-232, and FTDI circuits. Check that the ISO_VCC test point measures 3.3 V.

A complete transmit and receive path can be tested by connecting the RS-232 and RS-485 outputs to an Analog Devices ezLINX™ *i*Coupler® Isolated Interface Development Environment board. Alternatively, a USB to RS-232/RS-485 transmit test can be performed by using the Tera Term open source terminal emulator program. It is possible to transmit from the USB port to both RS-485/RS-232 ports simultaneously, if required, or to just one port.

Connect a USB cable from the laptop/PC to the J4 connector. Attach an oscilloscope probe to the ISOTxD test point next to the ADM3252E transceiver, as shown in Figure 3. Open the PC application software and select **COM5**, then click **OK**, as shown in Figure 4.

Load the RS-232 data to be transmitted by clicking **Send** under the **File** menu. Choose any large data size file for continuous test transmission and click **Send**, as shown in Figure 5.

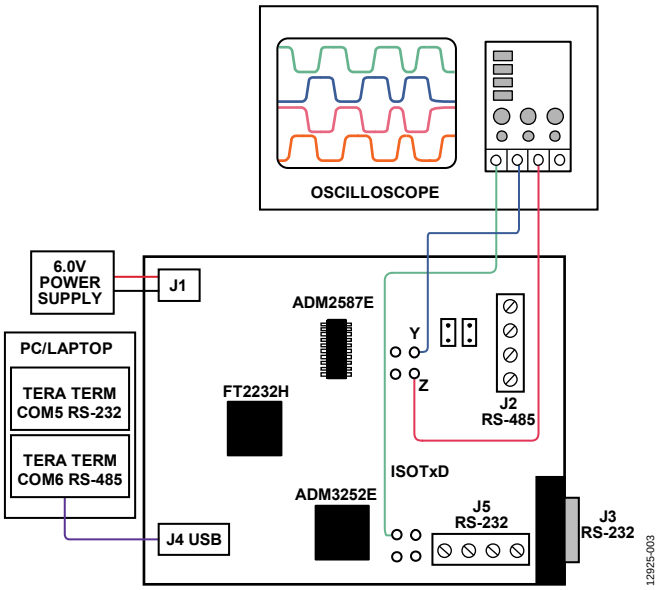

Figure 3. Test Setup for the EVAL-CN0373-EB1Z Board

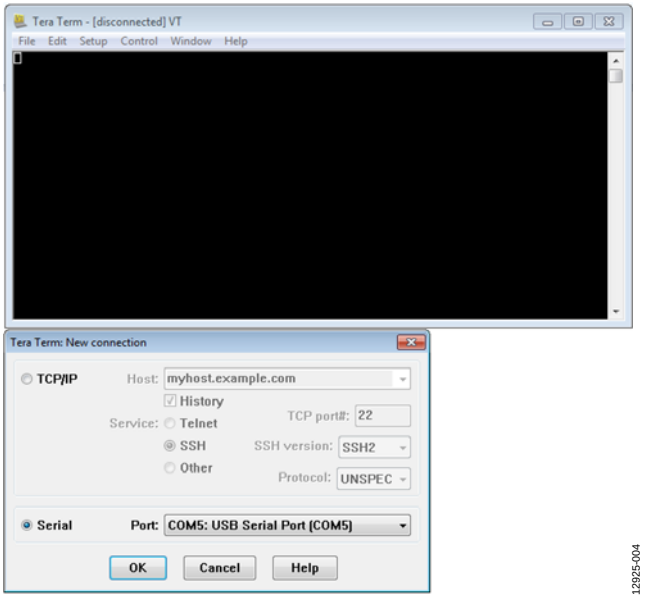

Figure 4. Tera Term COM5 for USB Transmission to the RS-232 Port on the EVAL-CN0373-EB1Z Board

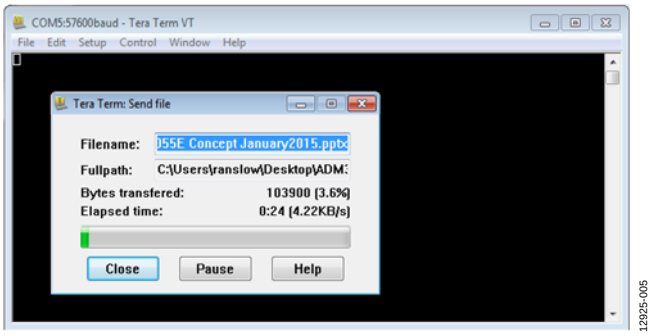

Figure 5. Tera Term COM5 Data for USB Transmission to the RS-232 Port on the EVAL-CN0373-EB1Z Board

Observe the isolated RS-232 signal on an oscilloscope by probing the ISOTxD test point on the EVAL-CN0373-EB1Z board (see Figure 6).

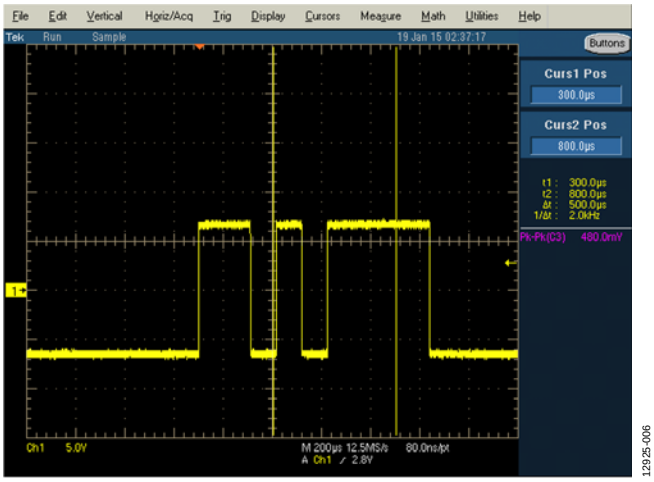

Figure 6. ISOTxD Signal for the RS-232 Port on the EVAL-CN0373-EB1Z Board

A similar test can be performed for the ADM2587E transceiver. Connect a USB cable from the laptop/PC to the J4 connector. Attach an oscilloscope probe to the Y and Z test points next to the ADM2587E transceiver as shown in Figure 3. Open a second Tera Term emulator window, and select **COM6** for RS-485 transmission, as shown in Figure 7.

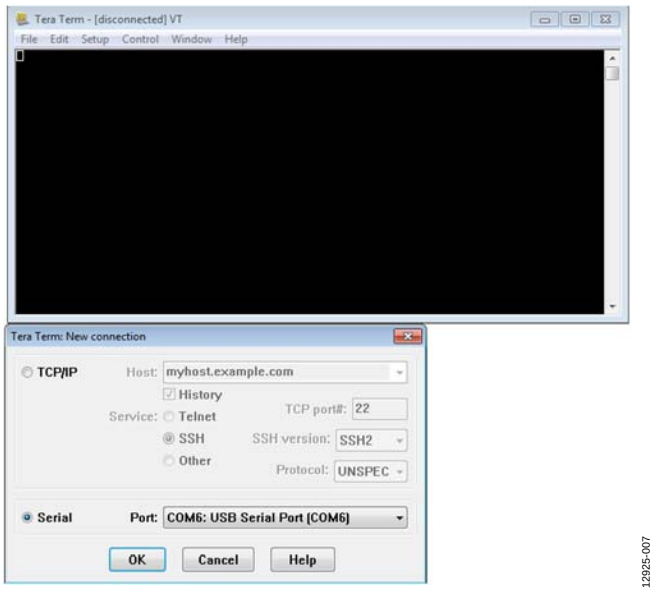

Figure 7. Tera Term COM6 for USB Transmission to the RS-485 Port on the EVAL-CN0373-EB1Z Board

Load the RS-485 data to be transmitted by clicking **Send** under the **File** menu. Choose any large data size file for continuous test transmission and click **Send**, as shown in Figure 8.

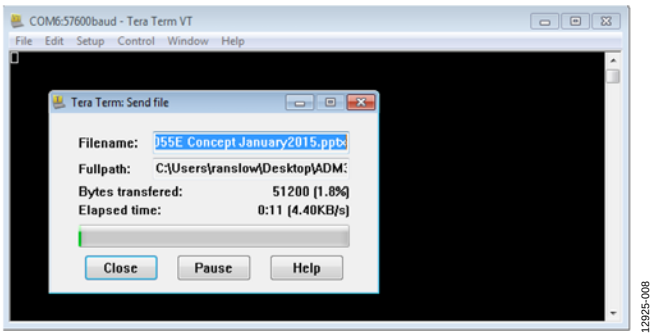

Figure 8. Tera Term COM6 Data for USB Transmission to the RS-485 Port on the EVAL-CN0373-EB1Z Board

Observe the isolated RS-485 signals on an oscilloscope by probing the Y and Z test points, or the differential bus signal by using the oscilloscope Y − Z Math function, as shown in Figure 9.

Figure 9. Math Y − Z Waveform for the RS-485 Port on the EVAL-CN0373-EB1Z Board

LEARN MORE

CN-0373 Design Support Package: www.analog.com/CN0373-DesignSupport

ezLINX™ *i*Coupler® Isolated Interface Development Environment, ezLINX Board Quick Start Guide.

Marais, Hein. AN-960 Application Note. *RS-485/RS-422 Circuit Implementation Guide.* Analog Devices, Inc.

Clark, Sean and Ronn Kliger. AN-740 Application Note. *iCoupler® Isolation in RS-232 Applications.* Analog Devices, Inc.

UG-400 User Guide. *ezLINX™ iCoupler® Isolated Interface Development Environment*. Analog Devices, Inc.

Data Sheets and Evaluation Boards

ADM2587E Data Sheet

ADM3252E Data Sheet

ADuM3160 Data Sheet

ADuM3070 Data Sheet

ADP190 Data Sheet

ADP7102 Data Sheet

ezLINX™ *i*Coupler® Isolated Interface Development Environment (EZLINX-IIIDE-EBZ)

REVISION HISTORY

4/15—Revision 0: Initial Version

Circuits from the Lab®
Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0376.

Devices Connected/Referenced	
AD7124-4	8-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADC with PGA and Reference
ADuM5010	2.5 kV rms, Isolated DC-to-DC Converter
ADuM1441	Micropower Quad-Channel Digital Isolator
ADP2441	36 V, 1 A, Synchronous, Step-Down DC-to-DC Regulator

Channel-to-Channel Isolated Temperature Input (Thermocouple/RTD) for PLC/DCS Applications

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0376 Circuit Evaluation Board (EVAL-CN0376-SDPZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 provides a dual-channel, channel-to-channel isolated, thermocouple or RTD input suitable for programmable logic controllers (PLC) and distributed control systems (DCS). The highly integrated design utilizes a low power, 24-bit, Σ-Δ analog-to-digital converter (ADC) with a rich analog and digital feature set that requires no additional signal conditioning ICs.

Each channel can accept either a thermocouple or a RTD input. The entire circuit is powered from a standard 24 V bus supply. Each channel measures only 27 mm × 50 mm.

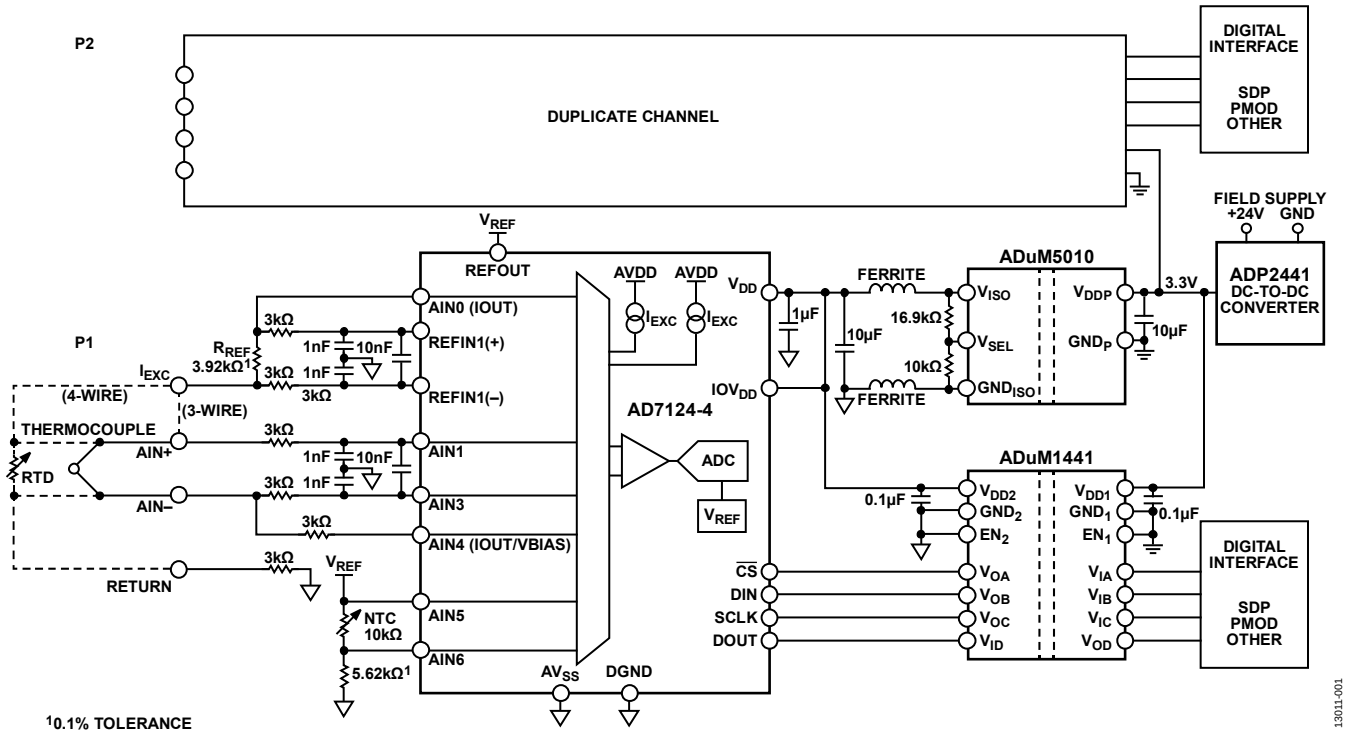

Figure 1. PLC/DCS Channel-to-Channel Isolated Temperature Input (Simplified Schematic: All Connections and Decoupling Not Shown)

Rev. 0

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CIRCUIT DESCRIPTION

The AD7124-4 24-bit, Σ-Δ ADC with programmable gain array (PGA) and voltage reference provides the complete set of features to implement a flexible input capable of connection to either thermocouple or RTD sensors. Features include on-chip reference, PGA, excitation currents, bias voltage generator, and flexible filtering with enhanced 50 Hz and 60 Hz rejection options. The AD7124-4 is in a small 5 mm × 5 mm LFCSP package, making it ideal in channel-to-channel isolated designs where space is a premium. It also includes multiple diagnostic functions that are available to the user.

The ADuM5010 isolated dc-to-dc converter provides 3.3 V isolated power via integrated *iso*Power® technology. The ADuM1441 isolates the serial peripheral interface (SPI) for the AD7124-4. The ADuM1441 micropower isolator consumes only 4.8 µA per channel when idle, resulting in an energy efficient solution.

The ADP2441 36 V, step-down, dc-to-dc regulator accepts an industrial standard 24 V supply, with wide tolerance on the input voltage. The ADP2441 steps the input voltage down to 3.3 V to power all of the controller-side circuitry.

System Overview

Channel-to-channel isolation is advantageous in automation systems, because faults on a particular input channel have no negative impact on other channels in the system. However, channel-to-channel isolated input modules present a significant design challenge in terms of complexity, space constraints, and system cost.

Both thermocouple or RTD inputs are commonly used in industrial automation systems; therefore, it is advantageous to design a temperature input module that handles both. This flexibility minimizes the design effort required for the two input module variants, and also offers flexibility to the module user.

The AD7124-4 significantly reduces the design complexity, providing a system-on-chip capable of performing all the necessary measurement functions for both thermocouple and RTD sensors.

Each channel of the circuit in Figure 1 measures only 27 mm by 50 mm, and this area can be further reduced by using both sides of the printed circuit board (PCB) for populating components. This small size is achieved because the AD7124-4 is in a small 5 mm × 5 mm LFCSP package and integrates almost all the required functions except the isolation and additional front-end filtering and protection. The isolation circuit consumes only 87 mm^2 for both the data and power isolation together, with a minimum combined width of 12.5 mm.

Terminal Connections

Figure 2 shows the terminal connections for each of the two input channels. These terminals correspond to P1 and P2 in the hardware (see Figure 1). The thermocouple as well as 2-, 3-, or 4-wire RTD connections are shown.

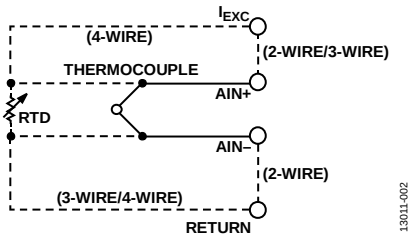

Figure 2. Terminal Connections (Per Channel)

Input Filtering

As shown in Figure 3, the input common-mode noise filtering is provided by R1, C1 and R2, C2, and has a 50 kHz cutoff frequency, approximately. Differential noise filtering is provided by R1, R2, and C3 and has a 2.5 kHz cutoff frequency, approximately. It is particularly important to filter out any interference at the Σ-Δ modulator frequency (307 kHz in full-power mode). It is suggested to adjust the cutoff of these filters to meet system bandwidth requirements, with the cutoff of the common-mode filters being approximately 10× the cutoff of the differential filter.

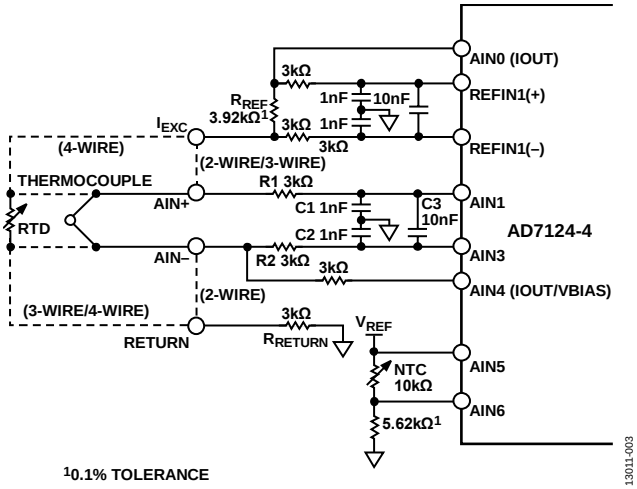

Figure 3. Front-End Filtering and Circuitry (Simplified)

Input Protection

To protect the input from an overvoltage condition, 3 kΩ resistors were placed on every input path to the AD7124-4. This resistor value limits the current from a 30 V dc overvoltage to less than 10 mA.

Consider the condition for 30 V connected between AIN+ and AIN−. Looking in from AIN+, the 30 V sees R1 (3 kΩ), followed by internal ESD protection diodes, followed by 3 kΩ looking out from AIN3 in parallel with 3 kΩ looking out from AIN4. Ignoring the internal ESD protection diodes, the total resistance seen between AIN+ and AIN− is 3 kΩ + 3 kΩ||3 kΩ = 4.5 kΩ. The current through the AD7124-4 is therefore limited to 30 V ÷ 4.5 kΩ = 6.7 mA.

RTD Input

The circuit in Figure 1 can be connected to 2-, 3-, or 4-wire RTDs. A resistance of up to 3.92 kΩ can be measured, making it suitable for Pt100 and Pt1000 RTDs. Current excitation is used, and the resistance measurement is a ratiometric measurement between the RTD and a precision 3.92 kΩ reference resistor (R_{REF}). As shown in Figure 3, the RTD measurement is made between AIN1 and AIN3, using REFIN1+ and REFIN1− as the reference input for the measurement. The excitation currents are set as follows:

- 2-wire mode: only the excitation on AIN0 is active, set at 250 µA.
- 3-wire mode: both the excitation currents on AIN0 and AIN4 are active, each set at 100 µA.
- 4-wire mode: only the excitation on AIN0 is active, set at 250 µA.

A high-side current sense technique is used. For low values of lead resistance to the RTD, this technique reduces the effect of any current mismatch in 3-wire mode. See the Circuit Note CN-0383 for more details on the 3-wire RTD configuration.

The reference resistor (R_{REF}) was chosen to be 3.92 kΩ, which allows measurement of a Pt1000 RTD up to 850°C (the RTD resistance is 3.9048 kΩ at 850°C). The value of R_{REF} must be selected based on the highest expected resistance for the RTD. The accuracy of the R_{REF} resistor has a direct impact on the measurement accuracy; therefore, a precision, low drift resistor must be used.

The excitation current must be set to 250 µA in 4-wire mode and 100 µA in 3-wire mode. For 4-wire mode, assume an RTD value of 3.92 kΩ. The excitation current coming from AIN0 passes through; $R_{REF} + R_{RTD} + R_{RETURN}$ = 3.92 kΩ + 3.92 kΩ + 3 kΩ = 10.84 kΩ. Therefore, the voltage at AIN0 is equal to 250 µA × 10.84 kΩ = 2.71 V. The AD7124-4 specifies an output compliance of AV_{DD} − 0.35 V on the excitation current outputs, which corresponds to 3.3 V − 0.35 V = 2.95 V. Because 2.95 V > 2.71 V, the 250 µA excitation current functions correctly even for the maximum RTD resistance.

See the Circuit Note CN-0381 for more details on the 4-wire RTD configuration.

In 3-wire mode, the lead compensation excitation current from AIN4 also flows through the 3 kΩ return resistor, producing an additional voltage at AIN0 of 250 µA × 3 kΩ = 0.75 V, thereby making the total voltage at AIN0 equal to 2.71 V + 0.75 V = 3.46 V, which violates the headroom requirement. Therefore, in 3-wire mode, the excitation currents must each be reduced to 100 µA to allow sufficient headroom.

The PGA gain can be used to increase the measurement resolution. For a Pt100 RTD, a gain of 8 is recommended (because Pt100 values are 10× smaller than Pt1000 values).

To achieve the desired accuracy, the RTD itself must be linearized in the software by the host controller, as described in the Circuit Note CN-0383.

Thermocouple Measurement

As shown in Figure 3, a thermocouple is connected between the AIN+ and AIN− terminals. The AIN4 pin provides a bias voltage for the thermocouple of 3.3 V ÷ 2 = 1.65 V. The thermocouple voltage is measured between AIN1 and AIN3, and because the thermocouple signals are very small, a PGA gain of 32 or 64 is typically recommended.

A 10 kΩ NTC thermistor is used for cold junction compensation. A reference voltage excitation, V_{REF}, is taken from REFOUT, and a precision, low-drift 5.62 kΩ resistor is placed in series to ground. The NTC resistance value can be calculated by

$$R_{NTC} = \frac{V_{NTC}}{V_{REF} - V_{NTC}} \times 5.62\ \text{k}\Omega$$

where:
V_{NTC} is the voltage measured between AIN1 and AIN3.
V_{REF} is the reference voltage from the AD7124-4 REFOUT.

Any temperature difference between the terminal block and the NTC temperature sensor directly impacts the resulting temperature reading for the thermocouple input. For this reason, the NTC thermistor must be placed as close to the terminal block as possible to maximize the thermal coupling.

To achieve the desired accuracy, the thermocouple and NTC must be linearized in the software by the host controller, as described in the Circuit Note CN-0384.

Diagnostics

The AD7124-4 provides a number of system level diagnostics, including

- Reference detection
- Overvoltage/undervoltage detection on the input
- CRC on SPI communications
- CRC on the memory map
- SPI read/write checks

These diagnostics allow a high level of fault coverage for the input channels.

Isolation

The data channels are isolated using the ADuM1441, a quad-channel, micropower isolator, resulting in an energy efficient solution. The ADuM1441 is in a small 5 mm × 6.2 mm, 16-lead QSOP package (30 mm^2).

The ADuM5010, a complete isolated switching converter utilizing *iso*Power technology, provides power isolation for the circuit. The ADuM5010 is in a small 7.4 mm × 7.5 mm, 20-lead SSOP package (56.25 mm^2).

Figure 4 shows details of the ADuM5010 circuitry. Ferrite beads are used on the secondary side of the supply to suppress any potential electromagnetic interference (EMI) emissions. The ferrite beads (Murata BLM18HK102SN1) are specifically chosen for their high impedance from 100 MHz to 1 GHz. Decoupling capacitors of 10 µF and 0.1 µF are also used. Both the ferrite beads and the capacitors use short traces to the ADuM5010 pins to minimize parasitic inductance and resistance.

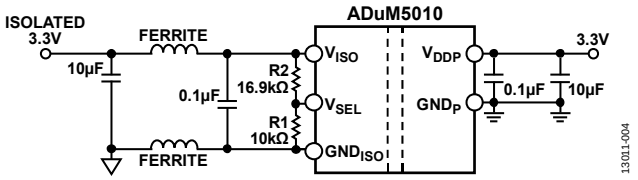

Figure 4. isoPower Circuit with Ferrite Beads and Decoupling Capacitors

The stitching capacitance is kept to a minimum size because the ferrite beads significantly reduce the emissions. The PCB area between the ADuM5010 supply, the GND pins, and the ferrite beads is kept clear of any ground planes or traces to minimize the capacitive coupling of any high frequency noise into the ground plane. See the AN-0971 Application Note for additional information on controlling radiated emissions from *iso*Power devices.

The R1 and R2 feedback resistors are chosen to select a 3.3 V output as per the ADuM5010 data sheet.

Power Consumption per Channel

The ADuM5010 typically consumes 3.3 mA from the controller-side supply. The efficiency of the ADuM5010 is only 27% at full load; therefore, minimizing the current drawn from field side significantly impacts the energy efficiency of the channel.

The AD7124-4 consumes ~994 µA (full power mode, gain = 32, TC bias, diagnostics and internal reference enabled). The AD7124-4 power can be significantly reduced by using the mid power or low power modes.

For the ADuM1441, the field side consumes a total of approximately 7.2 µA when idle and 552 µA when operating at 2 Mbps. If the interface is active 1/8th of the time, the power consumption for the ADuM1441 is (552 µA × 0.125) + (7.2 µA × 0.875) = 75.3 µA total.

The measured power consumption for an input channel operating in full power mode, gain = 32, internal reference, and TC bias enabled was 7.9 mA from the controller-side 3.3 V supply.

Power Supply Circuit

The evaluation board is powered by a 4.5 V to 36 V dc power supply and uses an on-board switching regulator to provide the 3.3 V supply to the system, as shown in Figure 5. The EVAL-SDP-CB1Z System Demonstration Platform (SDP) board provides a regulated 3.3 V for the digital interface.

The ADP2441 includes programmable soft start, regulated output voltage, switching frequency, and power good. These features are programmed externally via tiny resistors and capacitors. The ADP2441 also includes protection features, such as undervoltage lockout (UVLO) with hysteresis, output short-circuit protection, and thermal shutdown.

A 300 kHz switching frequency maximizes the efficiency of the ADP2441. Due to the high switching frequency of the ADP2441, using shielded ferrite core inductors is recommended because of their low core losses and low EMI.

In the Figure 5 circuit, the switching frequency is set to approximately 300 kHz using a 294 kΩ external resistor. The inductor value of 22 µH (Coilcraft LPS6235-223MLC) was chosen using the downloadable ADP2441 Buck Regulator Design Tool. This tool selects the best component values based on the required operating conditions (4.5 V to 36 V input, 3.3 V output, 1 A output current).A current of 1 A was selected to power additional circuits on the host controller side if required.

A complete set of documentation for the EVAL-CN0376-SDPZ circuit evaluation board including schematic, assembly, layout, Gerbers, and bill of materials is available at www.analog.com/CN0376-DesignSupport.

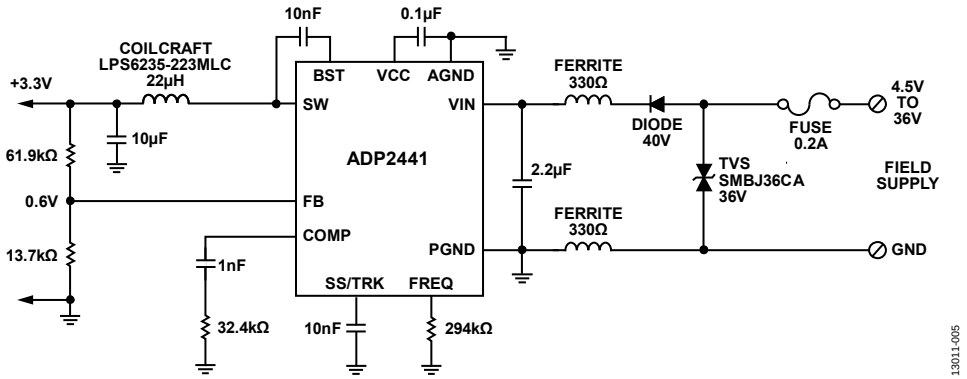

Figure 5. Power Supply Circuit (Simplified Schematic: All Connections Not Shown)

Testing Results

For detailed performance analysis of the thermocouple, 3-wire and 4-wire RTD circuits, see the Circuit Note CN-0381, Circuit Note CN-0383, and Circuit Note CN-0384 for in depth analysis and measurement results.

Figure 6 shows a histogram for the EVAL-CN0376-SDPZ using the 25 SPS post filter, with AIN+ shorted to AIN–, gain = 32, and TC bias enabled. The data corresponds to 17.85-bit noise-free code resolution.

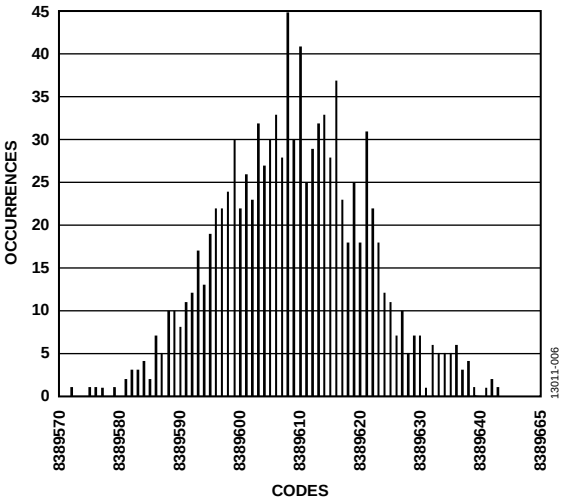

Figure 6. Histogram of Codes for the AIN+ and AIN- Shorted Inputs (25 SPS, Post Filter Selected, Gain = 32, TC Bias Enabled)

COMMON VARIATIONS

If more channels are needed, the AD7124-8 can be used. The AD7124-8 has 8 differential or 16 single-ended inputs. The AD7792 can also be considered as a lower cost option, but with reduced features and performance.

Alternate options for the data isolation are to use a SPIsolator™ such as the ADuM3151, which supports up to 17 MHz SPI transmission as well as containing three general-purpose, low speed, isolated channels.

An NTC thermistor is used for cold junction compensation in the circuit shown in Figure 1. Another option is to use the ADT7320 digital temperature sensor, which is 0.25°C accurate. (see the Circuit Note CN-0172).

CIRCUIT EVALUATION AND TEST

The circuit shown in Figure 1 uses the EVAL-CN0376-SDPZ evaluation board and the EVAL-SDP-CB1Z SDP controller board.

The EVAL-CN0376-SDPZ evaluation board features PMOD-compatible headers for integration with external controller boards.

The CN-0376 Evaluation Software communicates with the SDP board to configure and capture data from the EVAL-CN0376-SDPZ evaluation board.

Equipment Needed

The following equipment is needed:

- PC with a USB port and Windows® Vista (32-bit) or Windows 7 (32-bit)
- EVAL-CN0376-SDPZ circuit evaluation board
- EVAL-SDP-CB1Z SDP controller board
- CN-0376 Evaluation Software
- Precision voltage and resistance source, or alternately a thermocouple or RTD simulator.
- Power supply: 4.5 V to 36 V dc at 100 mA

Getting Started

Install the CN-0376 Evaluation Software, which is available for download at ftp://ftp.analog.com/pub/cftl/CN0376/. Follow the on-screen prompts to install and use the software. More information is available in the CN-0376 Software User Guide.

Test Setup Functional Block Diagram

Figure 7 shows a functional block diagram of the test setup.

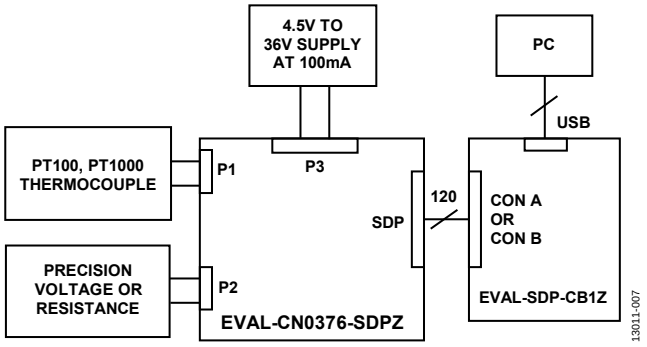

Figure 7. Test Setup Functional Block Diagram

Setup

The EVAL-CN0376-SDPZ evaluation board connects to the EVAL-SDP-CB1Z SDP board through a 120-pin mating connector found on both boards. The CN-0376 Evaluation Software and the SDP board allow the data to be analyzed using a PC.

Apply a voltage in the range of 4.5 V to 36 V (24 V nominal) to the P3 connector. Ensure that the P8 jumper is set to EXT (default), which powers the board via the P3 supply input.

External controllers can also be used to communicate with and power the evaluation board using the PMOD headers for SPI communication. If desired, set the P8 jumper to VCC_PMOD to power the board from 3.3 V via the PMOD connector.

Precision voltage and resistance sources can be used as input to the analog front end to evaluate system performance. Similarly, thermocouple or RTD simulators can be used.

Figure 8 shows a photo of the EVAL-CN0376-SDPZ circuit evaluation board.

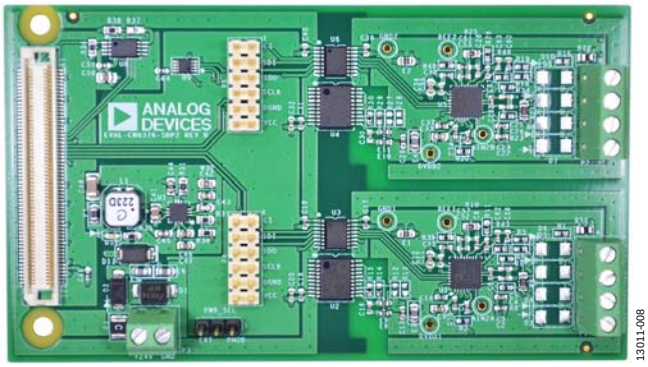

Figure 8. Photo of EVAL-CN0376-SDPZ Circuit Evaluation Board

LEARN MORE

CN-0376 Design Support Package: www.analog.com/CN0376-DesignSupport

SDP-B User Guide

CN-0376 Software User Guide

Duff, Matthew and Joseph Towey. *Two Ways to Measure Temperature Using Thermocouples Feature Simplicity, Accuracy, and Flexibility*. Analog Dialogue 44-10, Analog Devices.

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MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND".* Analog Devices.

MT-101 Tutorial. *Decoupling Techniques.* Analog Devices.

Circuit Note CN-0172. *3-Channel Thermocouple Temperature Measurement System with 0.25 °C Accuracy.* Analog Devices.

Circuit Note CN-0206. *Thermocouple Temperature Measurement System with Less Than 500 µA Current Drain.* Analog Devices.

Circuit Note CN-0209. *Fully Programmable Universal Analog Front End for Process Control Applications.* Analog Devices.

Circuit Note CN-0325. *PLC/DCS Universal Analog Input Using Either 4 or 6 Pin Terminal Block.* Analog Devices.

Circuit Note CN-0381. *Completely Integrated 4-Wire RTD Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC.* Analog Devices.

Circuit Note CN-0382. *Isolated 4 mA to 20 mA/HART Temperature and Pressure Industrial Transmitter using a Low Power, Precision, 24-Bit, Sigma-Delta ADC.* Analog Devices.

Circuit Note CN-0383. *Completely Integrated 3-Wire RTD Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC.* Analog Devices.

Circuit Note CN-0384. *Completely Integrated Thermocouple Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC.* Analog Devices.

Data Sheets and Evaluation Boards

CN-0376 Circuit Evaluation Board (EVAL-CN0376-SDPZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

AD7124-4 Data Sheet

ADuM1441 Data Sheet

ADuM5010 Data Sheet

ADP2441 Data Sheet

REVISION HISTORY

7/15—Revision 0: Initial Version

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0381.

Devices Connected/Referenced	
AD7124-4/ AD7124-8	4-Channel/8-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADCs with PGA and Reference
ADP1720	50 mA, High Voltage, Micropower Linear Regulator

Completely Integrated 4-Wire RTD Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

AD7124-4 Evaluation Board (EVAL-AD7124-4SDZ) or AD7124-8 Evaluation Board (EVAL-AD7124-8SDZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is an integrated 4-wire, resistance temperature detector (RTD) system based on the AD7124-4/ AD7124-8 low power, low noise, 24-bit Σ-Δ ADC optimized for high precision measurement applications. With a two-point calibration and linearization, the overall 4-wire system accuracy is better than ±1°C over a temperature range of −50°C to +200°C. Typical noise free code resolution of the system is 17.9 bits for full power mode, sinc^4 filter selected, at an output data rate of 50 SPS, and 17.3 bits for low power mode, post filter selected, and at an output data rate of 25 SPS.

The AD7124-4 can be configured for 4 differential or 7 pseudo differential input channels, while the AD7124-8 can be configured for 8 differential or 15 pseudo differential input channels. The on-chip programmable gain array (PGA) ensures that signals of small amplitude can be interfaced directly to the ADC.

The AD7124-4/AD7124-8 establishes the highest degree of signal chain integration, which include programmable low drift excitation current sources. Therefore, the design of an RTD system is greatly simplified because most of the required RTD measurement system building blocks are included on-chip.

The AD7124-4/AD7124-8 gives the user the flexibility to employ one of three integrated power modes, where the current consumption, range of output data rates, and rms noise are tailored with the power mode selected. The current consumed by the AD7124-4/AD7124-8 is only 255 µA in low power mode and 930 µA in full power mode. The power options make the device suitable for non-power critical applications, such as input/output modules, and also for low power applications such as loop powered smart transmitters where the complete transmitter must consume less than 4 mA.

The device also has a power-down option. In power-down mode, the complete ADC along with its auxiliary functions are powered down so that the device consumes 1 µA typical. The AD7124-4/ AD7124-8 also has extensive diagnostic functionality integrated as part of its comprehensive feature set.

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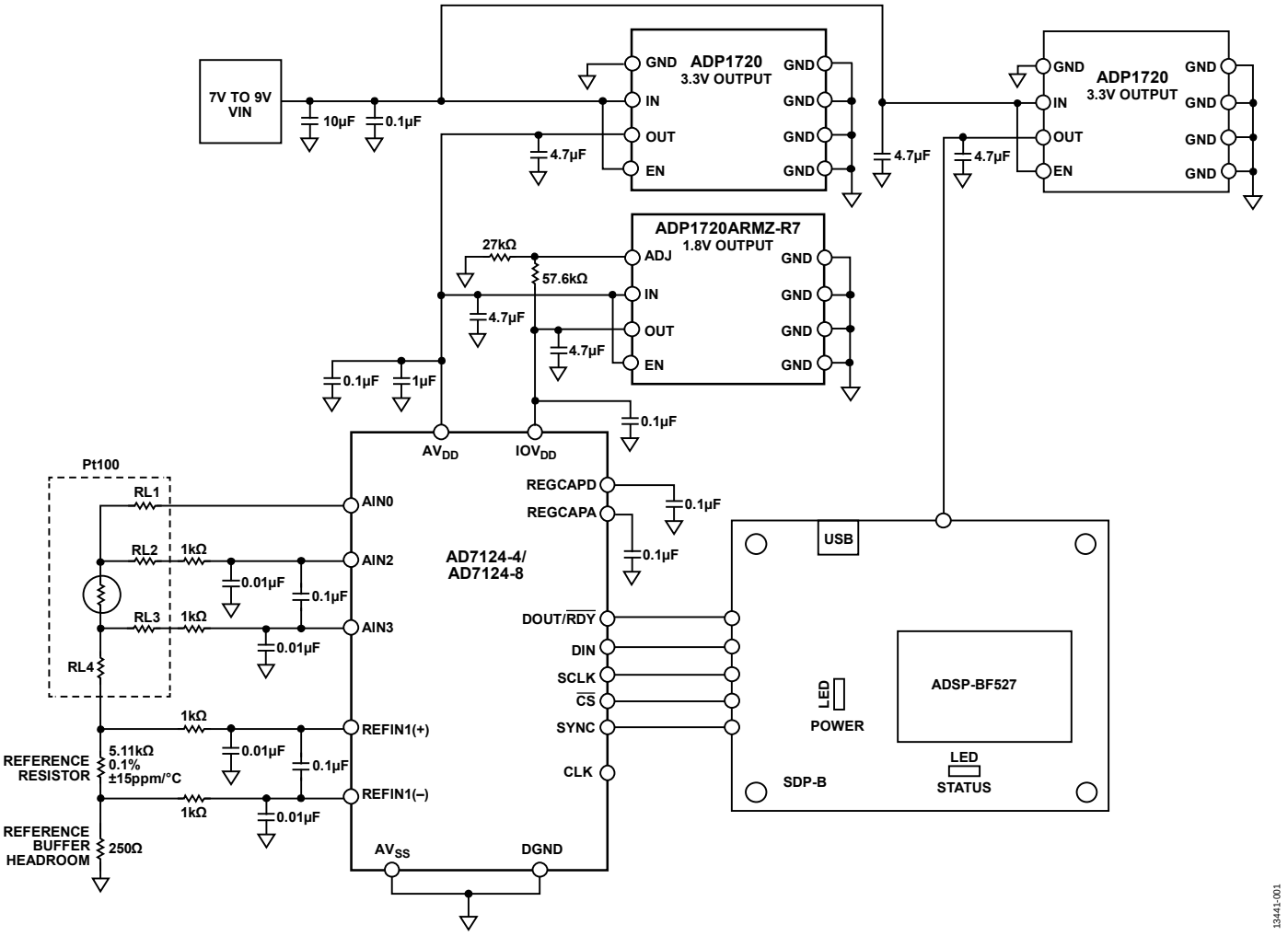

Figure 1. 4-Wire RTD Measurement Configuration

CIRCUIT DESCRIPTION

RTD Temperature Measurement Introduction

RTDs are frequently used sensors for temperature measurements in industrial applications. An RTD is made from a pure metal (examples include platinum, nickel, or copper), which has a predictable change in resistance as the temperature changes. The most widely used RTDs are platinum Pt100 and Pt1000. RTDs are capable of high accuracy and good stability when compared with other types of temperature sensors. The error due to the resistance of long wire lengths can be eliminated using the 4-wire connection.

To accurately measure the resistance, a voltage is generated across the RTD by a constant current source. The AD7124-4/ AD7124-8 offers two such excitation current sources that are register programmable from 50 µA to 1 mA. Errors in the current source can be easily cancelled by referring the measurement to the voltage across a precision reference resistor that is driven with the same current source, resulting in a ratiometric measurement.

For the circuit in Figure 1, a Pt100 RTD Class B sensor was used. Pt100 RTDs measure temperature from −200°C to +600°C. The resistance of a Class B RTD is typically 100 Ω at 0°C and has a typical temperature coefficient of ~0.385 Ω/°C (see Figure 2). Using this information, the voltage generated across the Pt100 RTD can easily be calculated based on the current source selected.

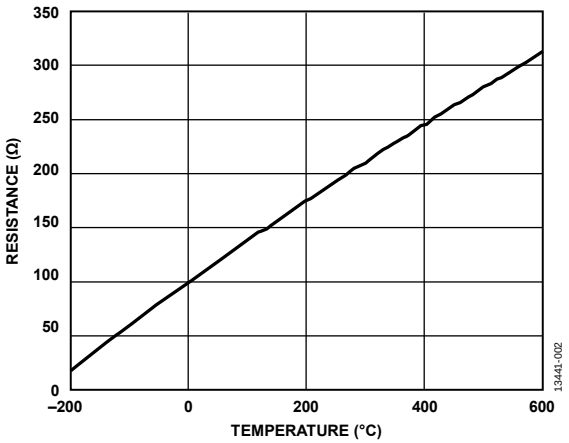

Figure 2. Pt100 RTD Resistance vs. Temperature

How the Circuit Works

The AD7124-4/AD7124-8 provides an integrated solution for RTD measurements; it can achieve high resolution, low non-linearity, and low noise performance as well as very high 50 Hz and 60 Hz rejection. The AD7124-4/AD7124-8 consists of an on-chip, low noise PGA that amplifies the small signal from the RTD with a gain programmable from 1 to 128, thus allowing direct interface with the sensor. The gain stage has high input impedance and limits the input leakage current to 3.3 nA typical for full power mode and 1 nA typical for low power mode. The following sections explain the different elements that make up the 4-wire RTD temperature measurement system.

Power Supplies

The AD7124-4/AD7124-8 has separate analog and digital power supplies. The digital power supply, IOV_{DD}, is independent of the analog power supply and can be 1.65 V to 3.6 V referenced to DGND. The analog power supply, AV_{DD}, is referred to AV_{SS} and has a range of 2.7 V to 3.6 V for low and mid-power modes, and 2.9 V to 3.6 V for full power mode. The circuit shown in Figure 1 operates on a single supply; therefore, AV_{SS} and DGND are connected together, and only one ground plane is used. The AV_{DD} and IOV_{DD} voltages are generated separately using ADP1720 low dropout voltage regulators. The AV_{DD} voltage is set to 3.3 V, and the IOV_{DD} voltage is set to 1.8 V, using the ADP1720 regulators. Using separate regulators ensures lowest noise.

Serial Peripheral Interface (SPI)

SPI communications to the AD7124-4/AD7124-8 are handled by the Blackfin® ADSP-BF527 on the EVAL-SDP-CB1Z board, as shown in Figure 1. To access the registers of the AD7124-4/AD7124-8, use the AD7124-4/AD7124-8 EVAL+ Software. Figure 3 shows the main window of this software. Clicking the **4-WIRE RTD** button configures the software for the 4-wire RTD measurement.

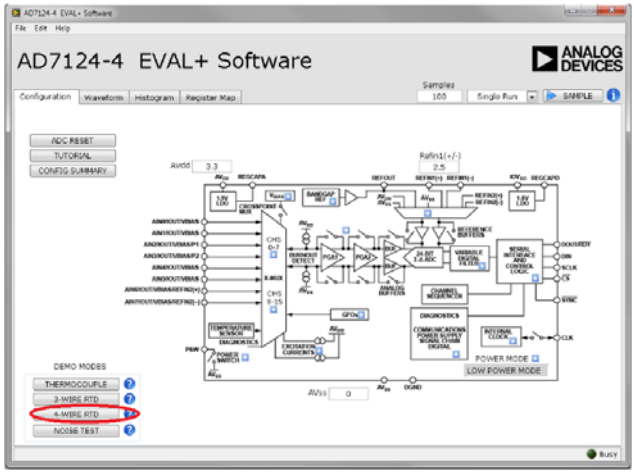

Figure 3. AD7124-4/AD7124-8 EVAL+ Software Configuration Window

The AD7124-4/AD7124-8 has diagnostic functions on-chip that can be used to detect faults in the SPI communication. These diagnostics include checks on the SPI read and write operations, ensuring that only valid registers are accessed. An SCLK counter ensures that the correct number of SCLK pulses is used, while the CRC functionality checks for changes in bit values during transmission. When any of these SPI communication diagnostic functions are enabled and an associated error occurs, the corresponding flag is set in the error register. All enabled flags are OR'ed together and control the ERR flag in the status register. This functionality is particularly useful if the status bits are appended to the ADC conversions.

Analog Inputs and Reference

The AD7124-4 can be configured for 4 differential or 7 pseudo differential input channels, while the AD7124-8 can be configured for 8 differential or 15 pseudo differential input channels.

The AD7124-4/AD7124-8 has on-chip diagnostics that can be used to check that the voltage level on the analog pins are within the specified operating range. The positive (AINP) and negative (AINM) analog inputs can be separately checked for overvoltages and undervoltages, as well as ADC saturation. An overvoltage is flagged when the voltage on the analog input exceeds AV_{DD}, while an undervoltage is flagged when the voltage on the analog input goes below AV_{SS}.

For the circuit in Figure 1, three analog pins are used to implement the 4-wire measurement: AIN0, AIN2, and AIN3. AIN2 and AIN3 are configured as a fully differential input channel and are used for sensing the voltage across the RTD. The excitation current source used to excite the RTD is generated from AV_{DD} and is directed to AIN0. The analog pins and their configuration are shown in greater detail in Figure 4.

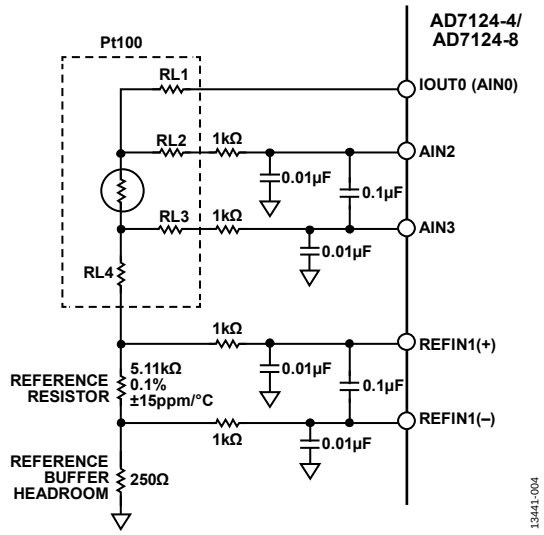

Figure 4. Analog Input Configuration for 4-Wire RTD Measurement

Digital and Analog Filtering

For the circuit in Figure 1, the reference input used is REFIN1(±). The current through the RTD also flows through the precision reference resistor that generates the reference voltage. The voltage generated across this precision reference resistor is ratiometric to the voltage across the RTD; therefore, any variations seen in the excitation current are removed. Because the buffers are enabled, it is necessary to ensure that the headroom required for correct operation is met (AV_{DD} − 0.1 V and AV_{SS} + 0.1 V). The headroom of 0.125 V (500 µA × 250 Ω) is provided by the 250 Ω resistor to ground, as shown in Figure 4.

Differential (~800 Hz cutoff) and common-mode (~16 kHz cutoff) filters are implemented at the analog inputs, as well as at the reference inputs. This filtering is required to reject any interference at the modulator frequency and also any multiples of this frequency.

The AD7124-4/AD7124-8 offers a great deal of on-chip digital filtering flexibility. Several filter options are available; the option selected has an effect on the output data rate, settling time, as well as 50 Hz and 60 Hz rejection. For this circuit note, the sinc^4 filter and the post filter are implemented. The sinc^4 filter is used because it has excellent noise performance across the range of output data rates, as well as having excellent 50 Hz and 60 Hz rejection. The post filter provide simultaneous 50 Hz and 60 Hz rejection, with a 40 ms settling time.

Calibration

The AD7124-4/AD7124-8 provides different calibration modes that can be used to eliminate offset and gain errors. For this circuit note, internal zero-scale calibration as well as internal full-scale calibrations were used.

4-Wire RTD Configuration

The circuit shown in Figure 1 is designed for precision 4-wire RTD measurements using the AD7124-4/AD7124-8. For the 4-wire RTD measurement, one excitation current source is required. The AD7124-4/AD7124-8 provides two matched current sources; therefore, either one of these current sources can be used to excite the RTD. The RTD produces a low-level voltage signal, which can then be amplified by the on-board PGA of the AD7124-4/AD7124-8. The amplified voltage is then converted to a precision digital representation using the 24-bit Σ-Δ ADC.

For this 4-wire RTD circuit, a Class B RTD is used. If the on-chip excitation current is programmed to 500 µA, at a maximum temperature of 600°C, the voltage generated across the RTD is approximately 156.85 mV. To ensure that the maximum range of the AD7124-4/AD7124-8 is used, the PGA gain is programmed to a gain of 16. The PGA amplifies the maximum RTD sensor output voltage to 2.5096 V.

The value of the external precision resistor is chosen so that the maximum voltage generated across the RTD equals the reference voltage divided by the PGA gain.

$$R_{REF} = V_{RTD\,MAX}/I_{EXC} = 2.5096\text{ V}/500\ \mu\text{A} = 5020\ \Omega$$

Therefore, a 5.11 kΩ resistor is used, which gives a reference voltage of

$$5.11\text{ k}\Omega \times \textit{Excitation Current} = 5.11\text{ k}\Omega \times 500\ \mu\text{A} = 2.555\text{ V}$$

The output compliance of the excitation current source must also be considered when making 4-wire RTD measurements using the AD7124-4/AD7124-8. The output compliance is dependent on the excitation current selected. For this circuit, 500 µA is selected, which has an output compliance voltage of AV_{DD} − 0.37 V. The AV_{DD} supply voltage for this circuit is 3.3 V; therefore, the output compliance level for the excitation current source must be less than 2.93 V. From the previous calculations, this specification is met, because the maximum voltage on the AIN0 pin is the voltage across the precision reference resistor plus the voltage across the RTD plus the voltage across the headroom resistor.

$$V_{REF} + V_{RTD} + V_{HEADROOM} = 2.555\text{ V} + 156.8\ 5\text{ mV} + 125\text{ mV} = 2.83685\text{ V}$$

The AD7124-4/AD7124-8 configuration for 4-wire RTD measurements is as follows:

- Differential input: AINP = AIN2, AINM = AIN3
- Excitation current: IOUT0 = AIN0 = 500 µA
- Gain = 16
- Precision reference resistor: 5.11 kΩ
- Digital filtering:
  - Sinc^4 filter (full power mode)
  - Post filter (low power mode)

The general expression to calculate the RTD resistance, R_{RTD}, when the ADC is operating in bipolar differential mode is given by

$$R_{RTD} = \frac{(CODE - 2^{N-1}) \times R_{REF}}{G \times 2^{N-1}} \quad (1)$$

where:
CODE is the ADC code output.
N is the resolution of the ADC (24, in this case).
R_{REF} is the reference resistor.
G is the selected gain.

From the specification of the Class B RTD, the resistance changes by approximately 0.385 Ω/°C. This relationship can be used as a quick method to obtain an approximate temperature of the RTD. This method has inaccuracies due to the temperature coefficient of the RTD changing slightly over the temperature range; however, it can be a useful method to check the temperature quickly.

To calculate the approximate temperature, use Equation 2.

$$\textit{Temperature}\ (°\text{C}) = \frac{R_{RTD} - 100}{0.385} \quad (2)$$

The RTD transfer function known as the Callender-Van Dusen equation is made up of two distinct polynomial equations to provide a more accurate result. Equation 3 is used for temperatures greater than 0°C, and Equation 4 is for temperatures less than 0°C.

The equation for temperature $t \leq 0°C$ is

$$R_{RTD}(t) = R_0[1 + At + Bt^2 + C(t - 100°C)t^3] \quad (3)$$

The equation for temperature $t \geq 0°C$ is

$$R_{RTD}(t) = R_0(1 + At + Bt^2) \quad (4)$$

where:
t is the RTD temperature (°C).
$R_{RTD}(t)$ is the RTD resistance (Ω).
R_0 is the RTD resistance at 0°C (in this case, R_0 = 100 Ω).
$A = 3.9083 \times 10^{-3}$.
$B = -5.775 \times 10^{-7}$.
$C = -4.23225 \times 10^{-12}$.

There are many different ways to determine the temperature as a function of the RTD resistance given the transfer function in Equation 3 and Equation 4. The direct mathematical method is chosen, due to its accuracy. Taking Equation 3, the temperature can be calculated as

$$T_{RTD}\ (°C) = \frac{-A + \sqrt{A^2 - 4B\left(1 - \frac{r}{R_0}\right)}}{2B} \quad (5)$$

where r is the RTD resistance, and the other variables are as defined previously.

This method works well for temperatures greater than or equal to 0°C. To calculate the RTD temperature for temperatures below 0°C, a best fit polynomial expression is required, and the polynomial used in this circuit note is a fifth-order polynomial shown in Equation 6.

$$T_{RTD}\ (°C) = -242.02 + 2.2228 \times r + (2.5859 \times 10^{-3})r^2 - (48260 \times 10^{-6})r^3 - (2.8183 \times 10^{-3})r^4 + (1.5243 \times 10^{-10})r^5 \quad (6)$$

As an example, if the code read back from the AD7124-4/AD7124-8 with the temperature set to 25°C is 11270065, converting this code to a resistance using Equation 1 gives

$$R_{RTD} = \frac{(11270065 - 2^{23}) \times R_{REF}}{G \times 2^{23}} = 109.704\ \Omega$$

Linearization using Equation 5 gives a temperature of 24.921°C.

As a second example, if the code read back from the AD7124-4/AD7124-8 with the temperature set to −25°C is 10757779, converting this code to a resistance gives

$$R_{RTD} = \frac{(10757779 - 2^{23}) \times R_{REF}}{G \times 2^{23}} = 90.200\ \Omega$$

Linearization using Equation 6 gives a temperature of −24.982°C.

4-Wire RTD Measurements and Results

For the circuit shown in Figure 1, data was gathered for different digital filter and power mode configurations of the AD7124-4/AD7124-8, with the sinc^4 filter operating in full power mode, and the post filter operating in low power mode.

Choosing the configuration for sinc^4 filter, full power mode, and 50 SPS allows the user to operate the AD7124-4/AD7124-8 for best performance relative to speed and noise. Figure 5 shows the noise distribution when a 4-wire RTD is connected as shown in Figure 1 at ambient temperature. The corresponding rms noise is typically 199.37 nV, which is approximately 17.9 noise free bits. The noise performance of the AD7124-4/AD7124-8 for inputs shorted using the same filter, gain, power mode, and output data rate was 100 nV rms or 18.7 noise free bits. The increase in the noise comes directly from the RTD connection across the input channel (AIN2, AIN3).

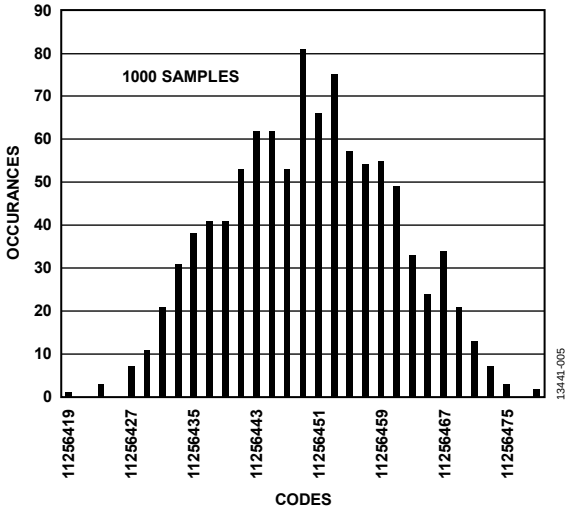

Figure 5. Histogram of Codes for RTD at Ambient Temperature, Sinc^4 Filter, Full Power Mode, 50 SPS

For the 4-wire RTD configuration where the sinc^4 filter and full power mode were selected, the temperature of the RTD was swept from −50°C to +200°C. For each temperature, the corresponding voltage across the RTD was measured using the AD7124-4/AD7124-8 as described previously. This voltage was then converted to a resistance, which was then linearized, and converted to a temperature as described in the 4-Wire RTD Configuration section. Figure 6 shows the resulting error between the set temperature and the measured temperatures of the RTD after linearization. For each RTD temperature setting, the AD7124-4/AD7124-8 is kept at 25°C. As shown in Figure 6, the error of the RTD temperature measured is well within the error window of the Pt100 Class B RTD after linearization. Figure 6 also shows the deviation of the RTD error across different AD7124-4/AD7124-8 temperature settings. For each AD7124-4/AD7124-8 temperature setting, an internal zero-scale and full-scale calibration is carried out. As shown in Figure 6, the error of the RTD is well within the expected error of the Class B RTD for all temperature settings of the AD7124-4/AD7124-8.

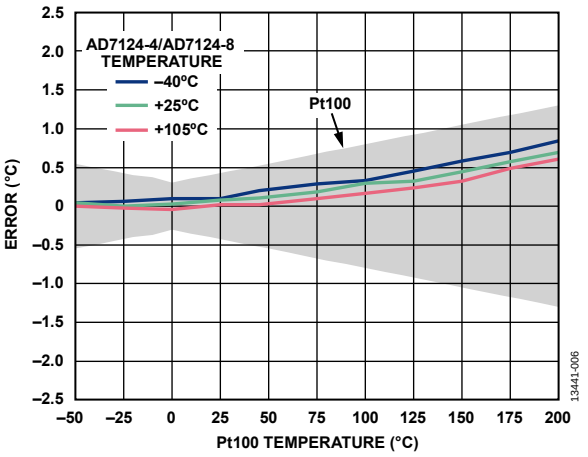

Figure 6. Temperature Accuracy Measurement, Sinc⁴ Filter, Full Power Mode, 50 SPS

Figure 7 shows the error in measured RTD temperature for a one time, internal zero-scale and full-scale calibration carried out at 25°C. From the plot, it can be seen that carrying out a one time calibration at 25°C or calibrating at each individual temperature of the AD7124-4/AD7124-8 gives the same performance.

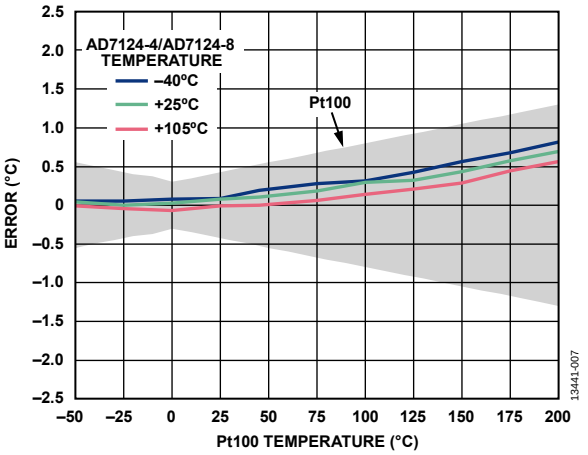

Figure 7. Temperature Accuracy Measurement, Sinc⁴ Filter, Full Power Mode, 50 SPS, One Time 25°C Calibration Only

The second AD7124-4/AD7124-8 configuration tested was the low power mode, where the post filter and 25 SPS output data rate were selected. The 25 SPS filter provides simultaneous 50 Hz and 60 Hz rejection and allows the user to trade off settling time with power supply rejection. Figure 8 shows the resulting noise distribution when a 4-wire RTD is connected as shown in Figure 1 at ambient temperature. The corresponding rms noise is typically 774 nV, equating to approximately 16.8 noise free bits. The noise performance of the AD7124-4/AD7124-8 for inputs shorted with the same filter, gain, power mode, and output data rate is typically 360 nV rms or 17.3 noise free bits. The increase in the noise between the two measurements comes directly from the RTD connection across the input channel (AIN2, AIN3).

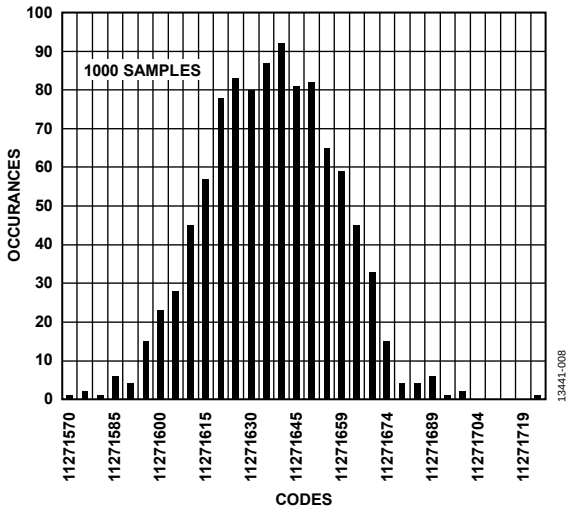

Figure 8. Histogram of Codes for RTD at Ambient Temperature, Post Filter, Low Power Mode, 25 SPS

The temperature of the RTD was swept from −50°C to +200°C. For each of the set RTD temperatures, the corresponding voltage across the RTD was measured using the AD7124-4/AD7124-8 as described previously. The voltage was then converted to a resistance, which was then linearized and converted to a temperature as described in the 4-Wire RTD Configuration section. Figure 9 shows the resulting error between the set and measured temperatures of the RTD after linearization. For each RTD temperature setting, the AD7124-4/AD7124-8 is kept at 25°C. As shown in Figure 9, the error of the RTD temperature measured is well within the error window of the Pt100 Class B RTD. Figure 9 also shows the deviation of the RTD error across different AD7124-4/AD7124-8 temperature settings. For each AD7124-4/AD7124-8 temperature setting, an internal zero-scale and full-scale calibration was carried out. As shown in Figure 9, the error of the RTD is well within the expected error of the Class B RTD for all temperature settings of the AD7124-4/AD7124-8.

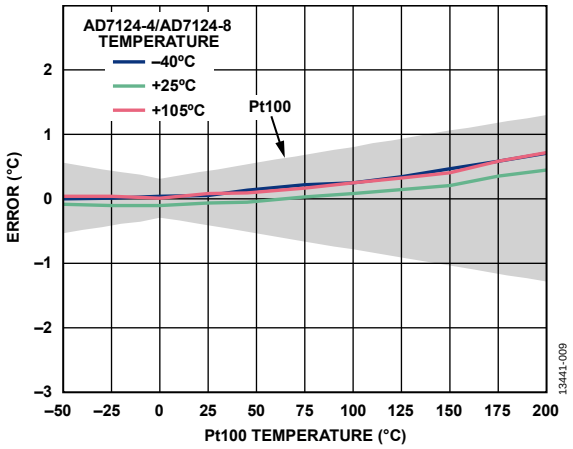

Figure 9. Temperature Accuracy Measurement, Post Filter, Low Power Mode, 25 SPS

Figure 10 shows the error in measured RTD temperature for a one time, internal zero-scale and full-scale calibration carried out at 25°C. From the plot, it can be seen that carrying out a one time calibration at 25°C or calibrating at each individual temperature of the AD7124-4/AD7124-8 gives similar performance.

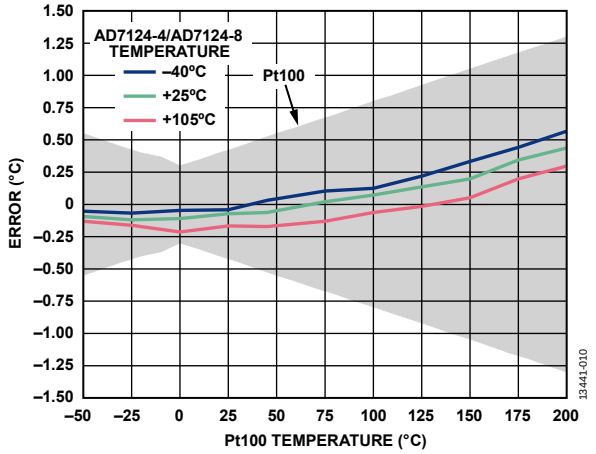

Figure 10. Temperature Accuracy Measurement, Post Filter, Low Power Mode, 25 SPS, 25°C One Time Calibration Only

COMMON VARIATIONS

Multiple 4-Wire RTDs

The AD7124-4/AD7124-8 can be used as a measurement system for multiple 4-wire RTDs. The AD7124-4 can be used to connect two 4-wire RTDs, while the AD7124-8 can be used to connect up to five 4-wire RTDs. The same reference input can be used for all the RTDs, and one current source can be used to excite all the RTDs. The current is directed to the top side of each of the RTDs in turn when the RTD temperature measurement is required. The cross multiplexer on the AD7124-4/AD7124-8 allows multiple channels to be configured separately, where each channel can be configured for different setups.

The steps needed to measure an RTD voltage are

1. Set the external reference to REFIN1±.
2. Enable the IOUT0 current to the RTD to be measured.
3. Enable the analog input channel that has the RTD connected across its input.

As an example, two 4-wire RTDs were connected to the AD7124-4 as shown in Figure 11. One 4-wire RTD is connected across the AIN2 and AIN3 analog input pins (Channel 0 configuration), where the excitation current comes from AIN0, and a second 4-wire RTD is also shown connected across the AIN6 and AIN7 analog input pins (Channel 1 configuration), where AIN1 is used for the excitation current. Temperature measurements were then carried out on each RTD in turn using the following steps:

1. IOUT0 is directed to AIN0. The voltage is measured on Channel 0 (AIN2, AIN3); therefore, Channel 0 must be enabled. All other channels are disabled for this measurement.
2. Disable Channel 0, enable Channel 1, and direct the IOUT0 current to AIN1. The voltage is then measured on Channel 1 (AIN6, AIN7).

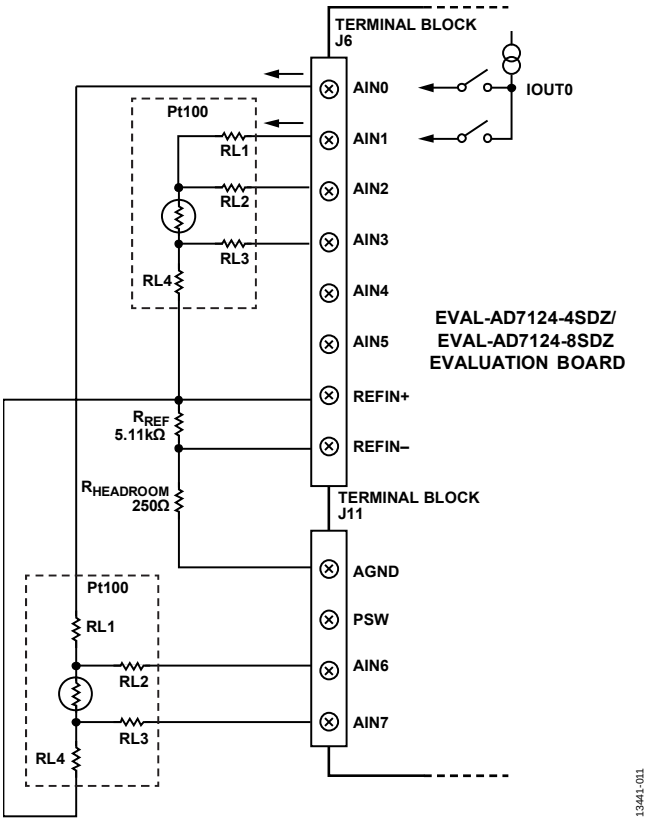

Figure 11. AD7124-4 4-Wire RTD Configuration Using Two 4-Wire RTDs

The performance of the 4-wire RTD configuration shown in Figure 11 was evaluated to ensure that the expected performance was achieved when more than one RTD was connected. For this measurement, the temperature of both 4-wire RTDs were swept from −50°C to +200°C. For each temperature setting, the voltage across each RTD was recorded. Figure 12 shows the error in each. As shown in the results, switching the same current from Channel 0 to Channel 1 has no effect on settling; both RTDs are well within the expected error window for the Class B RTD.

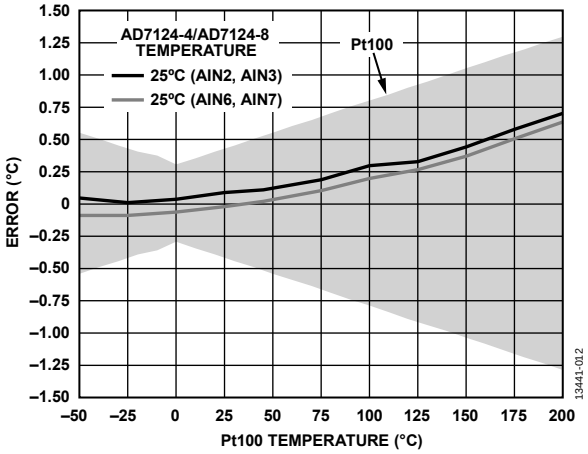

Figure 12. RTD Temperature Error Recorded for Two Different RTD Measurement Configurations

CIRCUIT EVALUATION AND TEST

Equipment Needed

The following equipment is needed for the 4-wire RTD measurement system:

- EVAL–AD7124-4SDZ or EVAL-AD7124-8SDZ evaluation board
- EVAL-SDP-CB1Z System Demonstration Platform (SDP)
- AD7124-4/AD7124-8 EVAL+ Software
- Power supply: 7 V or 9 V wall wart
- Class B Pt100 4-wire RTD
- A PC running Windows® XP (SP2), Windows Vista, or Windows 7 (32-bit or 64-bit)

Software Installation

A complete software user guide for the AD7124-4/AD7124-8 and the SDP board can be found in the EVAL–AD7124-4SDZ/ EVAL-AD7124-8SDZ user guide and the SDP User Guide.

Software is required to interface with the hardware. This software can be downloaded from ftp://ftp.analog.com/pub/evalcd/AD7124. If the setup file does not automatically run, double click **setup.exe** from the file. Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

After the evaluation software installation is complete, connect the EVAL-SDP-CB1Z (via Connector B) to the EVAL-AD7124-4SDZ/ EVAL-AD7124-8SDZ and then connect the EVAL-SDP-CB1Z to the USB port of the PC using the supplied cable. When the evaluation system is detected, proceed through any dialog boxes that appear to complete the installation.

Setup and Test

Figure 13 shows a functional block diagram of the test setup.

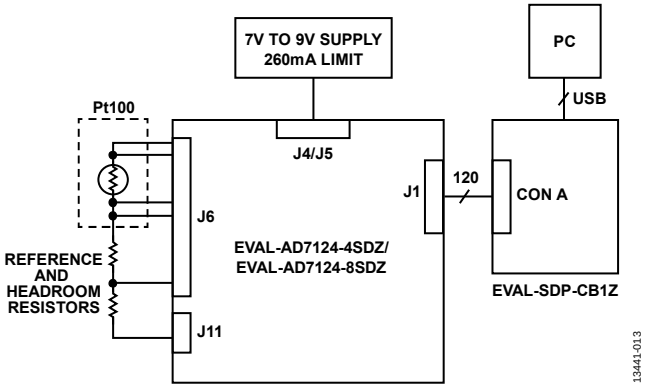

Figure 13. Test Setup Functional Diagram

The EVAL-AD7124-4SDZ /EVAL-AD7124-8SDZ evaluation board is required to test the circuit. In addition, the following sensor and resistors are required to ensure proper operation:

- 4-wire Pt100 RTD, Class B
- 5.11 kΩ precision resistor
- 250 Ω resistor needed for buffer headroom

Configuring the Hardware

To configure the hardware, take the following steps:

1. Set all links on the EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ evaluation board to the default positions, as described in the EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ user guide.
2. Power the board with a 7 V or 9 V power source connected to J5.
3. Connect the RTD, the precision reference resistor, and the resistor for headroom, as shown in Figure 14.

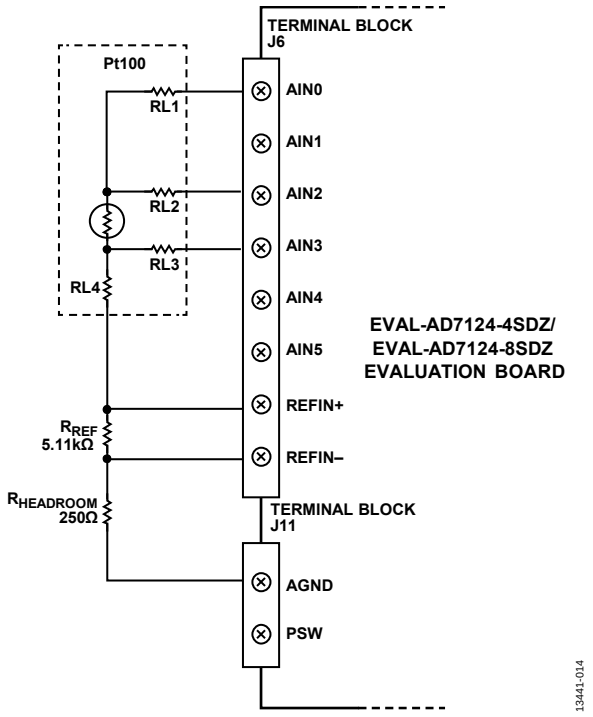

Figure 14. EVAL–AD7124-4SDZ/EVAL-AD7124-8SDZ Evaluation Board Connector for 4-Wire RTD Measurement

Run the AD7124-4/AD7124-8 EVAL+ Software, and the window shown in Figure 15 appears.

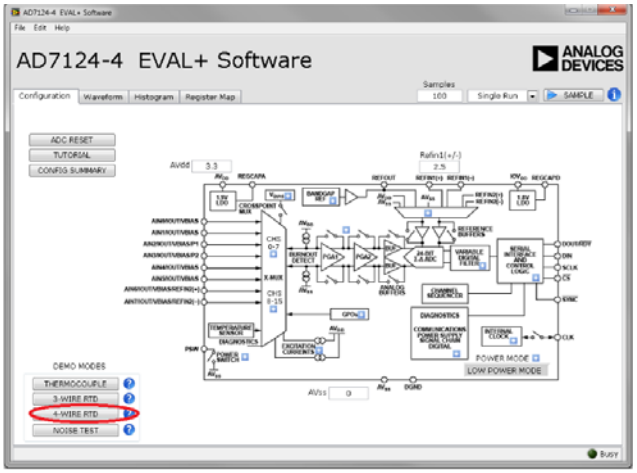

Figure 15. AD7124-4 EVAL+ Software Window

To configure the AD7124-4/AD7124-8 for 4-wire RTD measurements, click the **4-WIRE RTD** demo mode button (see Figure 15). Clicking the **4-WIRE RTD** button configures the ADC software as follows:

- Channel_0
  - AINP_0 = AIN2
  - AINM_0 = AIN3
  - Setup0
  - Enabled = TRUE
- Setup_0
  - PGA_0 = 16
  - AIN_BUFP, AIN_BUFM both = ENABLED
  - BIPOLAR = ENABLED
  - FS_0 = 384
  - FILTER_MODE_0 = SINC4
- ADC_Control
  - MODE = Continuous Conversion
  - POWER_MODE = FULL
- IO_CONTROL_1
  - IOUT0 Channel Enable = AIN1
  - IOUT0 Select = 500 µA

One additional step is required before the AD7124-4/AD7124-8 is configured for 4-wire RTD measurements: an internal full-scale and zero-scale calibration of the AD7124-4/AD7124-8. This calibration can be performed via the **Register Map** tab, as shown in Figure 16.

1. Click the **ADC_Control** register.
2. Select **Low Power** mode.
3. Perform an internal full-scale calibration.
   a. Click the **Mode** bitfield of the ADC control register
   b. In the **Mode** bitfield, select the internal full scale calibration option.
   c. Check the calibration performed by clicking the **Gain0** register from the register tree, and check that the coefficients have changed.
4. Perform an internal zero-scale calibration.
   a. Click the **Mode** bitfield of the ADC control register.
   b. In the **Mode** bitfield, select the internal zero-scale calibration option.
   c. Check the calibrations performed by clicking the **Offset0** register in the register tree, and check that the coefficients have changed.
5. When calibrations are complete, change the power mode to the required mode of operation, and ensure that the ADC is set to continuous conversion mode by selecting **Continuous** from the drop-down box in the **Mode** bit field of the **ADC_Control** register.

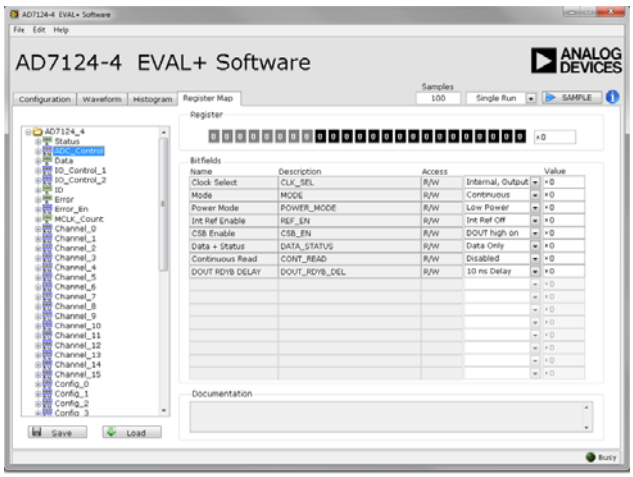

Figure 16. Register Map Internal Full-Scale and Zero-Scale Calibration

The board and device are now configured for 4-wire RTD measurements. Click **SAMPLE** to start gathering samples from the AD7124-4/AD7124-8. The **Waveform** tab and the **Histogram** tab show the data gathered from the AD7124-4/AD7124-8.

LEARN MORE

CN-0381 Design Support Package:
www.analog.com/CN0381-DesignSupport

EVAL-AD7124-4 User Guide (UG-855)

EVAL-AD7124-8 User Guide (UG-856)

SDP User Guide

Kester, Walt. "Temperature Sensors," Chapter 7 in *Sensor Signal Conditioning*. Analog Devices, 1999.

McCarthy, Mary. AN-615 Application Note. *Peak-to-Peak Resolution Versus Effective Resolution*. Analog Devices.

McNamara, Donal. AN-892 Application Note. *Temperature Measurement Theory and Practical Techniques*. Analog Devices.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*. Analog Devices.

MT-101 Tutorial. *Decoupling Techniques*. Analog Devices.

Circuit Note CN-0376. *Channel-to-Channel Isolated Temperature Input (Thermocouple/RTD) for PLC/DCS Applications*. Analog Devices.

Circuit Note CN-0382. *Ultralow Power Industrial Temperature and Pressure, 4 mA to 20 mA/HART Transmitter*. Analog Devices.

Circuit Note CN-0383. *Completely Integrated 3-Wire RTD Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC*. Analog Devices.

Circuit Note CN-0384. *Completely Integrated Thermocouple Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC*. Analog Devices.

Data Sheets and Evaluation Boards

EVAL-AD7124-4SDZ

EVAL-AD7124-8SDZ

System Demonstration Platform (EVAL-SDP-CB1Z)

AD7124-4 Data Sheet

AD7124-8 Data Sheet

ADP1720 Data Sheet

REVISION HISTORY

7/15—Revision 0: Initial Version

Circuits from the Lab Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0383.

Devices Connected/Referenced	
AD7124-4/ AD7124-8	4-Channel/8-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADCs with PGA and Reference
ADP1720	50 mA, High Voltage, Micropower Linear Regulator

Completely Integrated 3-Wire RTD Measurement System Using a Low Power, Precision, 24-Bit Sigma-Delta ADC

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

AD7124-4 Evaluation Board (EVAL-AD7124-4SDZ) or
AD7124-8 Evaluation Board (EVAL-AD7124-8SDZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is an integrated 3-wire resistance temperature detector (RTD) system based on the AD7124-4/ AD7124-8 low power, low noise, 24-bit Σ-Δ analog-to-digital converter (ADC) optimized for high precision measurement applications. With a two-point calibration and linearization, the overall 3-wire system accuracy is better than ±1°C over a temperature range of −50°C to +200°C. Typical noise free code resolution of the system is 17.9 bits for full power mode, sinc^4 filter selected, at an output data rate of 50 SPS, and 16.8 bits for low power mode, post filter selected, at an output data rate of 25 SPS.

The AD7124-4 can be configured for 4 differential or 7 pseudo differential input channels, while the AD7124-8 can be configured for 8 differential or 15 pseudo differential channels. The on-chip programmable gain array (PGA) ensures that signals of small amplitude can be interfaced directly to the ADC.

The AD7124-4/AD7124-8 establishes the highest degree of signal chain integration, which includes programmable low drift excitation current sources. Therefore, the design of an RTD system is greatly simplified because most of the required RTD measurement system building blocks are included on-chip.

The AD7124-4/AD7124-8 gives the user the flexibility to employ one of three integrated power modes, where the current consumption, range of output data rates, and rms noise are tailored with the power mode selected. The current consumed by the AD7124-4/AD7124-8 is only 255 µA in low power mode and 930 µA in full power mode. The power options make the device suitable for non-power critical applications, such as input/output modules, and also for low power applications, such as loop-powered smart transmitters where the complete transmitter must consume less than 4 mA.

The device also has a power down option. In power-down mode, the complete ADC along with its auxiliary functions are powered down so that the device consumes 1 µA typical. The AD7124-4/ AD7124-8 also has extensive diagnostic functionality integrated as part of its comprehensive feature set.

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Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

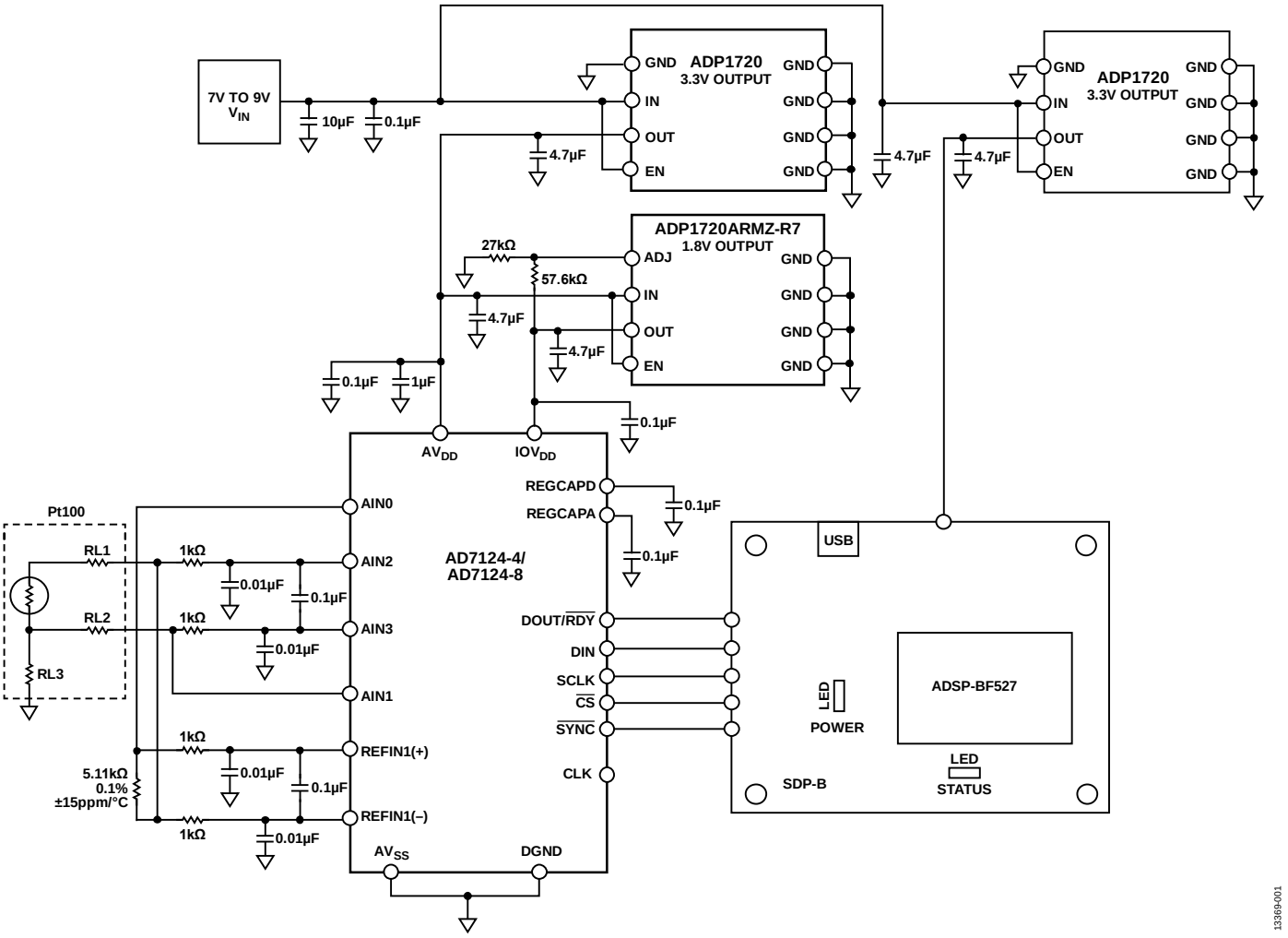

Figure 1. 3-Wire RTD Measurement Configuration

CIRCUIT DESCRIPTION

RTD Temperature Measurement Introduction

RTDs are frequently used sensors for temperature measurements in industrial applications. An RTD is made from a pure metal (examples include platinum, nickel, or copper), which has a predictable change in resistance as the temperature changes. The most widely used RTDs are platinum Pt100 and Pt1000. RTDs are capable of high accuracy and good stability when compared with other types of temperature sensors. The resistance of long wire lengths can be compensated for with a 3-wire connection.

To accurately measure the resistance, a voltage is generated across the RTD by a constant current source. The AD7124-4/AD7124-8 offers two such excitation current sources that are register programmable from 50 µA to 1 mA. Errors in the current source can be easily cancelled by referring the measurement to the voltage across a precision reference resistor that is driven with the same current source, thereby resulting in a ratiometric measurement result.

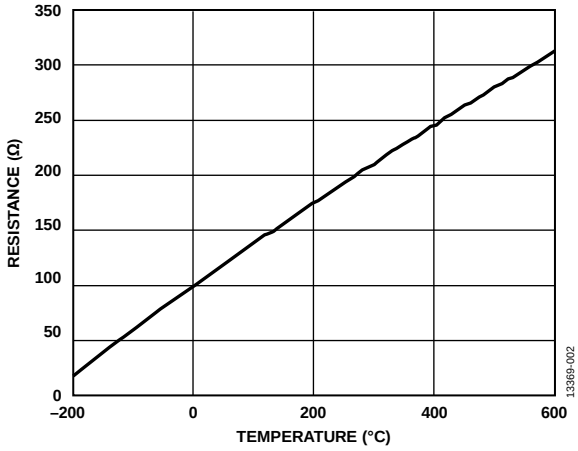

Figure 2. RTD Resistance vs. Temperature

For the circuit in Figure 1, a Class B Pt100 RTD sensor was used. Pt100 RTDs measure temperature from −200°C to +600°C. The resistance of a Class B RTD is typically 100 Ω at 0°C and has a typical temperature coefficient of ~0.385 Ω/°C (see Figure 2). Using this information, the voltage generated across the Pt100 RTD can easily be calculated based on the current source selected.

How the Circuit Works

The AD7124-4/AD7124-8 provides an integrated solution for RTD measurement. It can achieve high resolution, low non-linearity and low noise performance as well as very high 50 Hz and 60 Hz rejection. The AD7124-4/AD7124-8 consists of an on-chip, low noise PGA that amplifies the small signal from the RTD with a gain programmable from 1 to 128, thus allowing direct interface with the sensor. The gain stage has high input impedance and limits the input leakage current to 3.3 nA typical for full power mode and 1 nA typical for low power mode. The following section explain the different elements that make up the 3-wire RTD temperature measurement system.

Power Supplies

The AD7124-4/AD7124-8 has separate analog and digital power supplies. The digital power supply, IOV_{DD}, is independent of the analog power supply and can be from 1.65 V to 3.6 V referenced to DGND. The analog power supply, AV_{DD}, is referred to AV_{SS} and has a range of 2.7 V to 3.6 V for low and mid power modes, and 2.9 V to 3.6 V for full power mode. The circuit shown in Figure 1 operates from a single supply; therefore, AV_{SS} and DGND are connected together, and only one ground plane is used. The AV_{DD} and IOV_{DD} voltage are generated separately using ADP1720 voltage regulators. The AV_{DD} voltage is set to 3.3 V and the IOV_{DD} voltage is set to 1.8 V using the ADP1720 regulators. Using separate regulators ensures the lowest noise.

Serial Peripheral Interface (SPI)

SPI communications to the AD7124-4/AD7124-8 is handled by the Blackfin® ADSP-BF527 on the EVAL-SDP-CB1Z, as shown in Figure 1. To access the registers of the AD7124-4/AD7124-8, use the AD7124-4/AD7124-8 EVAL+ Software. Figure 3 shows the main window of this software. Clicking **3-WIRE RTD** configures the software for the 3-wire RTD measurement.

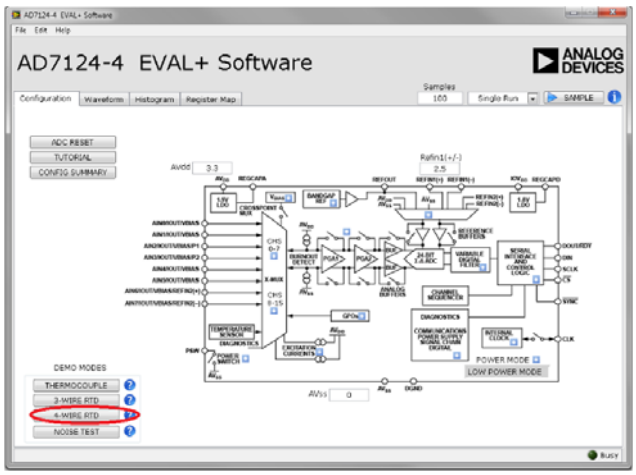

Figure 3. AD7124-4/AD7124-8 EVAL+ Software Configuration Screen

The AD7124-4/AD7124-8 has diagnostic functions on-chip that can be used to detect faults in the SPI communication. These diagnostics include checks on the SPI read and write operations, ensuring that only valid registers are accessed. An SCLK counter ensures that the correct number of SCLK pulses are used, while the CRC functionality checks for changes in bit values during transmission. When any of these SPI communication diagnostic functions are enabled and an associated error occurs, the corresponding flag is set in the error register. All enabled flags are OR'ed together and control the ERR flag in the status register. This functionality is particularly useful if the status bits are appended to the ADC conversions.

Analog Inputs and Reference

The AD7124-4 can be configured for 4 differential or 7 pseudo differential channels, while the AD7124-8 can be configured for 8 differential or 15 pseudo differential channels.

The AD7124-4/AD7124-8 has on-chip diagnostics that can be used to check that the voltage level on the analog pins are within the specified operating range. The positive (AINP) and negative (AINM) analog inputs can be separately checked for overvoltages and undervoltages, as well as ADC saturation. An overvoltage is flagged when the voltage on the analog input exceeds AV_{DD}, while an undervoltage is flagged when the voltage on the analog input goes below AV_{SS}.

For the circuit shown in Figure 1, four analog pins are used to implement the 3-wire measurement: AIN0, AIN1, AIN2, and AIN3. AIN2 and AIN3 are configured as a fully differential input channel and are used for sensing the voltage across the Pt100. The excitation current source used to excite the RTD is generated from AV_{DD} and is directed to AIN0. An identical current is directed to AIN1 and flows through the RL2 lead resistance, thereby generating a voltage that cancels the voltage dropped across the RL1 lead resistance. The analog pins and their configuration are shown in greater detail in Figure 4.

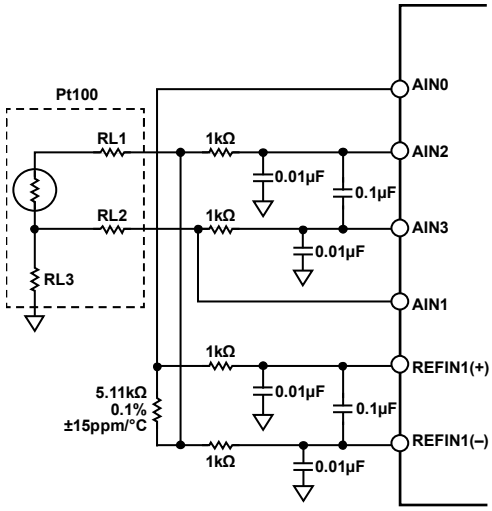

Figure 4. Analog Inputs for 3-Wire RTD Measurement

With the PGA enabled, the analog input buffers are automatically enabled. The PGA allows voltages on the input pins to be as low as AV_{SS}; therefore, headroom resistors are not required for the analog input pins. The reference buffers are also enabled. These buffers require headroom. Because the reference resistor is on the high side, the headroom requirements for the reference resistor are met; therefore, additional headroom resistors are not required.

For the circuit shown in Figure 1, the reference input used is REFIN1(±). The current through the Pt100 also flows through the precision reference resistor that generates the reference voltage. The voltage generated across this precision reference resistor is ratiometric to the voltage across the Pt100; therefore, any errors because of variations in the excitation current are removed.

Digital and Analog Filtering

Differential (~800 Hz cutoff) and common-mode (~16 kHz cutoff) filters are implemented at the analog inputs as well as at the reference inputs. This filtering is required to reject any interference at the modulator frequency and also any multiples of this frequency.

The AD7124-4/AD7124-8 offers a great deal of on-chip digital filtering flexibility. Several filter options are available; the option selected has an effect on the output data rate, settling time, as well as 50 Hz and 60 Hz rejection. For this circuit note, the sinc^4 filter and the post filter are implemented. The sinc^4 filter is used because it has excellent noise performance across the range of output data rates, as well as excellent 50 Hz and 60 Hz rejection. The post filter is used to provide simultaneous 50 Hz and 60 Hz rejection with a 40 ms settling time.

Calibration

The AD7124-4/AD7124-8 provides different calibration modes that can be used to eliminate offset and gain errors. For this circuit note, internal zero-scale calibration as well as internal full-scale calibration were used. Note that these calibrations remove only the ADC gain and offset errors, not gain and offset errors created by the external circuitry.

3-Wire RTD Configuration

The circuit shown in Figure 1 is designed for precision 3-wire RTD measurement using the AD7124-4/AD7124-8. For the 3-wire RTD measurement, two precision excitation current sources are required that provide an easy way to cancel the lead resistance errors produced by RL1 and RL2. Note that the RL3 lead resistance does not affect the measurement accuracy. For the 3-wire RTD configuration shown in Figure 1, the reference resistor is placed on the high side of the RTD. For this setup, one excitation current flows through both the reference resistor and the RTD; the second current flows through lead-resistance RL2 and develops a voltage that cancels the voltage dropped across RL1. Because only one excitation current generates the reference voltage to REFIN1±, and also generates the voltage across the RTD, the current source accuracy, mismatch, and mismatch drift has a minimal effect on the ADC transfer function.

A low level voltage is generated across the Pt100 RTD by the excitation current. This low level voltage can then be amplified by the on-board PGA of the AD7124-4/AD7124-8, and is then converted to a precision digital representation using the 24-bit Σ-Δ ADC. For this 3-wire RTD configuration, both excitation currents are programmed to 500 µA. For a maximum RTD temperature of 600°C, the voltage generated across the RTD using the 500 µA excitation current is approximately 156.85 mV.

To ensure that the maximum range of the AD7124-4/AD7124-8 is used, the PGA gain is programmed to 16, which amplifies the maximum RTD sensor output voltage to 2.5096 V. To ensure a true ratiometric configuration for this 3-wire circuit, the reference voltage to the ADC is generated using an external precision resistor using the same excitation current as that used for the Pt100. Using this configuration means that any deviation in the value of the excitation current is seen across the Pt100 as well as the reference resistor, and therefore does not alter the accuracy of the system.

Using the excitation current of 500 µA and the amplified voltage of the ADC, the reference resistor value is

$$V_{RTD\,MAX}/I_{EXC} = 2.51\text{ V}/500\text{ µA} = 5020\ \Omega$$

Therefore, a 5.11 kΩ resistor is chosen, which gives a reference voltage of

$$V_{REF} = R_{REF} \times I_{EXC} = 5.11\text{ k}\Omega \times 500\text{ µA} = 2.555\text{ V}$$

The output compliance of the excitation current source must also be considered when making 3-wire RTD measurements using the AD7124-4/AD7124-8. The output compliance is dependent on the excitation current selected. For this circuit, 500 µA is selected, which has an output compliance voltage of AV_{DD} − 0.37 V. The AV_{DD} supply voltage for this circuit is 3.3 V, which means that the output compliance level for the excitation current source must be less than 2.93 V. From the previous calculations, this specification is met because the maximum voltage on the AIN0 pin is the voltage across the precision reference resistor plus the voltage across the RTD:

$$V_{REF} + V_{RTD} = 2.555\text{ V} + 156.85\text{ mV} = 2.71185\text{ V}$$

The AD7124-4/AD7124-8 configuration for the 3-wire RTD measurement is as follows:

- Differential input: AINP = AIN2, AINM = AIN3
- Excitation current: IOUT0 = AIN0 = 500 µA
- Excitation current: IOUT1 = AIN1 = 500 µA
- Gain = 16
- 5.11 kΩ precision reference resistor
- Digital filtering (sinc^4 and post filter)

The general expression to calculate the RTD resistance (R), where the ADC is operating in bipolar mode, is given by

$$R_{RTD} = \frac{(CODE - 2^{N-1}) \times R_{REF}}{G \times 2^{N-1}} \quad (1)$$

where:
CODE is the ADC code.
N is the resolution of the ADC (24, in this case).
R_{REF} is the reference resistor.
G is the selected gain.

From the specification of the Class B RTD, the resistance changes by approximately 0.385 Ω/°C. This relationship can be used as a quick method to get an approximate temperature of the RTD. This method has inaccuracies due to the temperature coefficient of

the RTD changing slightly over the temperature range; however, it can be a useful method to quickly check the temperature.

To calculate the approximate temperature, use Equation 2, where the resistance of the RTD is 100 Ω at 0°C.

$$Temperature\ (°C) = \frac{R_{RTD} - 100}{0.385} \quad (2)$$

The RTD transfer function known as the Callender-Van Dusen equation is made up of two distinct polynomial equations. Equation 3 is used for temperatures greater than 0°C, and Equation 4 for temperatures less than 0°C.

The equation for temperature t ≤ 0°C is

$$R_{RTD}(t) = R_0[1 + At + Bt^2 + C(t - 100°C)t^3] \quad (3)$$

The equation for temperature t ≥ 0°C is

$$R_{RTD}(t) = R_0(1 + At + Bt^2) \quad (4)$$

where:
t is the RTD temperature (°C).
$R_{RTD}(t)$ is the RTD resistance at temperature (t).
R_0 is the RTD resistance at 0°C (in this case, R_0 = 100 Ω).
$A = 3.9083 \times 10^{-3}$.
$B = -5.775 \times 10^{-7}$.
$C = -4.23225 \times 10^{-12}$.

There are many different ways to determine the temperature as a function of the RTD resistance given the transfer function in Equation 3 and Equation 4. For this circuit note, the direct mathematical method is chosen because of its accuracy. Using Equation 3, the temperature can be calculated as

$$T_{RTD}\ (°C) = \frac{-A + \sqrt{A^2 - 4B\left(1 - \frac{r}{R_0}\right)}}{2B} \quad (5)$$

where r is the RTD resistance, and the other variables are as defined previously.

This method works well for temperatures greater than or equal to 0°C. To calculate the RTD temperature for temperatures below 0°C, a best fit polynomial expression is required. The polynomial used in this note is a fifth-order polynomial, shown in Equation 6.

$$T_{RTD}\ (°C) = -242.02 + 2.2228 \times r + (2.5859 \times 10^{-3})r^2 - (48260 \times 10^{-6})r^3 - (2.8183 \times 10^{-3})r^4 + (1.5243 \times 10^{-10})r^5 \quad (6)$$

As an example, the code read back from the AD7124-4/AD7124-8 for the temperature set to 25°C is 11270065. Converting this code to a resistance using Equation 1 gives

$$R_{RTD} = \frac{(11270065 - 2^{23}) \times R_{REF}}{G \times 2^{23}} = 109.704\ \Omega$$

Linearization using Equation 5 gives a temperature of 24.921°C.

As a second example, the code read back from the AD7124-4/AD7124-8 for the temperature set to −25°C is 10757779.

Converting this code to a resistance gives

$$R_{RTD} = \frac{(10757779 - 2^{23}) \times R_{REF}}{G \times 2^{23}} = 90.200\ \Omega$$

Linearization using Equation 6 gives a temperature of −24.982°C.

3-Wire RTD Measurements and Results

For the circuit shown in Figure 1, data was gathered for different digital filter and power mode configurations of the AD7124-4/AD7124-8, namely the sinc⁴ filter operating in full power mode and the post filter operating in low power mode.

Choosing the configuration for sinc⁴ filter, full power mode for an output data rate of 50 SPS allows the user to operate the AD7124-4/AD7124-8 for best performance in relation to speed and noise. Figure 5 shows the noise distribution when a 3-wire RTD is connected as shown in Figure 1 at ambient temperature. The corresponding rms noise is typically 199.37 nV rms equating to approximately 17.9 noise free bits. The noise performance of the AD7124-4/AD7124-8 for inputs shorted when the same filter, gain, and output data rate are selected is typically 100 nV rms or 18.7 noise free bits. The increase in the noise comes directly from the RTD connected across the input channel (AIN2, AIN3).

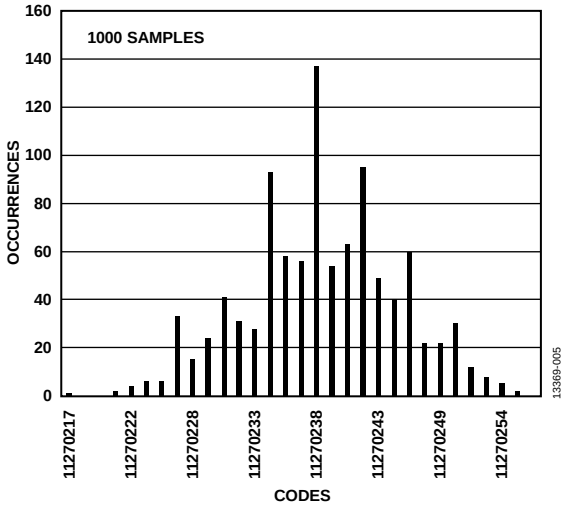

Figure 5. Histogram of Codes for RTD at Ambient, Sinc⁴ Filter, Full Power Mode, 50 SPS

For the 3-wire RTD configuration where the sinc⁴ filter and full power mode were selected, the temperature of the RTD was swept from −50°C to +200°C. For each temperature, the corresponding voltage across the RTD was measured using the AD7124-4/AD7124-8 as outlined previously. This voltage was then converted to a resistance, linearized, and converted to a temperature as outlined in the 3-Wire RTD Configuration section. Figure 6 shows the resulting error between the set temperature and the measured system temperature of the RTD after linearization. For each RTD temperature setting, the AD7124-4/AD7124-8 is kept at 25°C. As shown in Figure 6, the error of the RTD temperature measured is well within the error window of the Pt100 Class B RTD. Figure 6 also shows the deviation of the RTD error across different AD7124-4/AD7124-8

temperature settings. For each AD7124-4/AD7124-8 temperature setting, an internal zero-scale and full-scale calibration is carried out. As shown in Figure 6, the error of the RTD is well within the expected error of the Class B RTD for all temperature settings of the AD7124-4/AD7124-8.

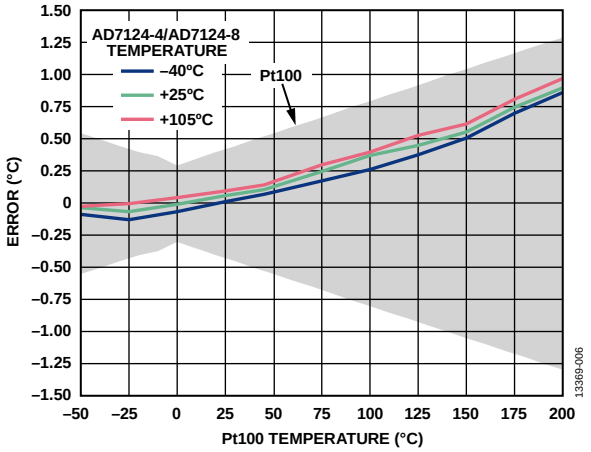

Figure 6. Temperature Accuracy Measurement, Sinc⁴ Filter, Full Power Mode, 50 SPS

Figure 7 shows the error in measured RTD temperature for a one time, internal zero-scale and full-scale calibrations carried out at 25°C. The plot shows that carrying out a one time calibration at 25°C or calibrating at each individual temperature of the AD7124-4/AD7124-8 gives similar performances.

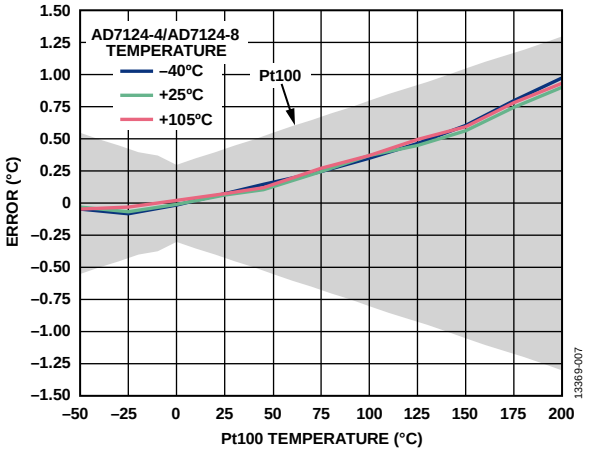

Figure 7. Temperature Accuracy Measurement, Sinc⁴ Filter, Full Power Mode, 50 SPS, One Time 25°C Calibration Only

The second AD7124-4/AD7124-8 configuration tested was the low power mode, where the post filter and 25 SPS output data rate were selected. The 25 SPS filter gives simultaneous 50 Hz and 60 Hz rejection and allows the user to trade off settling time with power supply rejection. Figure 8 shows the resulting noise distribution when a 3-wire RTD is connected as shown in Figure 1 at ambient temperature. The corresponding rms noise is typically 774 nV rms equating to approximately 16.8 noise free bits. The noise performance of the AD7124-4/AD7124-8 for inputs shorted with the same filter, gain, power mode, and output data rate is typically 360 nV rms or 17.3 noise free bits. The increase in the noise between the two measurements comes directly from the RTD connection across the input channel (AIN2, AIN3).

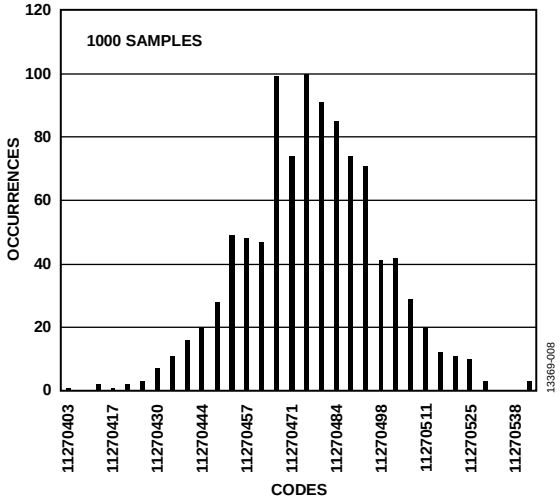

Figure 8. Histogram of Codes for RTD at Ambient, Post Filter, Low Power Mode, 25 SPS

For this AD7124-4/AD7124-8 configuration where the post filter and low power mode were selected, the temperature of the RTD was swept from −50°C to +200°C. For each of the set RTD temperatures, the corresponding voltage across the RTD was measured using the AD7124-4/AD7124-8 as outlined previously. This voltage was then converted to a resistance, which was then linearized and converted to a temperature as outlined in the 3-Wire RTD Configuration section. Figure 9 shows the resulting error between the set and measured temperatures of the RTD after linearization. For each RTD temperature setting, the AD7124-4/AD7124-8 is kept at 25°C. As shown in Figure 9, the error of the RTD temperature measured is well within the error window of the Pt100 Class B RTD. Figure 9 also shows the deviation of the RTD error across different AD7124-4/AD7124-8 temperature settings. For each AD7124-4/AD7124-8 temperature setting, an internal zero-scale and full-scale calibration is carried out. Figure 9 shows that the error of the RTD is well within the expected error of the Class B RTD for all temperature settings of the AD7124-4/AD7124-8.

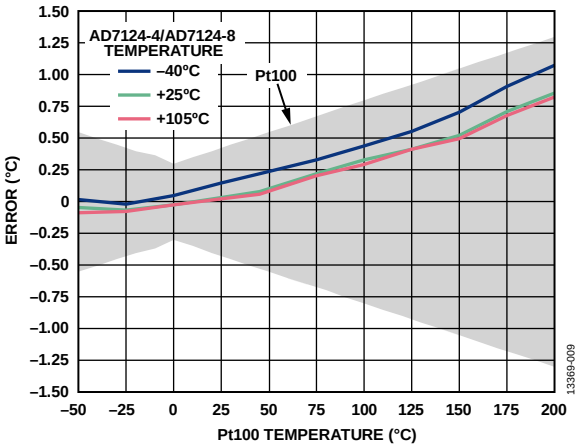

Figure 9. Temperature Accuracy Measurement, Post Filter, Low Power Mode, 25 SPS

Figure 10 shows the error in measured RTD temperature for a one time, internal zero-scale and full-scale calibration carried out at 25°C. The plot shows that carrying out a one time calibration at 25°C or calibrating at each individual temperature of the AD7124-4/AD7124-8 gives similar performances.

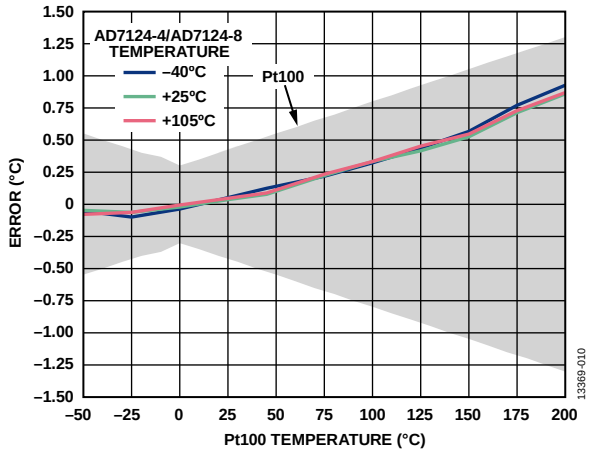

Figure 10. Temperature Accuracy Measurement, Post Filter, Low Power Mode, 25 SPS, 25°C One Time Calibration Only

COMMON VARIATIONS

Current Source Mismatch and Mismatch Drift

In the Figure 1 circuit, the precision reference resistor was placed on the high side. The high-side configuration works well for systems using a single RTD. When multiple RTDs are used, it is better to place the precision resistor on the low side because only a single reference resistor is required. With the reference resistor on the low side, better excitation current matching is required. Two different techniques can be used to minimize the errors due to mismatches in the currents:

- Chopping the excitation currents
- Calibration by measuring the excitation currents

Chopping the Excitation Currents

The crosspoint multiplexer on the AD7124-4/AD7124-8 allows easy implementation of the chopping configuration. Figure 11 shows the 3-wire RTD configuration with the precision 5.11 kΩ reference resistor connected to the low side of the Pt100 RTD. For this configuration, the current source used as well as the gain must be reconsidered. Both IOUT0 and IOUT1 are set to 250 µA. Selecting this current ensures that the circuit complies with the output compliance of the current sources as well as the reference voltage generated across the precision resistor. To ensure that the full range of the ADC is used, the gain of the PGA was set to 32. A resistor is required on the low side of the reference resistor because the reference buffers are enabled and require headroom (100 mV).

To chop the currents, a measurement of the RTD voltage is taken when IOUT0 is connected to AIN0, and IOUT1 is connected to AIN1, as shown in Figure 11. A second measurement of the voltage across the RTD is then taken when the currents are swapped, that is, when IOUT1 is connected to AIN0, and IOUT1 is connected to AIN1. The average of these two voltage measurements is then used in the overall calculation of the RTD resistance, and subsequently the temperature is calculated using Equation 1 through Equation 6. The chopping method greatly reduces any effects of excitation current mismatch and mismatch drift. However, there is an impact on the throughput rate since two measurements are required.

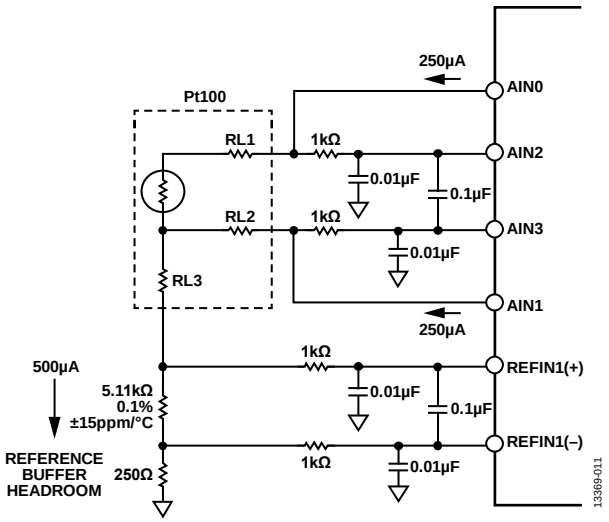

Figure 11. AD7124-4/AD7124-8 Configuration for 3-Wire RTD Measurement Using the Current Chopping Measurement Technique

Measurement data using the excitation current chopping method was gathered, and the corresponding Pt100 temperature error recorded as shown in Figure 12. For all RTD temperatures measured, the temperature error is within the error band of the Pt100 RTD for different ambient temperatures of the AD7124-4/AD7124-8. These results show that chopping the excitation current gives results that are comparable to the data gathered with the high-side precision reference resistor configuration.

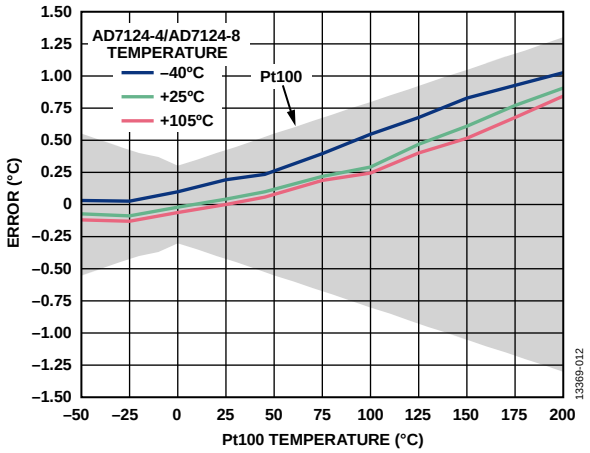

Figure 12. Temperature Accuracy Measurement for Chopping Configuration, Sinc⁴ Filter, Full Power Mode, Calibration at Each Temperature

Calibration by Measuring the Excitation Currents

The configuration for calibrating the 3-wire system by measuring the excitation currents is shown in Figure 13. For this configuration, the precision reference resistor is connected

to the low side of the RTD. This configuration is similar to that used for chopping the currents, where both the currents are set to 250 µA, and the PGA gain is set to 32. However, the main difference is that an additional differential input channel is required. The additional input channel enables the measurement of the two excitation currents. The measurement is implemented by measuring the voltage drop across the precision reference resistor with respect to the internal reference when each of the excitation currents is individually enabled. The measured voltage is then converted to a current based on the value of the precision reference resistor value, which is subsequently used to calculate the ratio of the currents, and then used to calibrate the mismatch.

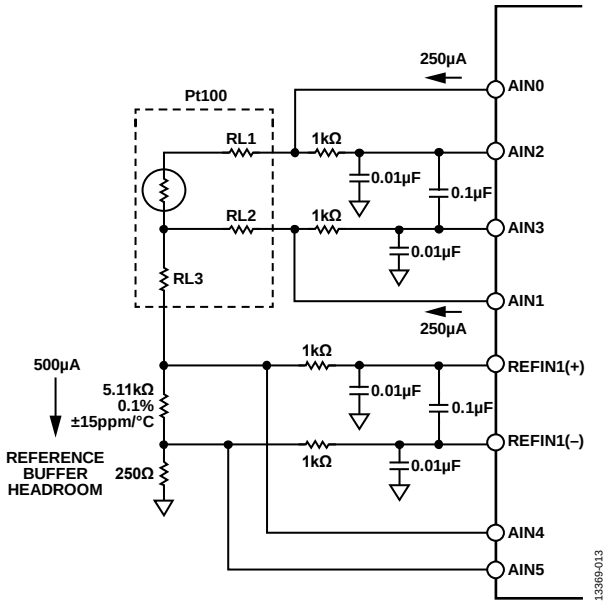

Figure 13. AD7124-4/AD7124-8 Configuration for 3-Wire RTD Measurement Calibration by Measuring the Excitation Currents

Figure 14 shows the calibrated temperature error in the RTD measurements. The results show that the RTD error is within the expected error band of the RTD, where the error in measurement is close to the error profile of the RTD itself. To ensure accurate results, calibration of the currents must take place at regular intervals over time.

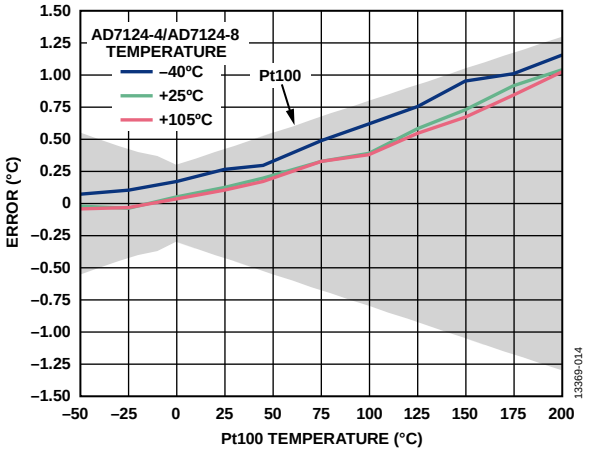

Figure 14. Temperature Accuracy Measurement for Excitation Current Calibration, Sinc⁴ Filter, Full Power Mode, Calibration at Each Temperature

Lead Resistance Considerations

For the 3-wire RTD measurement, the accuracy of the lead resistance compensation depends on the resistance of each of the leads being equal (specifically, RL1 = RL2). The voltage dropped across RL3 does not affect the voltage measured across the RTD element; therefore, RL3 does not introduce error in the measurement for the circuits described in this circuit note.

The nominal resistance of 24 AWG copper wire is 0.026 Ω/foot. A 50 foot length has a 1.3 Ω lead resistance. A 10% error in matching produces a 0.13 Ω error in the RTD measurement, assuming perfectly matched compensation and excitation currents. The RTD temperature coefficient is approximately 0.385 Ω/°C; therefore, the 0.13 Ω lead resistance mismatch measurement error translates into approximately (0.13 Ω) ÷ (0.385 Ω/°C) = 0.337°C error due to lead resistance mismatch. Therefore, for accurate 3-wire measurements, the matching characteristics of the connecting cables must be known precisely.

Assuming perfect lead resistance matching, mismatches in the excitation currents (IOUT0 and IOUT1) produce an error that is proportional to the total lead resistance. For instance, a 0.5% mismatch in the excitation currents (typical specification for the AD7124-4/AD7124-8) produces a corresponding 0.5% error in the RTD resistance measurement. The nominal Pt100 RTD resistance temperature coefficient is 0.385 Ω/°C, which is equivalent to a temperature change of 2.6°C/Ω. A 0.5% error in the resistance measurement gives an RTD measurement error of 0.005 × 2.6°C/Ω = 0.013°C/Ω. For a lead resistance of 10 Ω (~400 feet of 24 AWG copper wire), the error due to the mismatch in currents is only 0.13°C.

The previous discussion illustrates that, in most practical applications, the mismatch in the lead resistances creates much more error than the 0.5% mismatch in excitation currents. As previously mentioned, the mismatch error in the excitation currents can be minimized by using either the chopping mode or by measuring the individual excitation currents.

CIRCUIT EVALUATION AND TEST

Equipment Needed

The following equipment is required for the 3-wire RTD measurement system:

- The EVAL–AD7124-4SDZ or EVAL-AD7124-8SDZ evaluation board
- The EVAL-SDP-CB1Z System Demonstration Platform (SDP)
- AD7124-4/AD7124-8 EVAL+ Software
- Power supply: 7 V or 9 V wall wart
- Class B Pt100 3-wire RTD
- A PC running Windows® XP (SP2), Windows Vista, or Windows 7 (32-bit or 64-bit)

Software Installation

A complete software user guide for the AD7124-4/AD7124-8 and the SDP board can be found in the EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ user guide and the SDP User Guide.

Software is required to interface with the hardware. This software can be downloaded from ftp://ftp.analog.com/pub/evalcd/AD7124. If the setup file does not run automatically, double-click **setup.exe** from the file. Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

After the evaluation software installation is complete, connect the SDP board (via Connector A) to the EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ and then connect the SDP board to the USB port of the PC using the supplied cable. When the evaluation system is detected, proceed through any dialog boxes that appear to complete the installation.

Setup and Test

Figure 15 shows a functional block diagram of the test setup for the 3-wire RTD configuration.

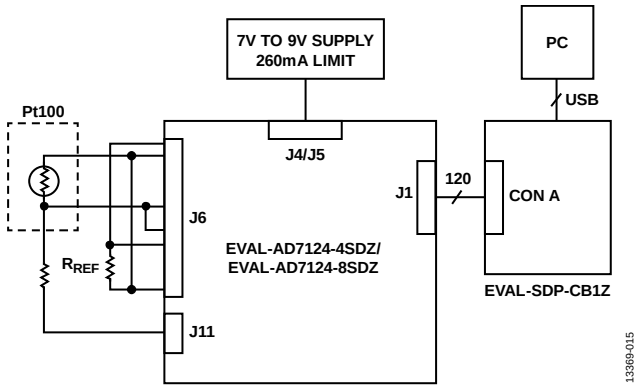

Figure 15. Test Setup Functional Diagram

The EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ evaluation board is required to test the circuit. In addition, the following sensor and resistors are required for proper operation:

- 3-wire Pt100 RTD, Class B
- 5.11 kΩ precision resistor
- 250 Ω resistor for buffer headroom (not needed for this configuration, but included for completeness because it may be required if a Pt1000 RTD is used with a gain of 1)

To configure the hardware, take the following steps:

- Set all links on the EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ to the default board positions as outlined in the EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ user guide.
- Power the board with a 7 V or 9 V power source connected to J5.
- Connect the RTD, precision reference resistor, and resistor for headroom as shown in Figure 16.

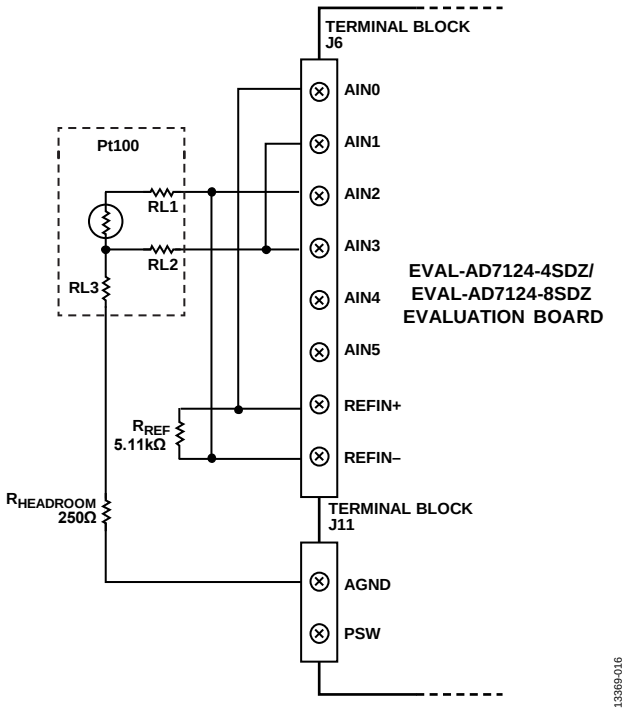

Figure 16. EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ Evaluation Board Connector for 3-Wire RTD Measurement

Run the AD7124-4/AD7124-8 EVAL+ Software. Figure 17 shows a screenshot of the main window of the software.

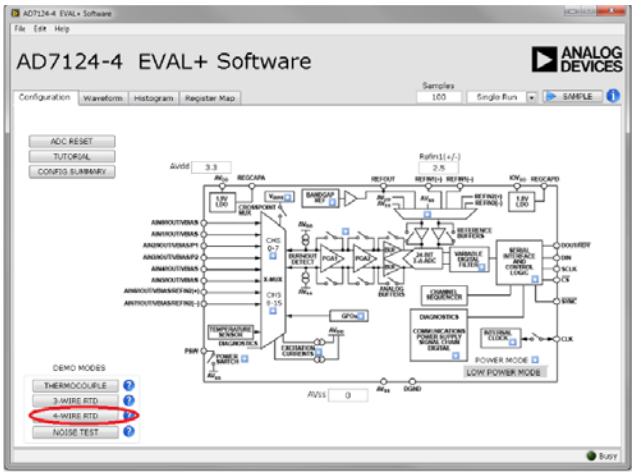

Figure 17. AD7124-4/AD7124-8 EVAL+ Software Main Window

To configure the AD7124-4/AD7124-8 for 3-wire RTD measurements, click the **3-WIRE RTD** demo mode button (see Figure 17). Clicking this button configures the ADC software for optimized performance. Some of the register settings are as follows:

1. Channel_0
   a. AINP_0 = AIN2
   b. AINM_0 = AIN3
   c. Setup0
   d. Enabled = TRUE
2. Setup_0
   a. PGA_0 = 16
   b. AIN_BUFP, AIN_BUFM both = ENABLED
   c. BIPOLAR = ENABLED
   d. FS_0 = 384
   e. FILTER_MODE_0 = SINC4
3. ADC_Control
   a. MODE = Continuous Conversion
   b. POWER_MODE = FULL
4. IO_CONTROL_1
   a. IOUT0 Channel Enable = AIN0
   b. IOUT0 Select = 500 µA
   c. IOUT1 Channel Enable = AIN1
   d. IOUT1 Select = 500 µA

One additional step is required before the AD7124-4/AD7124-8 is configured for 3-wire RTD measurements: an internal full-scale and zero-scale calibration of the AD7124-4/AD7124-8. This calibration can be performed via the **Register Map** tab, as shown in Figure 18.

1. From the register tree, select the **ADC_Control** register.
2. Select **Low Power** mode.
3. Perform an internal full-scale calibration.
   a. Click the **Mode** bitfield of the ADC control register.
   b. In the **Mode** bitfield, select the internal full-scale calibration option.
   c. Check that the calibration performed by selecting the **Gain0** register from the register tree, and check that the coefficients have changed.
4. Perform an internal zero-scale calibration.
   a. Click the **Mode** bitfield of the ADC control register.
   b. In the **Mode** bitfield, select the internal zero-scale calibration option.
   c. Check that the calibration performed by selecting the **Offset0** register from the register tree, and check that the coefficients have changed.
5. When calibrations are complete, change the power mode to the required mode of operation, and ensure that the ADC is set to continuous conversion mode by selecting **Continuous** from the drop-down box in the **Mode** bitfield of the **ADC_Control** register.

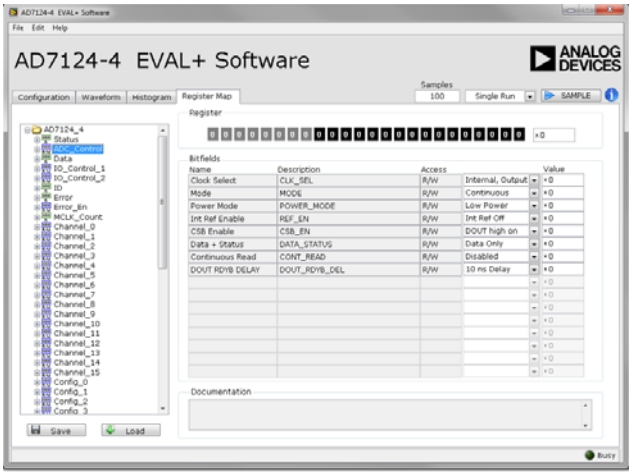

Figure 18. Register Map Internal Full-Scale and Zero-Scale Calibration

The board and device are now configured for 3-wire RTD measurements. Click **SAMPLE** to start gathering samples from the AD7124-4/AD7124-8. The **Waveform** tab and the **Histogram** tab show the data gathered from the AD7124-4/AD7124-8.

LEARN MORE

CN-0383 Design Support Package: www.analog.com/CN0383-DesignSupport

SDP User Guide

EVAL-AD7124-4 User Guide (UG-855)

EVAL-AD7124-8 User Guide (UG-856)

AN-892 Application Note. *Temperature Measurement Theory and Practical Techniques*. Analog Devices.

Kester, Walt. "Temperature Sensors," Chapter 7 in *Sensor Signal Conditioning*. Analog Devices, 1999.

McCarthy, Mary. AN-615 Application Note. *Peak-to-Peak Resolution Versus Effective Resolution*. Analog Devices.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*. Analog Devices.

MT-101 Tutorial. *Decoupling Techniques*. Analog Devices.

Circuit Note CN-0376. *Channel-to-Channel Isolated Temperature Input (Thermocouple/RTD) for PLC/DCS Applications*. Analog Devices.

Circuit Note CN-0381. *Completely Integrated 4-Wire RTD Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC*. Analog Devices.

Circuit Note CN-0382. *Ultralow Power Industrial Temperature and Pressure 4 mA to 20mA/HART Transmitter*. Analog Devices.

Circuit Note CN-0384. *Completely Integrated Thermocouple Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC*. Analog Devices.

Data Sheets and Evaluation Boards

EVAL-AD7124-4SDZ

EVAL-AD7124-8SDZ

System Demonstration Platform (EVAL-SDP-CB1Z)

AD7124-4 Data Sheet

AD7124-8 Data Sheet

ADP1720 Data Sheet

REVISION HISTORY

7/15—Revision 0: Initial Version

Circuits from the Lab Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0384.

Devices Connected/Referenced	
AD7124-4/ AD7124-8	4-Channel/8-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADCs with PGA and Reference
ADP1720	50 mA, High Voltage, Micropower Linear Regulator

Completely Integrated Thermocouple Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

AD7124-4 Evaluation Board (EVAL-AD7124-4SDZ) or
AD7124-8 Evaluation Board (EVAL-AD7124-8SDZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is an integrated thermocouple measurement system based on the AD7124-4/AD7124-8 low power, low noise, 24-bit, Σ-Δ analog-to-digital converter (ADC), optimized for high precision measurement applications. Thermocouple measurements using this system show an overall system accuracy of ±1°C over a measurement temperature range of −50°C to +200°C . Typical noise free code resolution of the system is approximately 15 bits.

The AD7124-4 can be configured for 4 differential or 7 pseudo differential input channels, while the AD7124-8 can be configured for 8 differential or 15 pseudo differential channels. The on-chip low noise programmable gain array (PGA) ensures that signals of small amplitude can be interfaced directly to the ADC.

The AD7124-4/AD7124-8 establishes the highest degree of signal chain integration, which includes programmable low drift excitation current sources, bias voltage generator, and internal reference. Therefore, the design of a thermocouple system is simplified when the AD7124-4/AD7124-8 is used because most of the required system building blocks are included on-chip.

The AD7124-4/AD7124-8 gives the user the flexibility to employ one of three integrated power modes, where the current consumption, range of output data rates, and rms noise are tailored with the power mode selected. The current consumed by the AD7124-4/AD7124-8 is only 255 µA in low power mode and 930 µA in full power mode. The power options make the device suitable for non-power critical applications, such as input/output modules, and also for low power applications, such as loop-powered smart transmitters where the complete transmitter must consume less than 4 mA.

The device also has a power-down option. In power-down mode, the complete ADC along with its auxiliary functions are powered down so that the device consumes 1 µA typical. The AD7124-4/AD7124-8 also has extensive diagnostic functionality integrated as part of its comprehensive feature set.

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Fax: 781.461.3113

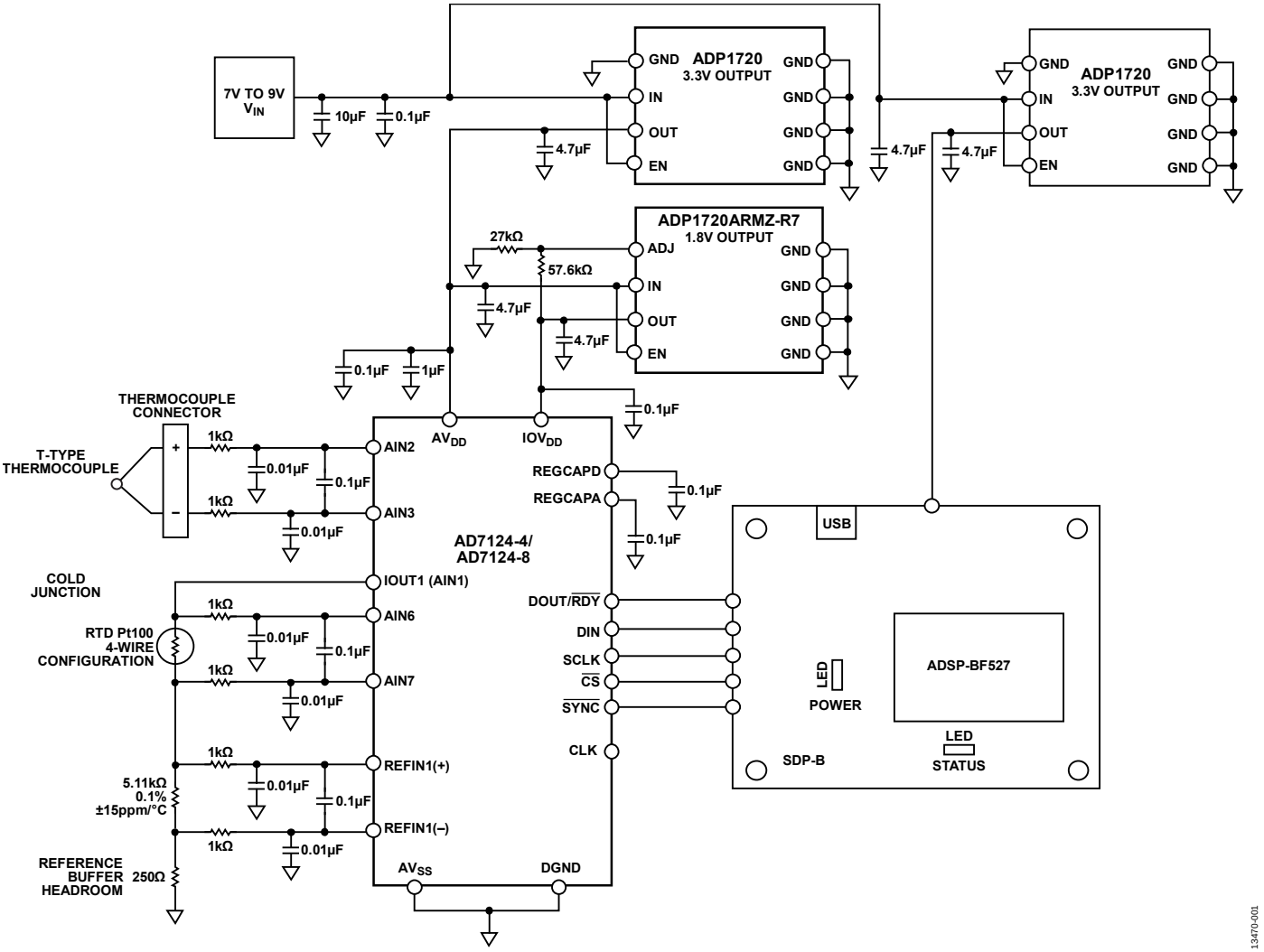

Figure 1. AD7124-4/AD7124-8 Thermocouple Measurement Configuration Including RTD Cold Junction Compensation

CIRCUIT DESCRIPTION

Temperature Measurement Introduction

Thermocouples are one of the most frequently used sensors for temperature measurements in industrial applications because of their low cost, ruggedness, repeatability, as well as wide operating temperature range and fast response time. Thermocouples are especially useful for making measurements at high temperatures (up to 2300°C for C-type thermocouples).

A thermocouple consists of the junction of two wires of different metal types, as shown in Figure 2.

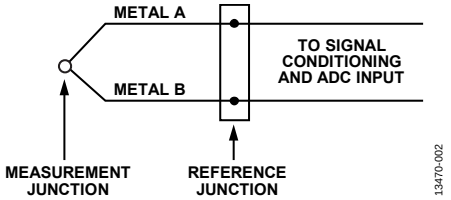

Figure 2. Thermocouple Connection Showing Measurement and Reference Junctions

The junction is placed where the temperature is to be measured, and is referred to as the measurement junction. The other end of the thermocouple is connected to a precision voltage measurement unit, and this connection is referred to as the reference junction, or alternately the cold junction. The temperature difference between the measurement junction and the cold junction generates a voltage that is proportional to the difference between the temperatures of the two junctions. The signal generated is typically from several microvolts to tens of millivolts and is dependent on the temperature difference. In the circuit shown in Figure 1, a T-type thermocouple is used. T-type thermocouples are capable of measuring temperatures of −200°C to +400°C with an output range of approximately −8.6 mV to +17.2 mV. It is important for the signal chain to present a high impedance and low leakage to the thermocouple to achieve the highest accuracy.

T-type thermocouples have a sensitivity of approximately 40 µV/°C. Therefore, by using the integrated PGA of the AD7124-4/AD7124-8, the small thermocouple voltage levels

can be easily sensed and accurately converted to a digital representation. The thermocouple response is approximately linear over a small portion of the range (0°C to 60°C), as shown in Figure 3. For accurate measurements over a wide temperature range, a linearization routine must be applied to the measured value to ensure accurate temperature values.

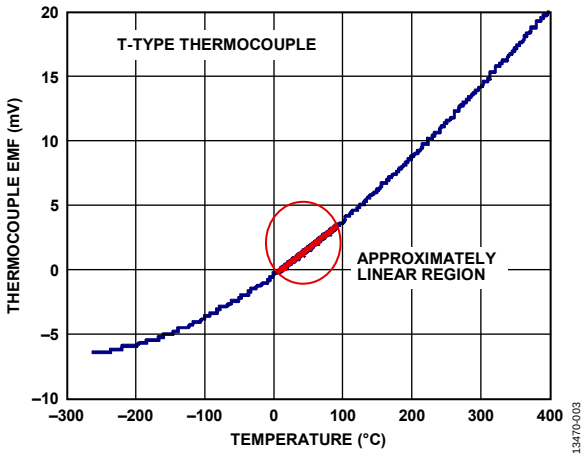

Figure 3. T-Type Thermocouple Output Voltage vs. Temperature

T-type thermocouples are formed by joining copper and constantan metals. Other combinations of metals form other types of thermocouples with various ranges and sensitivities. For instance, J-type thermocouples are made by joining iron and constantan and have a range of 0°C to 760°C with a sensitivity of 55 µV/°C. K-type thermocouples are made by joining chromel and alumel and have a range of −200°C to +1260°C with a sensitivity of 39 µV/°C.

Cold Junction Compensation (CJC)

The voltage generated by a thermocouple must be converted to temperature. Converting the voltage measured to an accurate temperature can be difficult because the thermocouple voltage is small, the temperature-voltage relationship is nonlinear, and the cold junction temperature must also be accurately measured.

The output voltage of the thermocouple represents the difference between the temperature of the thermocouple and the cold junction temperature. The cold junction temperature must be known to ensure an accurate absolute temperature reading from the thermocouple. The cold junction temperature is measured with another temperature sensitive device, typically a thermistor, diode, resistance temperature detector (RTD), or semiconductor temperature sensor. The temperature-sensing device used for this circuit is a 4-wire RTD. The cold junction measurement error contributes directly to the absolute temperature error; therefore, a high accuracy cold junction temperature measurement is required. The technique of measuring and compensating for the cold junction temperature is referred to as cold junction compensation, or CJC.

How the Circuit Works

The AD7124-4/AD7124-8 provides an integrated solution for thermocouple measurements. The AD7124-4/AD7124-8 can achieve high resolution, low nonlinearity, and low noise performance as well as high 50 Hz and 60 Hz rejection. The device consists of an on-chip, low noise PGA that amplifies the small signal from thermocouple with a gain programmable from 1 to 128, thus allowing direct interface with the sensor. The gain stage has high input impedance and limits the input leakage current to 3.3 nA typical for full power mode and 1 nA typical for low power mode. The following sections discuss the different elements used to develop a thermocouple temperature measurement system based on the AD7124-4/AD7124-8.

Power Supplies

The AD7124-4/AD7124-8 has separate analog and digital power supplies. The digital power supply, IOV_{DD}, is independent of the analog power supply and can be 1.65 V to 3.6 V referenced to DGND. The analog power supply, AV_{DD}, is referred to AV_{SS} and has a range of 2.7 V to 3.6 V for low power mode and mid power mode, and 2.9 V to 3.6 V for full power mode. The circuit shown in Figure 1 operates from a single supply; therefore, AV_{SS} and DGND are connected together, and only one ground plane is used. The AV_{DD} and IOV_{DD} voltages are generated separately using ADP1720 low dropout voltage regulators. The AV_{DD} voltage is set to 3.3 V and the IOV_{DD} voltage is set to 1.8 V using the ADP1720 regulators. Using separate regulators ensures the lowest noise.

Serial Peripheral Interface (SPI)

SPI communication to the AD7124-4/AD7124-8 is handled by the Blackfin® ADSP-BF527 on the EVAL-SDP-CB1Z board, as shown in Figure 1. To access the registers of the AD7124-4/AD7124-8, use the AD7124-4/AD7124-8 EVAL+ Software. Figure 4 shows the main window of this software. Clicking **THERMOCOUPLE** configures the software for a T-type thermocouple measurement.

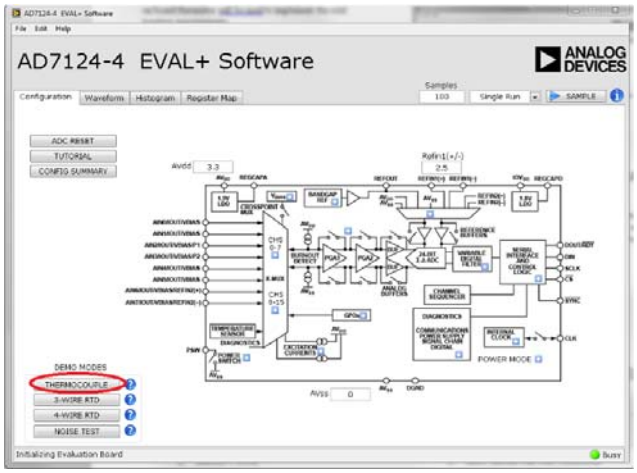

Figure 4. AD7124-4/AD7124-8 EVAL+ Software Configuration Screen

The AD7124-4/AD7124-8 has diagnostic functions on-chip that can be used to detect faults in the SPI communication. These diagnostics include checks on the SPI read and write operations, ensuring that only valid registers are accessed. An SCLK counter ensures that the correct number of SCLK pulses are used, while the CRC functionality checks for changes in bit values during transmission. When any of these SPI communication diagnostic functions are enabled and an associated error occurs, the corresponding flag is set in the error register. All enabled flags are OR'ed together and control the ERR flag in the status register. This functionality is particularly useful if the status bits are appended to the ADC conversions.

Analog Inputs

The AD7124-4 can be configured for 4 differential or 7 pseudo differential input channels, while the AD7124-8 can be configured for 8 differential or 15 pseudo differential input channels.

The AD7124-4/AD7124-8 has on-chip diagnostics that can be used to check that the voltage level on the analog pins are within the specified operating range. The positive (AINP) and negative (AINM) analog inputs can be separately checked for overvoltages and undervoltages, as well as ADC saturation. An overvoltage is flagged when the voltage on the analog input exceeds AV_{DD}, while an undervoltage is flagged when the voltage on the analog input goes below AV_{SS}.

For the circuit shown in Figure 1, two analog input pins are used to connect the thermocouple (AIN2, AIN3), and three analog pins are needed for the cold junction compensation (AIN1, AIN6, AIN7). AIN2 and AIN3 are configured as a fully differential input channel and measure the voltage generated by the thermocouple. For this circuit, the thermocouple is floating as shown in Figure 1. To bias the thermocouple to a known level, the V_{BIAS} voltage generator is enabled on AIN2 and biases the thermocouple to

$$V_{BIAS} = AV_{SS} + \left(\frac{AV_{DD} - AV_{SS}}{2}\right)$$

The thermocouple measurement is an absolute measurement; therefore, a voltage reference is needed, and the AD7124-4/AD7124-8 internal 2.5 V reference is used.

For the cold junction compensation, one excitation current source is used to excite the RTD. This current is generated from AV_{DD} and is directed to AIN1. The analog pins and their configuration are shown in greater detail in Figure 5.

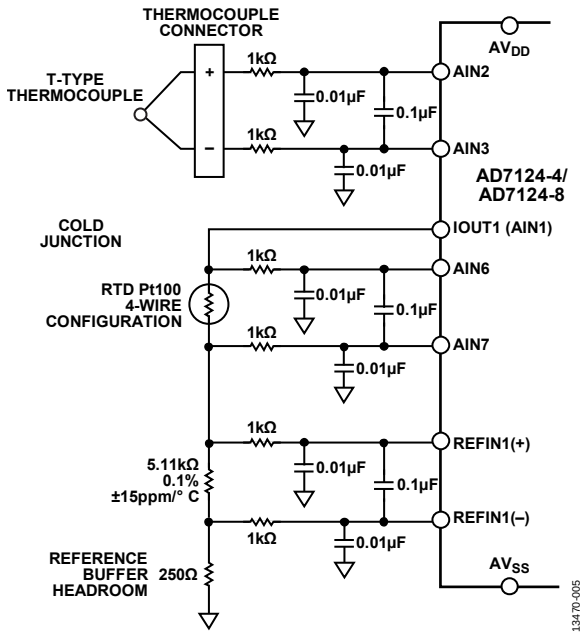

Figure 5. Analog Input Configuration for Thermocouple Measurement Using 4-Wire RTD for Cold Junction Compensation

For this circuit, the cold junction circuit utilizes the reference input, REFIN1(±). The current through the 4-wire RTD used for the cold junction measurement also flows through the precision reference resistor that generates the reference voltage. The voltage generated across this precision reference resistor is ratiometric to the voltage across the RTD; therefore, any variations seen in the excitation current are removed. Because the reference buffers are enabled, it is necessary to ensure that the headroom required for correct operation is met (AV_{DD} – 0.1 V and AV_{SS} + 0.1 V). The headroom of 0.125 V (500 µA × 250 Ω) is provided by the 250 Ω resistor to ground, as shown in Figure 5.

Digital and Analog Filtering

Differential (~800 Hz cutoff) and common-mode (~16 kHz cutoff) filters are implemented at the analog inputs as well as at the reference inputs. This filtering is required to reject any interference at the modulator frequency and also any multiples of this frequency.

The AD7124-4/AD7124-8 offers a great deal of on-chip digital filtering flexibility. There are several filter options available; the option selected has an effect on the output data rate, settling time, as well as 50 Hz and 60 Hz rejection. For this circuit note, the sinc^4 filter and the post filter are implemented. The sinc^4 filter is used because it has excellent noise performance across the range of output data rates, as well as excellent 50 Hz and 60 Hz rejection. The post filter is used to provide simultaneous 50 Hz and 60 Hz rejection with a 40 ms settling time.

Calibration

The AD7124-4/AD7124-8 provides different calibration modes that can be used to eliminate offset and gain errors. For this circuit note, internal zero-scale calibration as well as internal full-scale calibrations were used.

Thermocouple Configuration

The circuit shown in Figure 1 is designed for precision T-type thermocouple measurement using the AD7124-4/AD7124-8. Thermocouple measurements require cold junction compensation. As shown in Figure 1, a 4-wire Pt100 RTD is used for this purpose. Using the configuration shown in Figure 1, one precision excitation current source is required to excite the RTD as part of the cold junction compensation measurement. The RTD is connected to analog inputs AIN6, AIN7. The bottom side of the RTD is connected to a precision reference resistor, which applies an external reference voltage to the device. The precision reference resistor is connected between reference input pins REFIN1(±). This configuration represents a ratiometric configuration, where any deviation in the excitation current is seen by both the RTD and the reference resistor, and is therefore removed from the measurement.

The thermocouple itself is connected to the AIN2, AIN3 analog inputs. One of the inputs is biased using the internal bias voltage generator of the ADC. The thermocouple voltage is in the range of −8 mV to +17.2 mV, which represents a temperature range of −200°C to +400°C. This low level voltage is amplified by the on-board PGA of the AD7124-4/AD7124-8, which is converted to a precision digital representation using the 24-bit Σ-Δ ADC. To ensure that the full range of the ADC is utilized, the PGA gain is set to 128. This thermocouple measurement is made with respect to the internal low drift 2.5 V reference.

A 4-wire Pt100 Class B RTD is used for the cold junction measurement. The excitation current for the Pt100 RTD is programmed to 500 µA.

The value of the external precision resistor is chosen so that the maximum voltage generated across the RTD equals the reference voltage divided by the selected gain. The Circuit Note CN-0381 discusses in detail the following required steps:

- Selecting a precision reference resistor
- Selecting an appropriate PGA gain for RTD measurement
- Headroom resistor selection
- Excitation current output compliance

The AD7124-4/AD7124-8 full system configuration for the thermocouple measurement is as follows:

- Thermocouple measurement (T-type)
  - Differential input (AINP = AIN2, AINM = AIN3)
  - Gain = 128
  - Internal 2.5 V reference
  - Digital filtering (sinc^4 and post filter)
- Cold junction compensation measurement (4-wire RTD)
  - Differential input (AINP = AIN6, AINM = AIN7)
  - Excitation current: IOUT1 = AIN1= 500 µA
  - Gain = 16
  - 5.11 kΩ precision reference resistor
  - Digital filtering (sinc^4 and post filter)

Thermocouple Temperature Calculation

Once the previous procedure is implemented, the next step is to work through the thermocouple and cold junction calculations. Different approaches can be used for the linearization/ compensation, which include

- Look-up table: requires memory for storage, but also provides a quick, accurate conversion.
- Software linear approximation: does not require storage except for the conversion polynomial coefficients. Requires processing time to solve the multiple order polynomial. However, it also yields a very accurate result. This is the method used for this circuit.

The software linear approximation requires two inputs: the voltage measured across the thermocouple, and the cold junction temperature.

The analog input channel (AIN2, AIN3) is used to measure the voltage across the thermocouple. The formula used to convert the code representation to a voltage is Equation 1, which assumes a bipolar configuration of the ADC. The AD7124-4/AD7124-8 software automatically converts the codes to a voltage based on the configuration implemented.

$$V_{TC} = \frac{(CODE_{TC} - 2^{N-1}) \times V_{REF}}{2^{N-1} \times Gain} \quad (1)$$

where:
V_{TC} is the thermocouple (TC) voltage.
$CODE_{TC}$ is the thermocouple (TC) code.
N is the resolution of ADC, 24.
V_{REF} is the reference used for measurement. For this circuit, the internal reference is used for the thermocouple measurement.
$Gain$ is the chosen gain for TC mode, 128.

The 4-wire RTD used for the cold junction requires its own linearization. The general expression to calculate the RTD resistance (R) where the ADC is operating in bipolar mode is given by

$$R_{RTD} = \frac{(CODE - 2^{N-1}) \times R_{REF}}{G \times 2^{N-1}} \quad (2)$$

where:
R_{RTD} is the resistance of the RTD.
$CODE$ is the ADC code.
N is the resolution of ADC, 24.
R_{REF} is the reference resistor.
G is the selected gain, 16.

The steps involved in converting the RTD voltage to a temperature and the linearization are outlined in the Circuit Note CN-0381.

The following steps are required to calculate the thermocouple temperature:

- Convert the cold junction temperature to a voltage
- Calculate the thermoelectric voltage
- Convert the thermoelectric voltage to a temperature representation

The cold junction temperature must be converted to a voltage. The cold junction temperature is converted using a polynomial generated by National Institute of Standards and Technology (NIST) and is outlined in Equation 3.

$$V_{CJ} = a_0 + a_1T + a_2T^2 + \ldots + a_nT^n \quad (3)$$

where:
V_{CJ} is the thermoelectric voltage.
a_x is the thermocouple type dependent polynomial coefficient.
T is the cold junction temperature (°C).
n is the order of the polynomial.

The cold junction temperature-to-voltage conversion accuracy can be increased by increasing the order of the polynomial. However, the higher the order, the more processing is required. Therefore, a trade-off is required when carrying out this conversion. For the calculations implemented for this circuit, an eighth-order polynomial was used.

The cold junction temperature voltage must be added to the differential voltage measured across the thermocouple. The resulting voltage is an approximation of the thermoelectric voltage generated by the temperature sensing junction of the thermocouple.

The thermoelectric voltage can then be used to calculate the overall thermocouple temperature. This step involves a power series polynomial given by Equation 4. For this circuit, a sixth-order polynomial was used, where the T-type thermocouple polynomial coefficients were taken from the NIST website.

$$T = a_0 + a_1V + a_2V^2 + a_3V^3 + \ldots + a_nV^n \quad (4)$$

where:
V is the thermoelectric voltage (microvolts).
a_x is the type dependent polynomial coefficient.
T is the temperature (°C).
n is the order of polynomial.

Thermocouple Measurements and Results

For the circuit shown in Figure 1, data was gathered for different digital filter and power mode configurations of the AD7124-4/AD7124-8.

The first configuration was with the sinc^4 filter, full power mode, with an output data rate of 50 SPS. These conditions optimize the AD7124-4/AD7124-8 for best performance in relation to speed and noise. Figure 6 shows the noise distribution when a thermocouple is connected between the AIN2, AIN3 input channel as shown in Figure 1 at ambient temperature. The corresponding rms noise is typically 70 nV rms or approximately 16.4 noise free bits. The noise performance of the AD7124-4/AD7124-8 for inputs shorted under the same conditions is typically 48 nV rms or 17 noise free bits. The increase in the noise comes directly from the thermocouple that is connected across the input channel (AIN2, AIN3).

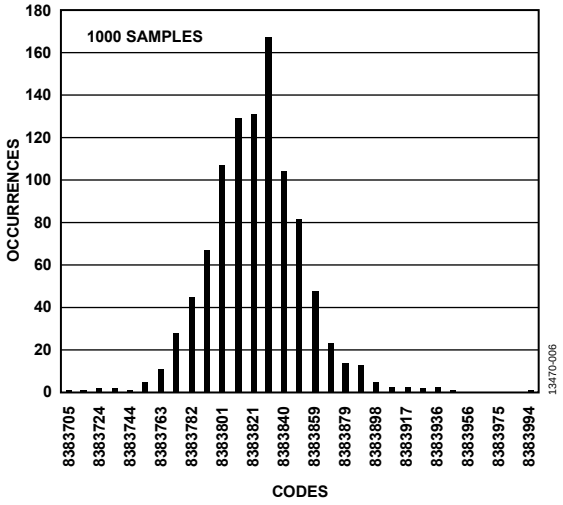

Figure 6. Histogram of Codes for Thermocouple at Ambient, Sinc^4 Filter, Full Power Mode, 50 SPS

For the thermocouple configuration where the sinc^4 filter and full power mode were selected, the temperature of the thermocouple was swept from −50°C to +200°C, while the cold junction was held at −40°C, +25°C, and +105°C. For each of the set thermocouple temperatures, the corresponding voltage across the thermocouple was measured using the AD7124-4/AD7124-8 as previously outlined. Also recorded was the cold junction temperature using the 4-wire RTD. The voltage of the thermocouple along with the voltage representation of the cold junction temperature were used to calculate the temperature of the thermocouple. Figure 7 shows the resulting error measured between the set temperature value and measured temperatures of the thermocouple after linearization, for cold junction temperatures of −40°C, +25°C, and +105°C. Internal zero-scale and full-scale calibrations were performed at each cold junction temperature. As shown in Figure 7, the error between the calculated and set temperature of the thermocouple is well within the root sum square combined error window of the T-type thermocouple and Pt100 RTD, as shown in the plot. The T-type thermocouple has a maximum error of 1°C, or 0.75%, and from the IEC751 Standard, the Pt100 error is ±(0.3 + 0.005 × |T|).

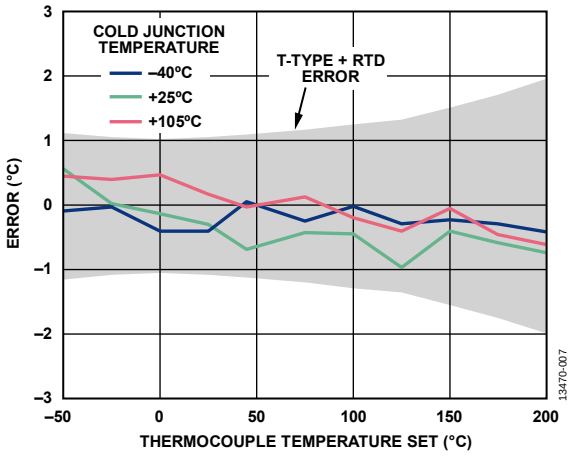

Figure 7. Thermocouple Temperature Accuracy Measurement, Sinc^4 Filter, Full Power Mode, 50 SPS

The second configuration tested was with the post filter, low power mode, and a 25 SPS output data rate that gives simultaneous 50 Hz and 60 Hz rejection, allowing the user to trade off settling time with rejection. Figure 8 shows the noise distribution when a thermocouple is connected between the AIN2, AIN3 input channel as shown in Figure 1 at ambient temperature. The corresponding rms noise is typically 220 nV rms equating to approximately 14.7 noise free bits. The noise performance of the AD7124-4/AD7124-8 for inputs shorted when the same filter, gain, and output data rate are selected is typically 170 nV rms or 15.1 noise free bits. The increase in the noise comes directly from the thermocouple that is connected across the input channel (AIN2, AIN3).

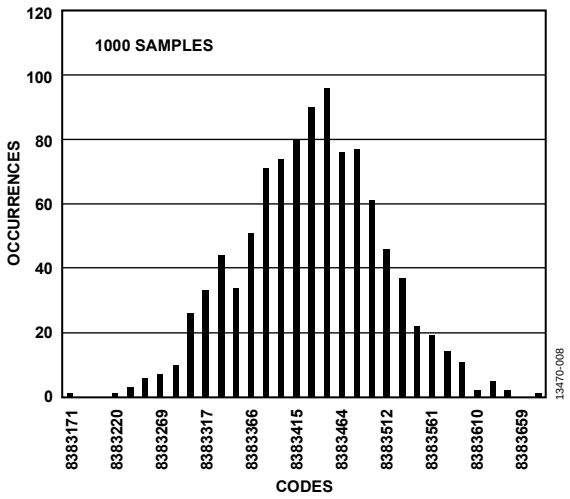

Figure 8. Histogram of Codes for Thermocouple and Cold Junction Temperature at Ambient, Post Filter, Low Power Mode, 25 SPS

For this AD7124-4/AD7124-8 configuration (with the post filter and low power mode selected), the temperature of the RTD was swept from −50°C to +200°C. For each of the set thermocouple temperatures, the corresponding voltage across the thermocouple was measured using the AD7124-4/AD7124-8, as outlined previously. Also recorded was the cold junction temperature using the 4-wire RTD. The voltage of the thermocouple along with the voltage representation of the cold junction temperature were used to calculate the temperature of the thermocouple.

Figure 9 shows the resulting error between the set and measured temperatures of the thermocouple after linearization for cold junction temperatures of −40°C, +25°C, and +105°C. As shown in Figure 9, the error between the calculated and set temperature of the thermocouple is well within the root sum square combined error window of the T-type thermocouple and Pt100 RTD, as shown in the plot. The T-type thermocouple has a maximum error of 1°C or 0.75%, and the Pt100 error is ±(0.3 + 0.005 × |T|) from the IEC751 Standard.

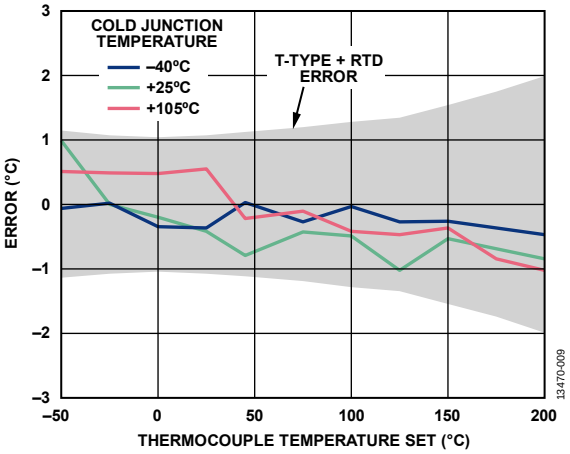

Figure 9. Thermocouple Temperature Accuracy Measurement, Post Filter, Low Power Mode, 25 SPS

COMMON VARIATIONS

Cold Junction Measurement Alternative

The EVAL–AD7124-4SDZ/EVAL-AD7124-8SDZ evaluation boards have a thermistor on board as part of the overall board design. This thermistor is a KTY81/110 and has a typical resistance of 1 kΩ at +25°C, 500 Ω at −40°C, and 1.7 kΩ at +105°C. The thermistor can be used for measuring the cold junction temperature. Thermistors are cheaper than 4-wire RTDs, but are not as accurate. When implementing a thermistor for cold junction measurements, care must be taken to ensure that the cold junction measurement works as expected. The following steps outline some decisions that need consideration:

1. Choose the precision reference resistor value.
2. Choose the appropriate gain.
3. Choose the excitation current.
4. Check the output voltage compliance range of the excitation current.
5. Check the resistance value of the thermistor for the different cold junction temperatures.

Taking all of these steps into consideration, the settings for implementing this thermistor when measuring the cold junction temperature as part of the overall temperature measurement system requires the following register configurations:

- Thermocouple measurement settings as outlined previously (T-type)
  - Differential input (AINP = AIN2, AINM = AIN3)
  - Gain = 128
  - Internal 2.5 V reference
  - Digital filtering (sinc^4 and post filter)
- Cold junction compensation measurement (thermistor)
  - Differential input (AINP = AIN4, AINM = AIN5)
  - Excitation current: IOUT0 = AIN1 = 500 µA
  - Gain = 1
  - 2 kΩ precision reference resistor (the thermistor resistance varies from 500 Ω at −40°C to 1.7 kΩ at +105°C; it is also required to evaluate the headroom with this resistance)

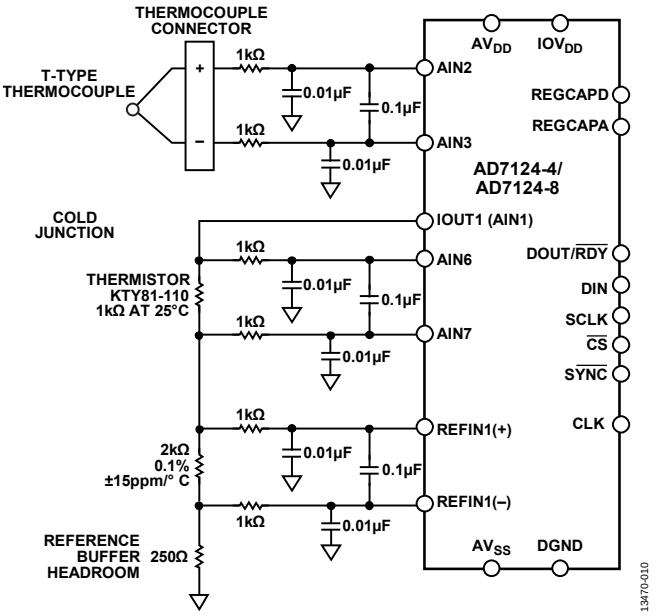

Figure 10. Thermistor Cold Junction Configuration for Thermocouple Measurements

Using the setup configuration shown in Figure 10, the reference to the AD7124-4/AD7124-8 is always approximately 1 V based on the 500 µA current and the 2 kΩ precision reference resistor. The performance of the system when the thermistor is used for cold junction compensation was recorded where the cold junction was held at 25°C, and the temperature of the thermocouple swept from −50°C to +200°C. The sinc^4 filter in full power mode and the post filter in low power mode were used. Figure 11 shows the worst-case error recorded between the set temperature of the thermocouple, and the calculated temperature using the linearization technique for both filter types and power modes. The worst case error recorded was ±1°C.

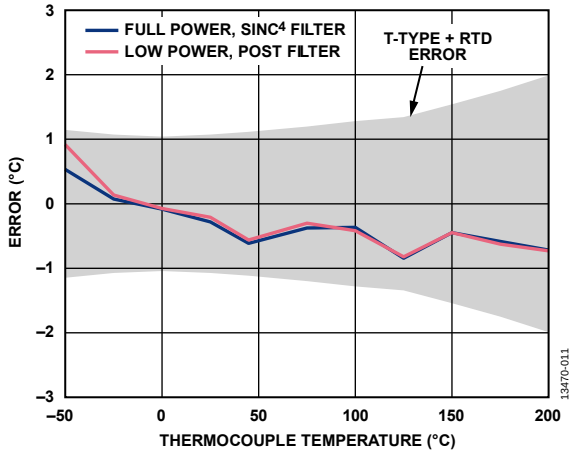

Figure 11. Thermocouple Temperature Accuracy Measurement Using Thermistor for Cold Junction Compensation at 25°C

Bias Voltage

In Figure 1, the internal V_{BIAS} voltage is supplied to the thermocouple via the AINP or AINM pins. This configuration for the V_{BIAS} voltage works well when the anti-alias filters are implemented using the component values shown in Figure 1. If filters with very large R and C values are used (for example, for EMC filtering), V_{BIAS} must be taken from a separate dedicated pin and then applied externally to the thermocouple. This removes any inaccuracies in the measurements caused by potential common-mode noise that can be converted to differential-mode noise.

Multiple Thermocouple Measurement System

The AD7124-4 and AD7124-8 can be used for multiple thermocouple measurements. Thermocouple measurements require

- Two analog pins configured differentially to measure the voltage across the thermocouple
- Two analog pins configured differentially to measure the voltage at the cold junction terminal
- One single analog pin to steer the excitation current to the cold junction compensation circuitry

Using this information, the AD7124-4 allows two thermocouples to be connected and measured with respect to the same cold junction, as shown in Figure 12. The AD7124-8 allows up to six different thermocouple measurements with respect to the same cold junction, as shown in Figure 13.

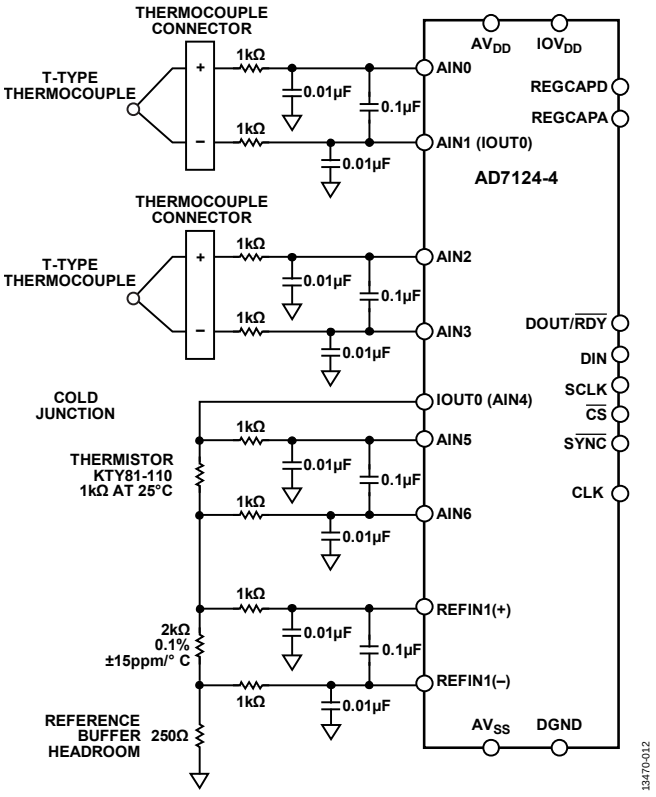

Figure 12. AD7124-4—Two Thermocouple Measurement System Including Cold Junction Compensation

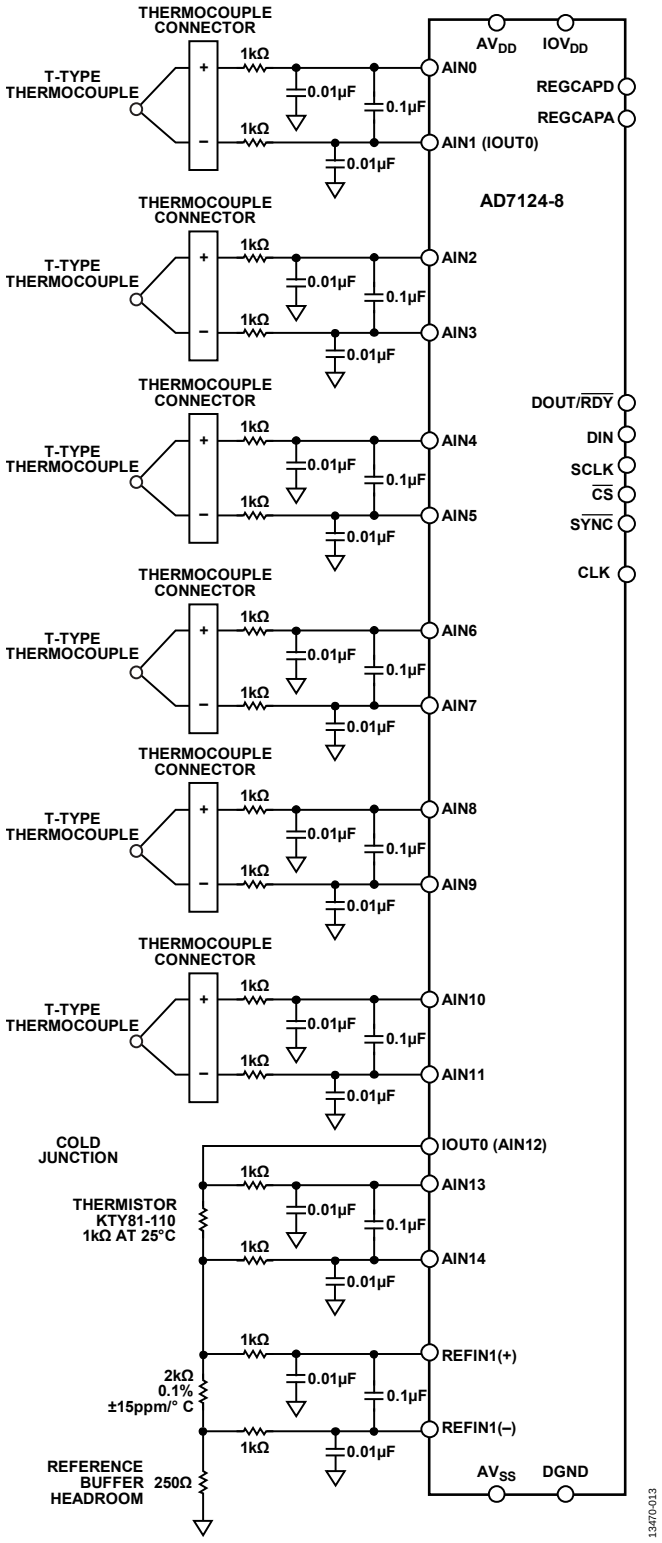

Figure 13. AD7124-8—Six Thermocouple Measurement System Including Cold Junction Compensation

CIRCUIT EVALUATION AND TEST

Equipment Needed

The following equipment is required for the thermocouple measurement system:

- EVAL–AD7124-4SDZ/EVAL-AD7124-8SDZ evaluation board
- EVAL-SDP-CB1Z System Demonstration Platform (SDP)
- AD7124-4/AD7124-8 EVAL+ Software
- Power supply: 7 V or 9V wall wart
- T-type thermocouple
- A PC running Windows® XP (SP2), Windows Vista, or Windows 7 (32-bit or 64-bit)

Software Installation

A complete software user guide for the EVAL–AD7124-4SDZ/ EVAL-AD7124-8SDZ and SDP boards can be found in the EVAL–AD7124-4SDZ/EVAL-AD7124-8SDZ user guide and the SDP User Guide, respectively.

Software is required to interface with the hardware, and can be downloaded from ftp://ftp.analog.com/pub/evalcd/AD7124 . If the setup file does not automatically run, double-click **setup.exe** from the file. Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

After the evaluation software installation is complete, connect the SDP board (via Connector A) to the evaluation board, and then connect the evaluation board to the USB port of the PC using the supplied cable. When the evaluation system is detected, proceed through any dialog boxes that appear to complete the installation.

Setup and Test

Figure 14 shows the functional block diagram of the test setup. To allow quick setup for thermocouple measurements, the on-board thermistor is used to implement the cold junction measurements.

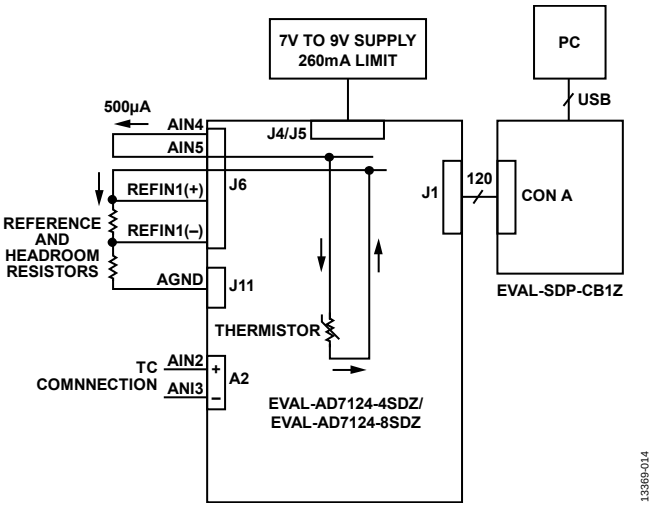

Figure 14. Test Setup Functional Diagram

The EVAL–AD7124-4SDZ/ EVAL-AD7124-8SDZ evaluation board is needed to test the circuit. In addition, the following sensor and resistors are required for proper operation:

- T-type thermocouple
- 2 kΩ precision resistor
- 250 Ω resistor needed for buffer headroom

Configuring the Hardware

To configure the hardware, do the following:

- Set all links on the EVAL-AD7124-4SDZ/EVAL-AD7124-8SDZ to the default board positions as outlined in the evaluation board user guide.
- Power the board with a 7 V or 9 V power source connected to J5.
- Connect the thermocouple, precision reference resistor, and resistor for headroom as shown in Figure 15.

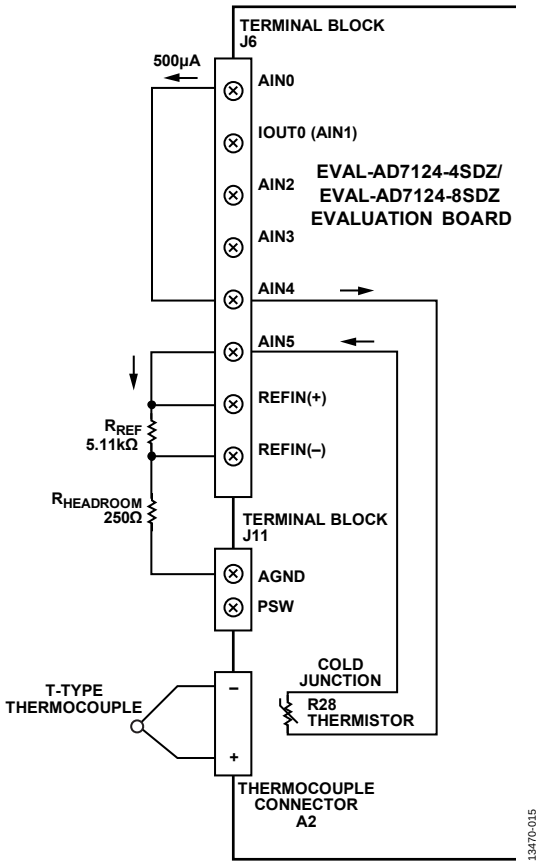

Figure 15. Evaluation Board Connector for Thermocouple Measurement

Configuring the Software

Run the AD7124-4/AD7124-8 EVAL+ Software. Figure 16 shows a screenshot of the main window of the software.

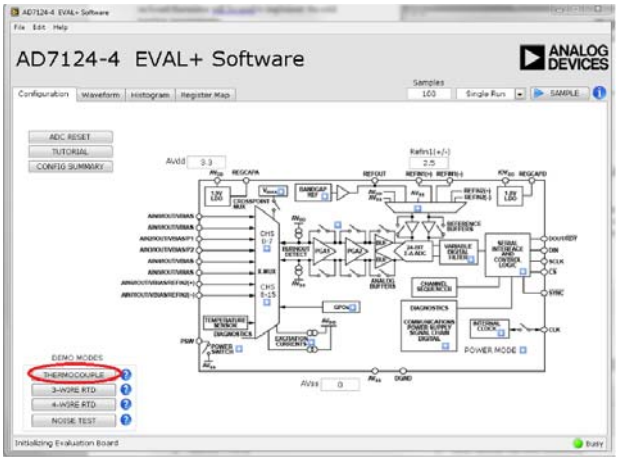

Figure 16. AD7124-4/AD7124-8 EVAL+ Software Main Window

To configure the AD7124-4/AD7124-8 for thermocouple measurements, click the **THERMOCOUPLE** demo mode button in the main window, as shown in Figure 16. Clicking this button configures the ADC software for optimized performance. Some of the register settings are as follows:

- Channel_0 (thermocouple)
  - AINP_0 = AIN2
  - AINM_0 = AIN3
  - Setup = Setup0
  - Enabled = TRUE
- Channel_1 (thermistor cold junction measurement)
  - AINP_1 = AIN4
  - AINM_0 = AIN5
  - Setup = Setup1
  - Enabled = TRUE
- CONFIG_0 (thermocouple)
  - PGA_0 = 128
  - AIN_BUFP, AIN_BUFM both = ENABLED
  - BIPOLAR = ENABLED
  - REF_SEL = Internal Reference
- CONFIG_1 (thermistor cold junction measurement)
  - PGA_0 = 1
  - AIN_BUFP, AIN_BUFM both = ENABLED
  - BIPOLAR = ENABLED
  - REF_SEL = External Reference
- FILTER_0 (thermocouple)
  - Filter = Sinc4
  - FS_0 = 384
- FILTER_1 (thermistor cold junction)
  - Filter = Sinc4
  - FS_0 = 384
- ADC_Control
  - MODE = Continuous Conversion
  - POWER_MODE = FULL POWER
  - REF_EN = Enabled
- IO_CONTROL_1 (excitation for RTD)
  - IOUT1 Channel Enable = AIN1
  - IOUT1 Select = 500 µA
- IO_CONTROL_2 (biasing the thermocouple)
  - VBIAS2 = True

One additional step is required before the AD7124-4/AD7124-8 is configured for thermocouple measurements: an internal full-scale and zero-scale calibration of the AD7124-4/AD7124-8 is required for the thermocouple channel. This can be performed via the **Register Map** tab, as shown in Figure 17.

1. From the register tree, select the **ADC_Control** register.
2. Enable Channel 0 only.
3. Select low power mode.
4. Carry out an internal full-scale calibration.
   a. Click the **Mode** bitfield of the ADC control register.
   b. Select internal full-scale calibration.
   c. Check that the calibration has been performed by selecting the **Gain0** register from the register tree, and check that the coefficients have changed.
5. Carry out an internal zero-scale calibration.
   a. Click the **Mode** bitfield of the ADC control register.
   b. Select internal zero-scale calibration.
   c. Check that the calibration has been performed by selecting the **Offset0** register in the register tree, and check that the coefficients have changed.

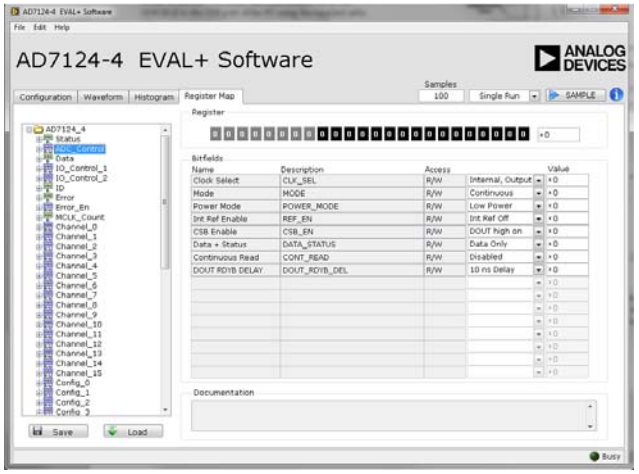

Figure 17. Register Map Internal Full-Scale and Zero-Scale Calibration

A calibration is not required for the thermistor channel because the gain error at a gain of 1 is factory calibrated.

The board and device are now configured for thermocouple measurements, which includes cold junction compensation measurement using the thermistor positioned on the evaluation board. Click **SAMPLE** to start gathering samples from the AD7124-4/AD7124-8. The **Waveform** tab and the **Histogram** tab show the data gathered from the AD7124-4/AD7124-8.

For more accurate cold junction measurements, a 4-wire RTD can be connected, as outlined in the previous sections. To use a 4-wire RTD, the current from AIN1 must be disconnected from the thermistor and connected to the 4-wire RTD, as shown in Figure 1.

LEARN MORE

CN-0384 Design Support Package:
www.analog.com/CN0384-DesignSupport

SDP User Guide

EVAL-AD7124-4 User Guide (UG-855)

EVAL-AD7124-8 User Guide (UG-856)

AN-892 Application Note. *Temperature Measurement Theory and Practical Techniques.* Analog Devices.

Kester, Walt. "Temperature Sensors," Chapter 7 in *Sensor Signal Conditioning.* Analog Devices, 1999.

Mary McCarthy. AN-615 Application Note. *Peak-to-Peak Resolution Versus Effective Resolution*. Analog Devices.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND".* Analog Devices.

MT-101 Tutorial. *Decoupling Techniques.* Analog Devices.

CN-0376 Circuit Note. *Channel-to-Channel Isolated Temperature Input (Thermocouple/RTD) for PLC/DCS Applications.* Analog Devices.

CN-0381 Circuit Note. *Completely Integrated 4-Wire RTD Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC.* Analog Devices.

CN-0382 Circuit Note. *Isolated 4 mA to 20 mA/HART Temperature and Pressure Industrial Transmitter Using a Low Power, Precision, 24-Bit Sigma-Delta ADC.* Analog Devices.

CN-0383 Circuit Note. *Completely Integrated 3-Wire RTD Measurement System Using a Low Power, Precision, 24-Bit, Sigma-Delta ADC.* Analog Devices.

Data Sheets and Evaluation Boards

EVAL-AD7124-4SDZ

EVAL-AD7124-8SDZ

System Demonstration Platform (EVAL-SDP-CB1Z)

AD7124-4 Data Sheet

AD7124-8 Data Sheet

ADP1720 Data Sheet

REVISION HISTORY

7/15—Revision 0: Initial Version

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0387.

Devices Connected/Referenced	
ADL6010	Fast Responding, 45 dB Range, 0.5 GHz to 43.5 GHz Envelope Detector
AD7091R	1 MSPS, Ultralow Power, 12-Bit ADC in 10-Lead LFCSP and MSOP
HMC547	GaAs MMIC, SPDT, Nonreflective Switch, DC to 28 GHz

Calibration-Free Return Loss Measurement System

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0387 Return Loss Measurement Evaluation Board (EV-VSWR-SDZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 accurately measures return loss in a wireless transmitter from 1 GHz to 28 GHz without any need for system calibration.

The design is implemented on a single circuit board using a nonreflective RF switch; a microwave RF detector; and a 12-bit, precision analog-to-digital converter (ADC). To evaluate the circuit over the widest possible frequency range, a dual-port directional coupler with SMA connectors was used instead of a narrow-band, surface-mount directional coupler.

The circuit measures return loss of up to 20 dB over an input power range of 25 dB (return losses in excess of 20 dB can be measured over a smaller input power range).

A unique feature of the circuit is that it calculates return loss using a simple ratio of the digitized voltages from the RF detector, thereby eliminating the need for system calibration.

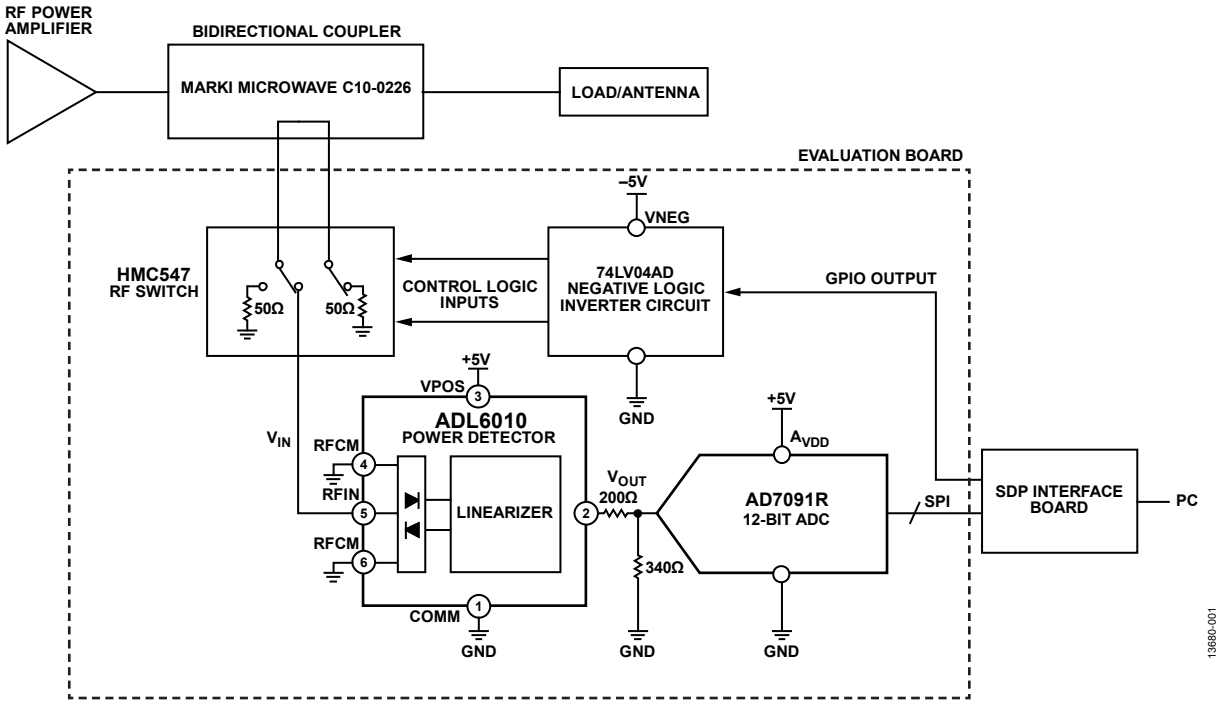

Figure 1. Voltage Standing Wave Ratio (VSWR) Evaluation Board Measurement Setup (All Connections and Decoupling Not Shown)

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Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

CIRCUIT DESCRIPTION

An RF signal between 1 GHz and 28 GHz is fed through an RF coupler (Marki Microwave C10-0226) to a matched 50 Ω load or antenna as shown in Figure 1. The forward and reverse coupled ports are connected to the HMC547, a single-pole/double-throw (SPDT) nonreflective switch. The switch input is toggled between the forward and reverse coupled ports, while terminating the opposite port in 50 Ω, so that both coupled ports always see a 50 Ω load.

The output port of the RF switch drives the ADL6010, a microwave RF detector that can operate from 500 MHz to 43.5 GHz. The output voltage level of the detector is directly proportional to the amplitude of the input signal. The ADL6010 is a linear-in-V/V detector, having a nominal slope of 2.1 V/V.

The AD7091R 12-bit ADC samples the power detector output voltage at a rate of 1 MSPS. (Lower sampling rates can also be used, resulting in lower power consumption in the ADC).

The AD7091R converts the analog voltage to a digital code. The EVAL-SDP-CB1Z (SDP-B) interface board then uses serial peripheral interface (SPI) communications to control the ADC and sends results to a PC for system evaluation and return loss calculation. The VSWR, return loss, and reflection coefficient are then calculated using the ratio between the forward and reverse coupled voltages sampled by the ADC.

Return Loss Calculation

The following derivation shows the relationship between the ratio of forward and reverse voltages and the return loss of the system. This relationship is fundamental to the calibration-free nature of the system.

The system transfer function of the detector in its linear operating region can be expressed using the familiar straight-line equation,

$$y = mx + c$$

where:
m is the slope.
c is the intercept.

Using actual circuit parameters,

$$V_{OUT} = m \times V_{IN} + c \quad (1)$$

As noted previously, m is nominally 2.1, but can vary with frequency and from device to device. The value of c is typically close to zero.

Rewriting Equation 1 in terms of V_{IN},

$$\Rightarrow V_{IN} = \frac{V_{OUT} - c}{m} \quad (2)$$

Converting this equation to power,

$$\Rightarrow P_{IN} = \frac{\left(\frac{V - c}{m}\right)^2}{R} \quad (3)$$

Then converting to dBm,

$$P_{IN_{dBm}} = 10 \times \log\left(1000 \times \frac{\left(\frac{V_{OUT} - c}{m}\right)^2}{R}\right) \quad (4)$$

If the ADC is included, the equation becomes

$$P_{IN_{dBm}} = 10 \times \log\left(1000 \times \frac{\left(\frac{CODE - c'}{m'}\right)^2}{R}\right) \quad (5)$$

where:
m' is the slope of the detector and ADC combined signal chain.
c' is the intercept of the detector and ADC combined signal chain.

The return loss is the difference between the forward and reverse power in dBm:

$$P_{F_{dBm}} - P_{R_{dBm}} = 10 \times \log\left(\frac{1000 \times \frac{\left(\frac{CODE_F - c'}{m'}\right)^2}{R}}{1000 \times \frac{\left(\frac{CODE_R - c'}{m'}\right)^2}{R}}\right) \quad (6)$$

$$\Rightarrow P_{F_{dBm}} - P_{R_{dBm}} = 10 \times \log\left(\frac{(CODE_F - c')^2}{(CODE_R - c')^2}\right) \quad (7)$$

Because c' is close to zero, and because $CODE_F$ and $CODE_R$ are generally much greater than c', the formula reduces to

$$P_{F_{dBm}} - P_{R_{dBm}} = 10 \times \log\left(\frac{CODE_F^2}{CODE_R^2}\right) \quad (8)$$

The derivation in this section shows that return loss can be calculated without the need for calibration, because the formula does not include the slope (m') or intercept (c') of the signal chain.

RF Switch

The HMC547 is a nonreflective SPDT RF switch with a frequency range of dc to up to 28 GHz. As shown in the Figure 2 block diagram, the switch internally terminates either input at 50 Ω, while the other input is fed to the RFC output. The switch has a fast switching time of typically 6 ns. The A and B logic inputs of this switch are controlled by negative voltage logic of −5 V high and 0 V low. A recommended control circuit is included in the HMC547 data sheet. The circuit consists of a 5.1 V Zener diode level shifter that drives 74LV04AD inverters. The inverters are powered between −5 V and 0 V, rather than 0 V and +5 V. The complete power supply circuit is shown in the detailed schematic contained in the CN-0387 Design Support Package, available at www.analog.com/CN0387-DesignSupport.

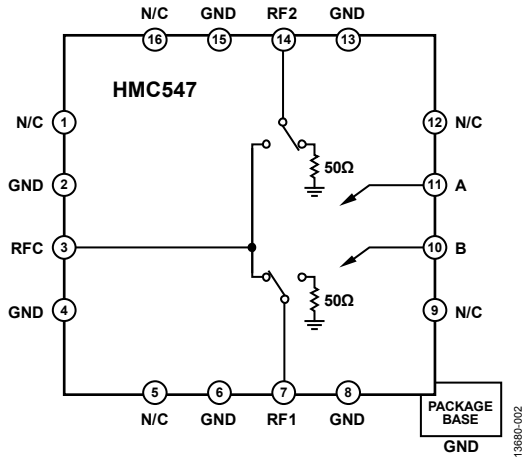


Figure 2. HMC 547 Top View

Power Detector

The ADL6010 power detector has a linear-in-V/V characteristic, which is key to this application. To power this device, apply a +5 V dc voltage to the VPOS pin and round to the COMM pin, as shown in Figure 3.

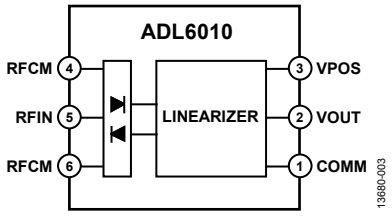


Figure 3. ADL6010 RF/Microwave Detector Functional Diagram

As shown in Figure 4, the output voltage varies with frequency. This variation in transfer function vs. frequency does not degrade the performance of the circuit in any way because the return loss calculation relies on a ratiometric calculation at a specific frequency.

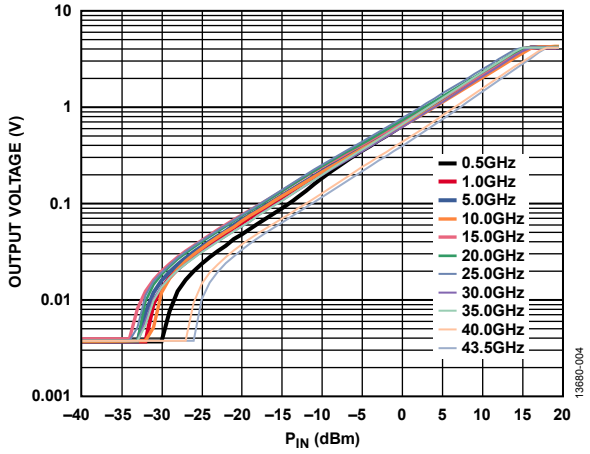
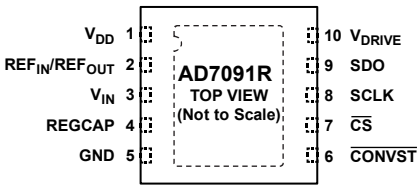


Figure 4. Transfer Function at Frequencies from 500 MHz to 43.5 GHz

Analog-to-Digital Converter



NOTES
1. THE EXPOSED PAD IS NOT CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND FOR MAXIMUM THERMAL CAPABILITY, SOLDER THE EXPOSED PAD TO THE SUBSTRATE, GND.

Figure 5. AD7091R Analog-to- Digital Converter

The AD7091R is a 12-bit successive approximation register (SAR) ADC, which has a throughput rate of up to 1 MSPS. Although a highly accurate external reference voltage can be used, it is not required in this application. In this circuit, the internal reference of 2.5 V is used, which yields an LSB size of

$$LSB = (2.5\ V)/2^{12} = 610\ \mu V$$

Because the output voltage of the ADL6010 can reach a maximum voltage of approximately 3 V, it is necessary to attenuate this voltage using a 200 Ω/340 Ω resistor divider between the detector and the ADC, as shown in Figure 1. This divider provides a nominal attenuation of 1.6.

Directional Coupler

A directional coupler couples a portion of the forward or reverse signals to the power detector for measurement. In general, couplers have 4 ports as shown in Figure 6.

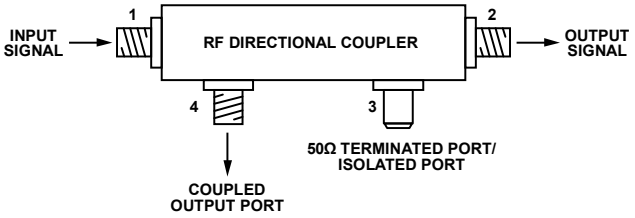


Figure 6. Directional Coupler

In the Figure 6 configuration, the input signal is coupled to Port 4, and Port 3 is terminated at 50 Ω for nonreflective coupling of the signal. If Port 4 is terminated in 50 Ω instead of Port 3, the reflected signal is coupled to Port 3.

In this circuit, instead of using the 50 Ω termination connected directly to the port as shown previously, both ports are fed to the RF switch inputs. Therefore, the coupler can be regarded as being bidirectional, because the 50 Ω termination is applied by the HCM547 internally to Port 3 or Port 4, depending on the state of the switch.

The RF coupler chosen for this circuit was the Marki Microwave C10-0226 stripline coupler. This coupler has 10 dB coupling, meaning that the coupled signal is 10 dB less than the input signal. A directional coupler with SMA connectors was used in this circuit to demonstrate operation over the widest possible frequency range. A surface-mount coupler can also be used; however, such devices generally have a narrower frequency range.

Data Analysis

The EVAL-SDP-CB1Z system demonstration platform (SDP) board is used in conjunction with evaluation software, to capture the data being sampled by the ADC.

The software calculates the return loss using Equation 8, which was derived previously. The reflection coefficient and VSWR are derived from this equation.

$$P_{F_{dBm}} - P_{R_{dBm}} = 10 \times \log\left(\frac{CODE_F^{\,2}}{CODE_R^{\,2}}\right) \quad (8)$$

Figure 7 shows the result display panel of the software GUI.

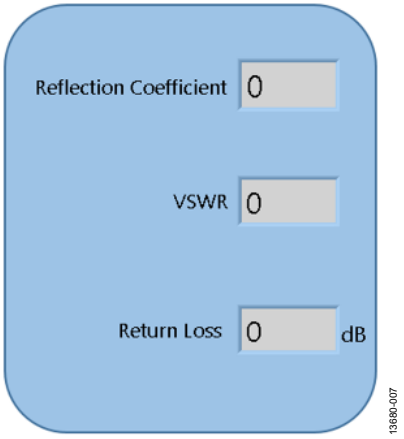


Figure 7. CN-0387 Evaluation Software Display

Detector Sampling Strategy

To accurately measure the return loss of the system, the forward and reverse voltages must be measured with a short time delay between the forward and reverse measurements. Figure 8 shows the sampling sequence performed when sampling continuously.

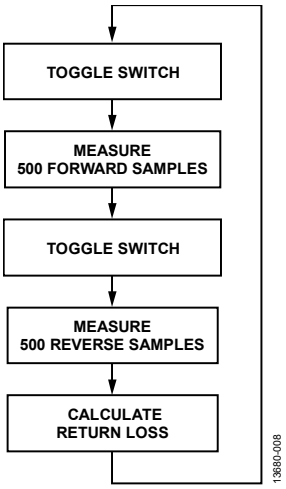


Figure 8. Sampling Sequence

When the RF switch receives the signal to toggle the switch, the switch position changes, and the forward or reverse coupled port signal is fed to the power detector. In the return loss calculation step, 500 forward samples and 500 reverse samples are averaged, and the return loss is calculated from the ratio of averaged forward and reverse voltages.

The ADC samples at a rate of 1 MSPS. Therefore, it takes 500 µs to measure 500 samples. Toggling the switch position using a general-purpose input/output (GPIO) of the SDP-B interface takes approximately 400 µs between forward and reverse cycles. The timing diagram is shown in Figure 9.

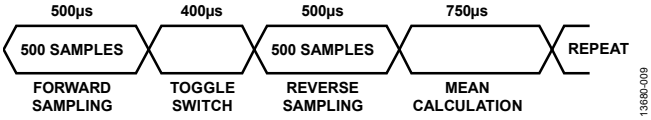


Figure 9. Timing Diagram Representation

The return loss, reflection coefficient, and VSWR are calculated using the resultant average of forward and reverse voltage measurements. To allow results to be clearly read before updating, 50 sample results are averaged before displaying on the GUI results panel.

Complete documentation for the EVAL-VSWR-SDZ board, including schematics, layouts, Gerber files, and bill of materials, is available for download in the CN-0387 Design Support Package at www.analog.com/CN0387-DesignSupport.

COMMON VARIATIONS

As previously noted, a wideband connectorized directional coupler was used in this circuit to enable operation over the widest possible frequency range. Surface-mount directional couplers or printed circuit directional couplers can also be used; however, these devices tend to have narrower frequency ranges.

Directional couplers with higher coupling factors can also be used, which tend to have lower insertion loss. However, it is recommended that the circuit be dimensioned to maximize measurement range. For example, if the maximum system power is +35 dBm, using a 20 dB directional coupler sets the maximum power to the detector at approximately +15 dBm, which is at the upper limit of the input range.

CIRCUIT EVALUATION AND TEST

Equipment Needed

The following equipment is needed to perform the evaluations described in this circuit note:

- The EV-VSWR-SDZ evaluation board.
- A suitably rated broadband RF Coupler. For this evaluation, the Marki Microwave C10-0226 was used. However, any coupler with suitable specifications and with a 3.5 mm SMA type connector can be used.
- The EVAL-SDP-CB1Z SDP-B board.
- A signal generator (with output frequency within the range of 500 MHz to 28 GHz).
- A suitable power supply unit with 6 V dc output voltage.
- The CN-0387 Evaluation Software, which can be downloaded from ftp://ftp.analog.com/pub/cftl/CN0387/.
- An SMA attenuator and 50 Ω termination.
- A PC running Windows® 7 connected to the SDP-B board via a USB cable (supplied with the EVAL-SDP-CB1Z).

Setup and Test

To set up and test the VSWR measurement system, set LK6 in Position B and put LK22 in place, and then take the following steps:

1. Turn on all test equipment and wait until all equipment boots up.
2. Connect the input and output coupled ports of the RF coupler to the RF1 and RF2 3.5 mm SMA connections of the evaluation board, respectively, using suitably rated RF cables.
3. Connect the coupler input port to the 50 Ω output of the signal generator.
4. Connect the output of the coupler to a 50 Ω termination or a suitably rated RF attenuator termination.
5. Connect the EVAL-SDP-CB1Z SDP interface board to the EV-VSWR-SDZ evaluation board.
6. Connect the SDP interface board to a PC via the USB cable provided.
7. Connect the power supply from the dc supply to the power and ground of the banana sockets of the evaluation board.
8. Download and install the CN-0387 Evaluation Software onto the PC that is connected to the SDP-B control board.
9. After the software is installed properly, run the executable.
10. Set the output frequency of the signal generator to 2 GHz and set the power level to 15 dBm output. Then turn on the output of the signal generator.
11. In the software display, select **Continuous**, and then click **Capture**. The software continuously repeats measurements; when each measurement is gathered, the GUI display updates with the value of the return loss and the corresponding values of VSWR and reflection coefficient.

Functional Block Diagram of Test Setup

Figure 10 shows the functional block diagram of the test setup.

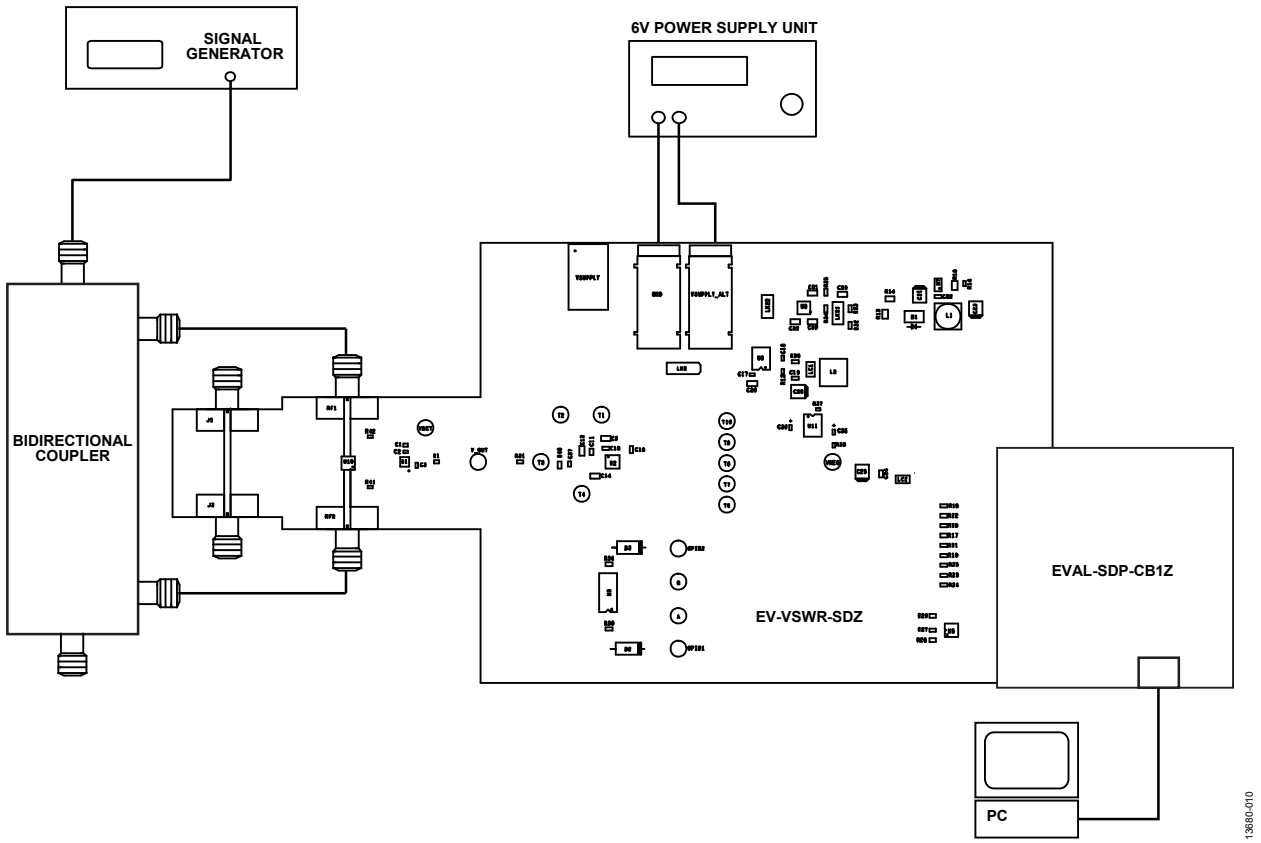


Figure 10. Functional Block Diagram of Test Setup

Test Results

Measurements were gathered manually by adjusting the RF input power levels. Return loss in different output configurations was measured over the power range of the ADL6010.

RF simulations were also run using the Keysight Advanced Design System (ADS). This software is an electronic design simulation tool for RF and microwave applications. Simulations were performed to verify that RF input trace insertion loss and reflection were within certain limits and to simulate the performance of the directional coupler.

The Marki Microwave C10-0226 directional coupler was provided with a simulation model file, an .s4p file. This file contains information that describes the S-parameters of the coupler and can be readily used in ADS within a simulation. Simulations were performed over a frequency range from dc up to the upper frequency limit of the coupler of 26.5 GHz, and the input power was set to 0 dBm for each simulation.

Return Loss Measurement

While testing the EV-VSWR-SDZ evaluation board, a 9 dB attenuator termination was connected to the coupler output to verify that the expected attenuation levels were measured at a chosen frequency as compared to the simulated results.

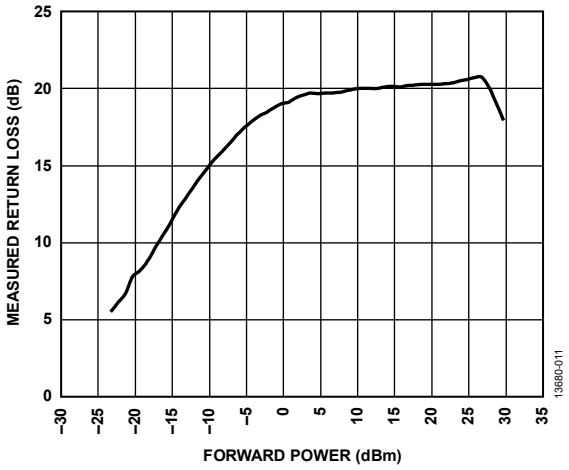


Figure 11. Return Loss Measurement

As shown in Figure 11, within the input power range of 0 dBm to 25 dBm, the return loss measured remains nearly constant at 20 dB. This value is the summation of the forward and reverse attenuations as previously outlined (9 dB + 9 dB), and the forward insertion loss of the coupler at 2 GHz using the Marki Microwave C10-0226. After the input power at the forward coupled port reaches approximately 27 dBm, the return loss reduces significantly. This reduction occurs because the coupled power at the forward coupled port is close to +15 dBm (with 10 dB coupling), which is the upper power limit of the ADL6010. As input power is reduced, the measured return loss begins to reduce due to the reflected power at the reverse coupled port dropping below the lower limit of –30 dBm. Figure 11 illustrates the power range over which the ADL6010 can operate to measure a return loss of 20 dB.

Power Detector Measured Power

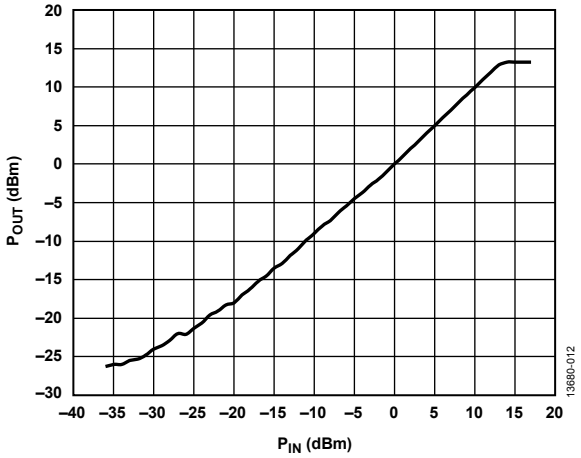


Figure 12. Input Power vs. Measured Coupled Output Power

Figure 12 shows how the measured power changes with input power. A calibration routine was performed at 2 GHz to obtain accurate power measurement at the forward coupled port, at each power level. As the input power rises, the measured power reaches the detector limit of 15 dBm. Similarly, as input power is reduced, the lower limit of the detector is reached and measurement accuracy reduces.

Open Circuit Configuration

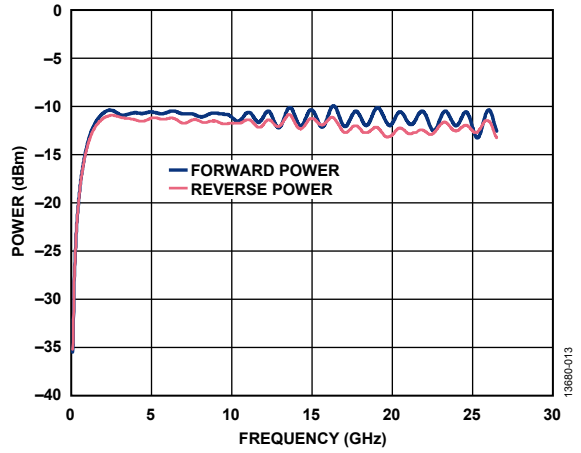


Figure 13. Coupler Forward and Reverse Power vs. Frequency—Open Circuit

Figure 13 shows that the return loss is close to 0 dB as forward and reverse power levels are close in value, compared to the previous 50 Ω termination case.

This open-circuit simulation shows how the majority of the signal is reflected back through the coupler in the opposite direction to the forward wave. The difference in amplitude between the forward and reflected waves is a result of the insertion loss of the coupler across the frequency range. This graph highlights that exact return loss and VSWR measurements vary with the coupler used, due to non-ideal coupler impedance matching across frequency.

Additionally, a threshold return loss can be set to indicate whether there is a mismatch occurring in the system, which is much greater than the coupler return loss.

50 Ω Output Termination Circuit Configuration

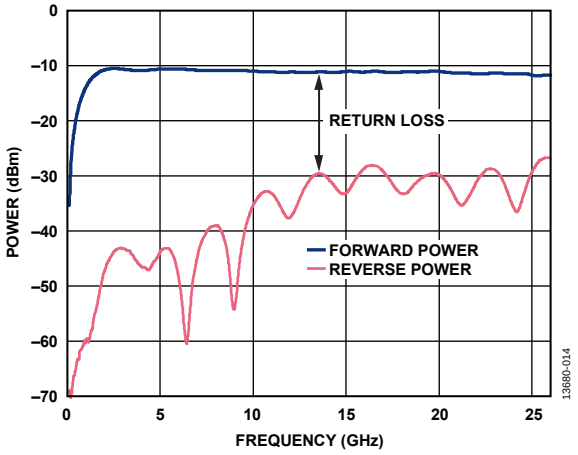


Figure 14. Coupler Forward and Reverse Power vs. Frequency—50 Ω Termination

Figure 14 shows the Marki Microwave C10-0226 RF coupler forward insertion loss and reflected signal for a 50 Ω terminated output with a 0 dBm power level applied to the forward port of the coupler. The coupler is specified to operate from 2 GHz to 26.5 GHz. Therefore, the coupler begins to operate as expected beyond 2 GHz in Figure 14. The simulation uses an ideally matched transmission line of 50 Ω output impedance on the coupler. The return loss at any frequency is the difference between the forward and reverse power. The graph shows that return loss varies with frequency. However, within this frequency range, the return loss is close to 20 dB, which is acceptable because return loss values greater than 20 dB are taken to be negligible.

3 dB Output Attenuator Circuit Configuration

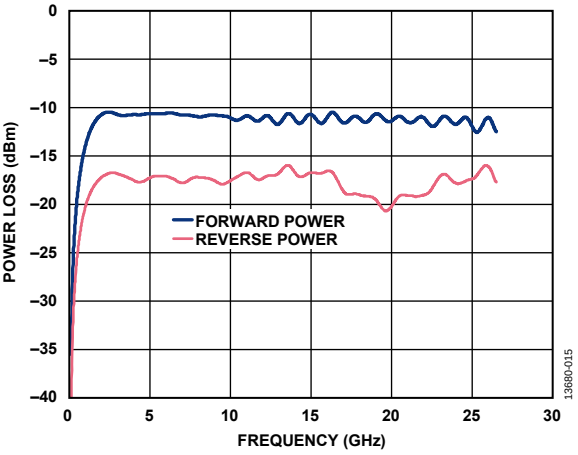


Figure 15. Coupler Forward and Reverse Power vs. Frequency—3 dB Attenuator

In Figure 15, the return loss is relatively stable at 6 dB until up to approximately 15 GHz, after which the loss of the coupler increases and the attenuation increases.

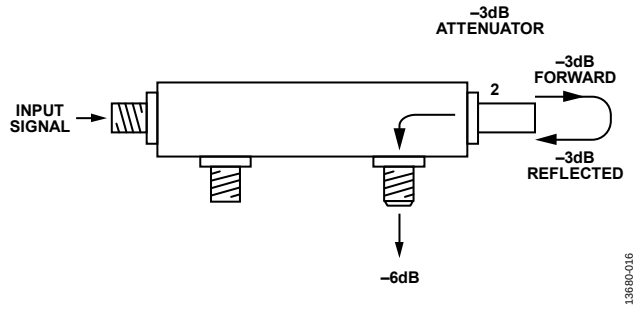


Figure 16. Coupler with 6 dB Attenuation

The 6 dB attenuation is due to the 3 dB coupler attenuating both the incident signal and reflected signal by 3 dB. As shown in Figure 16, the signal first attenuates by 3 dB in the forward direction before being reflected and attenuated by a further 3 dB. The measured reflected signal is the result of the accumulated forward and reverse attenuations.

Calibration Structure Trace Insertion Loss

The RF trace insertion loss was simulated using the layout file of the EV-VSWR-SDZ evaluation board. This layout file was imported into the ADS tool to run a simulation, to determine the losses of the RF traces on the board.

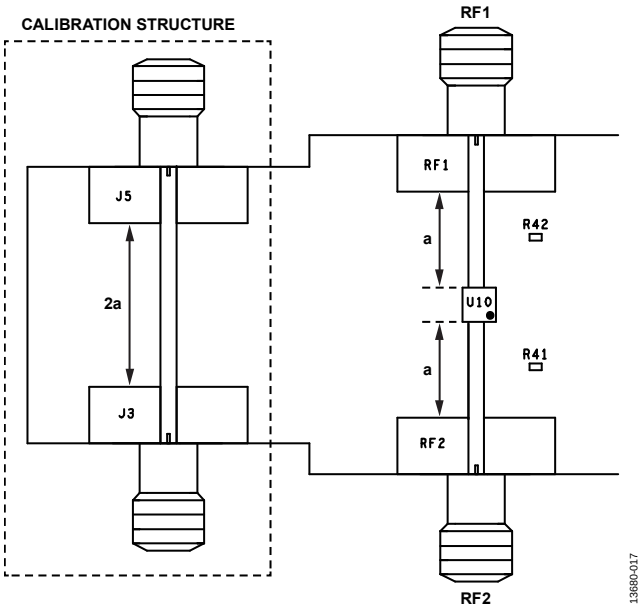


Figure 17. Calibration Structure

The calibration structure shown in Figure 17 on the board section was used in the simulation. This structure was included in the board design to measure the losses from the SMA connector to the switch (Distance A). As shown, the length of the calibration structure is exactly twice the distance from RF1/RF2 to the HMC547 switch (U10). To measure these RF trace losses at a particular frequency, the signal is applied to one of the calibration structure connectors and is then measured on the opposite connector.

The ADS simulation tool was run on this structure from dc to 26.5 GHz to simulate the insertion loss of the RF traces.

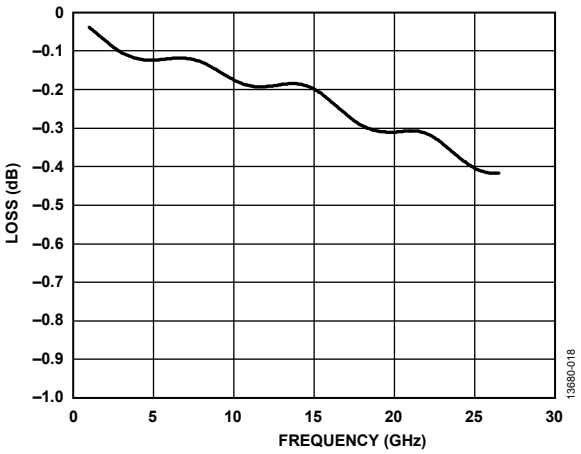


Figure 18. Calibration Structure Loss—Frequency vs. Power

As shown in Figure 18, the insertion loss of the calibration structure reaches a maximum attenuation of approximately −0.4 dB at a frequency of 26.5 GHz.

This insertion loss is considered to be within the acceptable limits for the evaluation board. If this insertion loss is significant, it limits the range of measurement.

A photograph of the EV-VSWR-SDZ board connected to the EVAL-SDP-CB1Z board is shown in Figure 19.

An electrically equivalent replacement part for the HMC547LC3 will be available in June 2016.

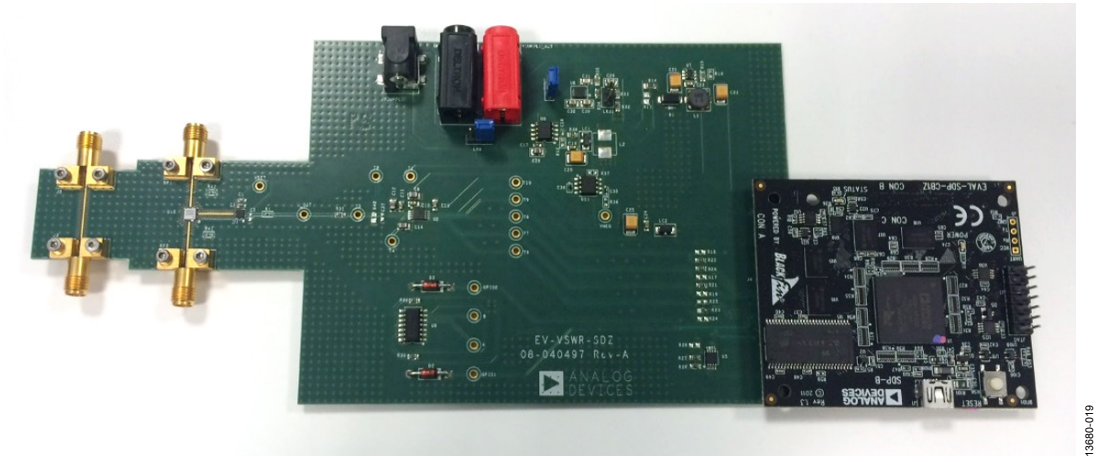


Figure 19. EV-VSWR-SDZ Board Connected to EVAL-SDP-CB1Z Board

LEARN MORE

CN-0387 Design Support Package: www.analog.com/CN0387-DesignSupport

EVAl-SDP-CB1Z System Demonstration Platform User Guide (UG-277)

EVAL-AD7091RSDZ Evaluation Board User Guide (UG-409)

ADIsimRF Design Tool

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*. Analog Dialogue 39-09, September 2005.

Circuit Note CN-0366. *A 40 GHz Microwave Power Meter with a Range from −30 dBm to +15 dBm*. Analog Devices.

Circuit Note CN-0178. *Software-Calibrated, 50 MHz to 9 GHz, RF Power Measurement System*. Analog Devices.

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND."* Analog Devices.

MT-073 Tutorial. *High Speed Variable Gain Amplifiers (VGAs)*. Analog Devices.

MT-101 Tutorial. *Decoupling Techniques*. Analog Devices.

Data Sheets and Evaluation Boards

HMC547LC3 Data Sheet and Evaluation Board

ADL6010 Data Sheet and Evaluation Board

AD7091R Data Sheet and Evaluation Board

REVISION HISTORY

10/15—Rev. 0 to Rev. A

Changes to Setup and Test Section 5

10/15—Revision 0: Initial Version

CN13680-0-10/15(A)

NOTES