



PSMN4R0-25YLC

N-channel 25 V 4.5 mΩ logic level MOSFET in LPAK

Rev. 01 — 2 December 2010

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising Superjunction technology
- Ultra low QG, QGD & QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

1.4 Quick reference data

Table 1. Quick reference data

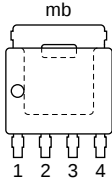
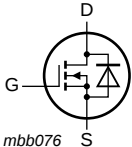
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	25	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	-	-	84	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	61	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; see Figure 12	-	4.5	5.8	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; see Figure 12	-	3.5	4.5	mΩ

Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 20\text{ A}$; $V_{DS} = 12\text{ V}$; see Figure 14 ; see Figure 15	-	3.5	-	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$; $I_D = 20\text{ A}$; $V_{DS} = 12\text{ V}$; see Figure 14 ; see Figure 15	-	10.9	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT669 (LPAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R0-25YLC	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	-	84	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	60	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 4	-	336	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	61	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
V_{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	200	-	V
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	55	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	336	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 84\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped; see Figure 3	-	17.4	mJ

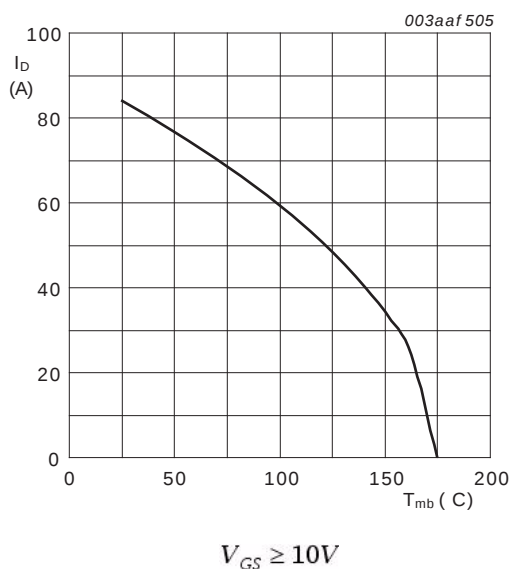


Fig 1. Continuous drain current as function of mounting base temperature

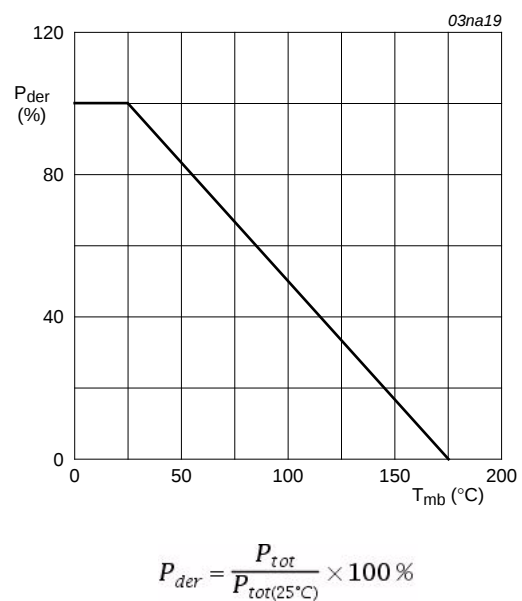


Fig 2. Normalized total power dissipation as a function of mounting base temperature

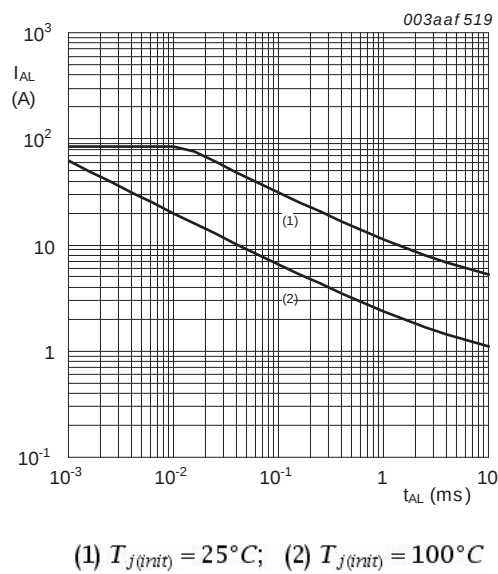


Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

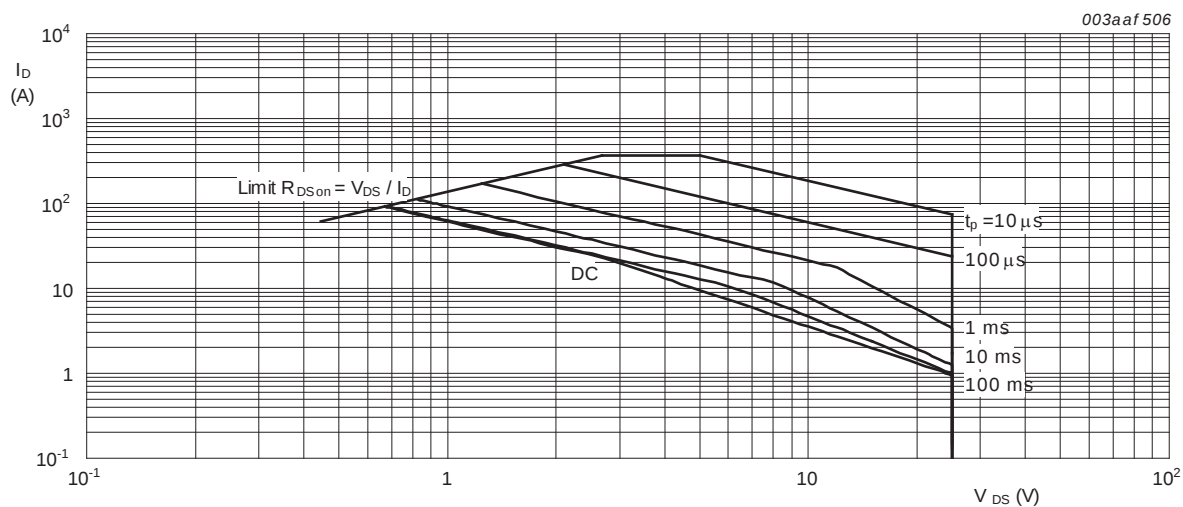


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	1.4	2.4	K/W

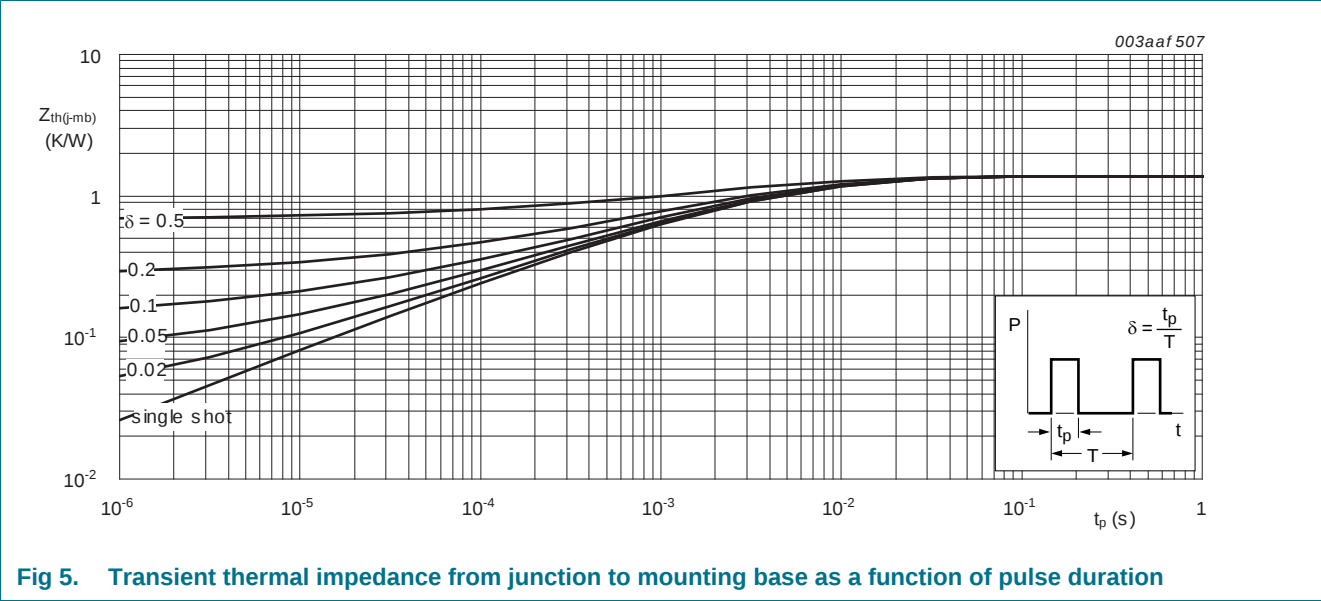


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_J = 25\ ^\circ C$	25	-	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_J = -55\ ^\circ C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_J = 25\ ^\circ C$; see Figure 10	1.05	1.53	1.95	V
		$I_D = 10\ mA$; $V_{DS} = V_{GS}$; $T_J = 150\ ^\circ C$; see Figure 11	0.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_J = -55\ ^\circ C$; see Figure 11	-	-	2.25	V
I_{DSS}	drain leakage current	$V_{DS} = 25\ V$; $V_{GS} = 0\ V$; $T_J = 25\ ^\circ C$	-	-	1	μA
		$V_{DS} = 25\ V$; $V_{GS} = 0\ V$; $T_J = 150\ ^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ V$; $V_{DS} = 0\ V$; $T_J = 25\ ^\circ C$	-	-	100	nA
		$V_{GS} = -16\ V$; $V_{DS} = 0\ V$; $T_J = 25\ ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ V$; $I_D = 20\ A$; $T_J = 25\ ^\circ C$; see Figure 12	-	4.5	5.8	mΩ
		$V_{GS} = 4.5\ V$; $I_D = 20\ A$; $T_J = 150\ ^\circ C$; see Figure 12 ; see Figure 13	-	-	9.85	mΩ
		$V_{GS} = 10\ V$; $I_D = 20\ A$; $T_J = 25\ ^\circ C$; see Figure 12	-	3.5	4.5	mΩ
		$V_{GS} = 10\ V$; $I_D = 20\ A$; $T_J = 150\ ^\circ C$; see Figure 12 ; see Figure 13	-	-	7.65	mΩ
R_G	internal gate resistance (AC)	$f = 1\ MHz$	-	2.1	4.2	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 20\ A$; $V_{DS} = 12\ V$; $V_{GS} = 10\ V$; see Figure 14 ; see Figure 15	-	22.8	-	nC
		$I_D = 0\ A$; $V_{DS} = 0\ V$; $V_{GS} = 10\ V$; see Figure 14	-	21.1	-	nC
		$I_D = 20\ A$; $V_{DS} = 12\ V$; $V_{GS} = 4.5\ V$; see Figure 14 ; see Figure 15	-	10.9	-	nC
Q_{GS}	gate-source charge		-	3.3	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	2.25	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.05	-	nC
Q_{GD}	gate-drain charge	$I_D = 20\ A$; $V_{DS} = 12\ V$; $V_{GS} = 4.5\ V$; see Figure 14 ; see Figure 15	-	3.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 12\ V$; see Figure 14 ; see Figure 15	-	2.58	-	V
C_{iss}	input capacitance	$V_{DS} = 12\ V$; $V_{GS} = 0\ V$; $f = 1\ MHz$; $T_J = 25\ ^\circ C$; see Figure 16	-	1407	-	pF
C_{oss}	output capacitance		-	354	-	pF
C_{rss}	reverse transfer capacitance		-	119	-	pF

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.5\text{ }\Omega; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 4.7\text{ }\Omega$	-	15.9	-	ns
t_r	rise time		-	17.5	-	ns
$t_{d(off)}$	turn-off delay time		-	24	-	ns
t_f	fall time		-	9.9	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 12\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C}$	-	7.32	-	nC

Source-drain diode

V_{SD}	source-drain voltage	$I_S = 20\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see Figure 17	-	0.8	1.1	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 12\text{ V}$	-	24.5	-	ns
Q_r	recovered charge		-	16.1	-	nC
t_a	reverse recovery rise time	$V_{GS} = 0\text{ V}; I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s};$ $V_{DS} = 12\text{ V};$ see Figure 18	-	14.9	-	ns
t_b	reverse recovery fall time		-	9.6	-	ns

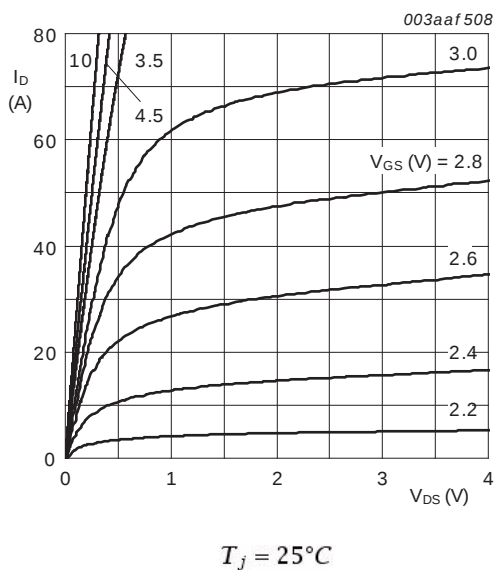


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

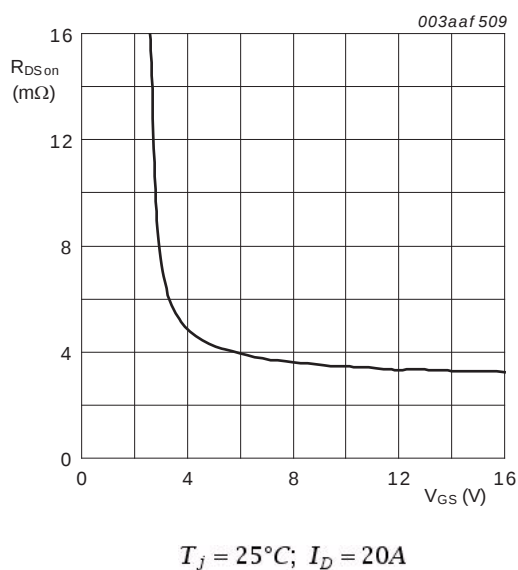
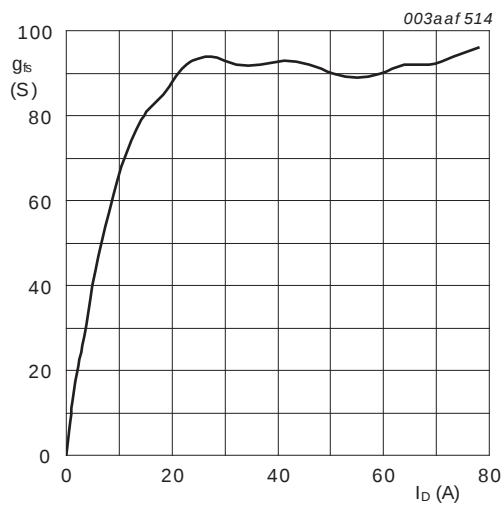
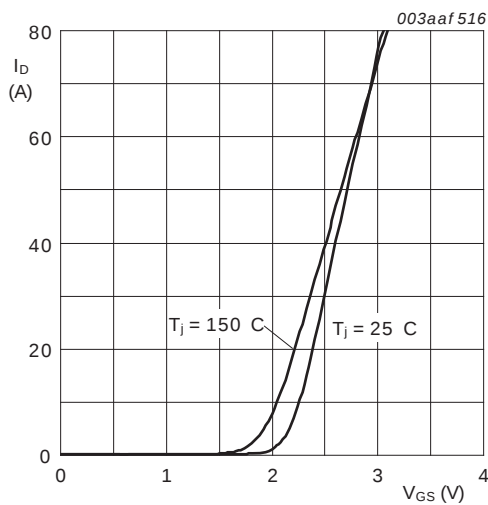


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



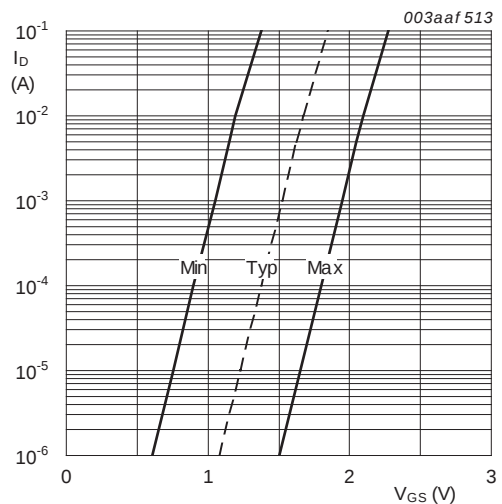
$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$

Fig 8. Forward transconductance as a function of drain current; typical values



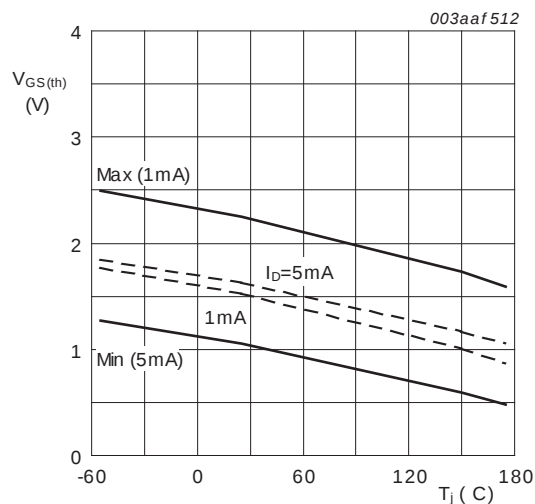
$V_{DS} = 10\text{V}$

Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature

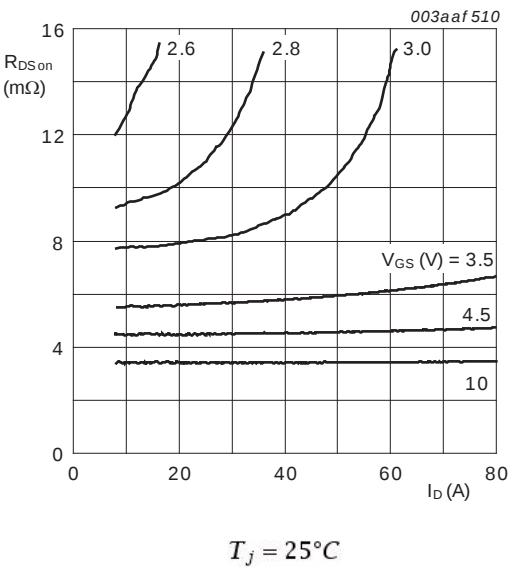


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

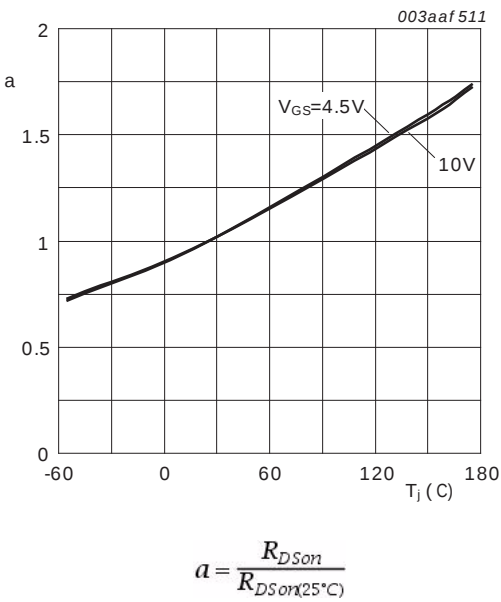


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

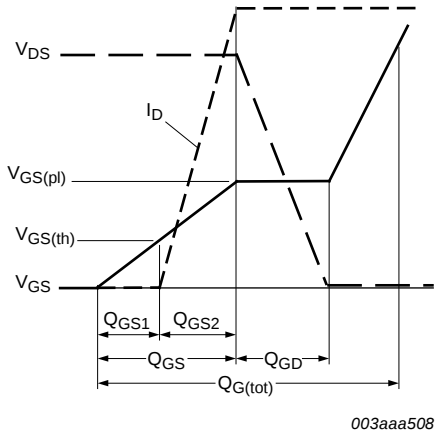


Fig 14. Gate charge waveform definitions

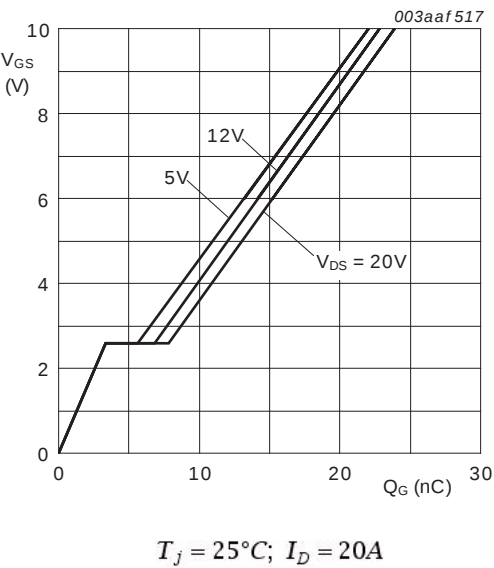


Fig 15. Gate-source voltage as a function of gate charge; typical values

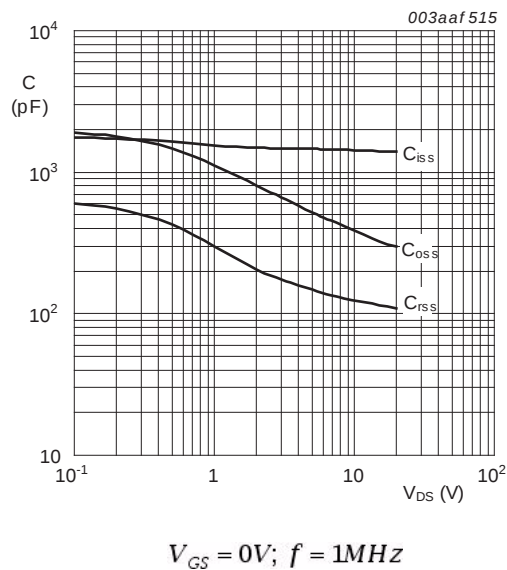


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

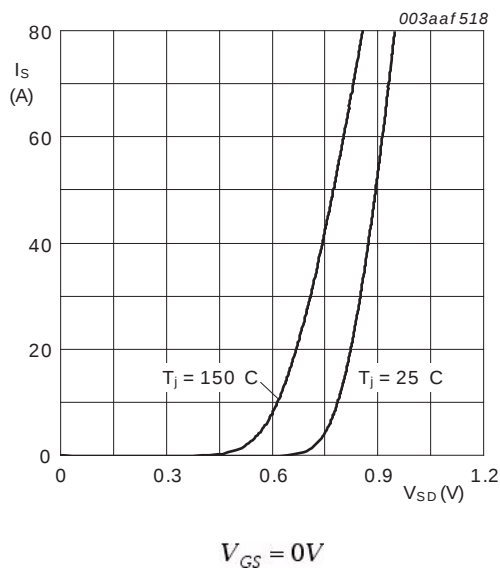


Fig 17. Source current as a function of source-drain voltage; typical values

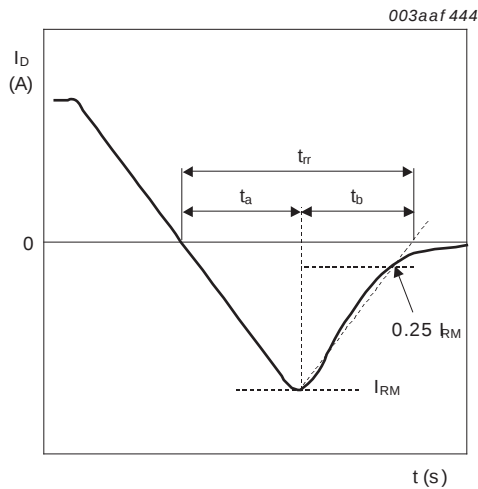


Fig 18. Reverse recovery timing definition

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

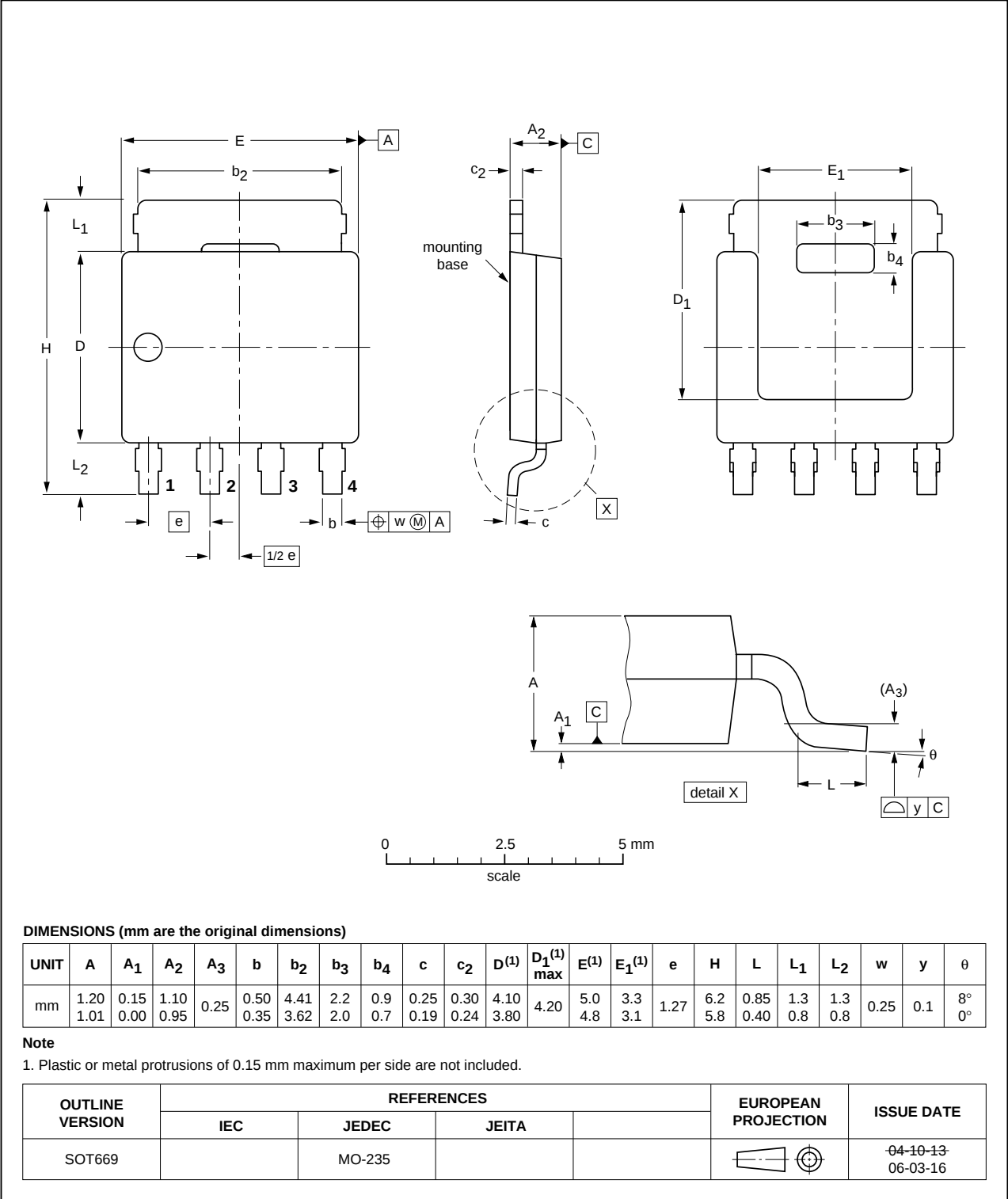


Fig 19. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN4R0-25YLC v.1	20101202	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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