

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ C7

650V CoolMOS™ C7 Power Transistor
IPA65R225C7

Data Sheet

Rev. 2.0
Final

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The product portfolio provides all benefits of fast switching superjunction MOSFETs offering better efficiency, reduced gate charge, easy implementation and outstanding reliability.



Features

- Increased MOSFET dv/dt ruggedness
- Better efficiency due to best in class FOM $R_{DS(on)} \cdot E_{oss}$ and $R_{DS(on)} \cdot Q_g$
- Best in class $R_{DS(on)}$ /package
- Easy to use/drive
- Pb-free plating, halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Benefits

- Enabling higher system efficiency
- Enabling higher frequency / increased power density solutions
- System cost / size savings due to reduced cooling requirements
- Higher system reliability due to lower operating temperatures

Applications

PFC stages and hard switching PWM stages for e.g. Computing, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

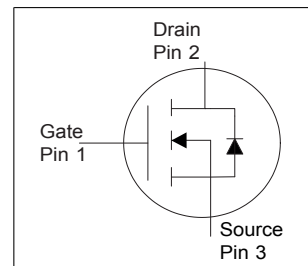


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	225	mΩ
$Q_{g,typ}$	20	nC
$I_{D,pulse}$	41	A
$E_{oss@400V}$	2.3	μJ
Body diode di/dt	55	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPA65R225C7	PG-TO 220 FullPAK	65C7225	see Appendix A

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	7	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	41	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	48	mJ	$I_D=4.8\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.24	mJ	$I_D=4.8\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	4.8	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	29	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	7	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	41	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	1	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	55	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$.

³⁾ Identical low side and high side switch with identical R_G .

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.38	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

4 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$, $I_D=0.24mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=650$, $V_{GS}=0V$, $T_j=25^\circ\text{C}$ $V_{DS}=650$, $V_{GS}=0V$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.199 0.478	0.225 -	Ω	$V_{GS}=10V$, $I_D=4.8A$, $T_j=25^\circ\text{C}$ $V_{GS}=10V$, $I_D=4.8A$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	1.2	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	996	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Output capacitance	C_{oss}	-	14	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	29	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	313	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	9	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=4.8A$, $R_G=10\Omega$; see table 9
Rise time	t_r	-	6	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=4.8A$, $R_G=10\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	48	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=4.8A$, $R_G=10\Omega$; see table 9
Fall time	t_f	-	10	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=4.8A$, $R_G=10\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5	-	nC	$V_{DD}=400V$, $I_D=4.8A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	6	-	nC	$V_{DD}=400V$, $I_D=4.8A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	20	-	nC	$V_{DD}=400V$, $I_D=4.8A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=400V$, $I_D=4.8A$, $V_{GS}=0$ to $10V$

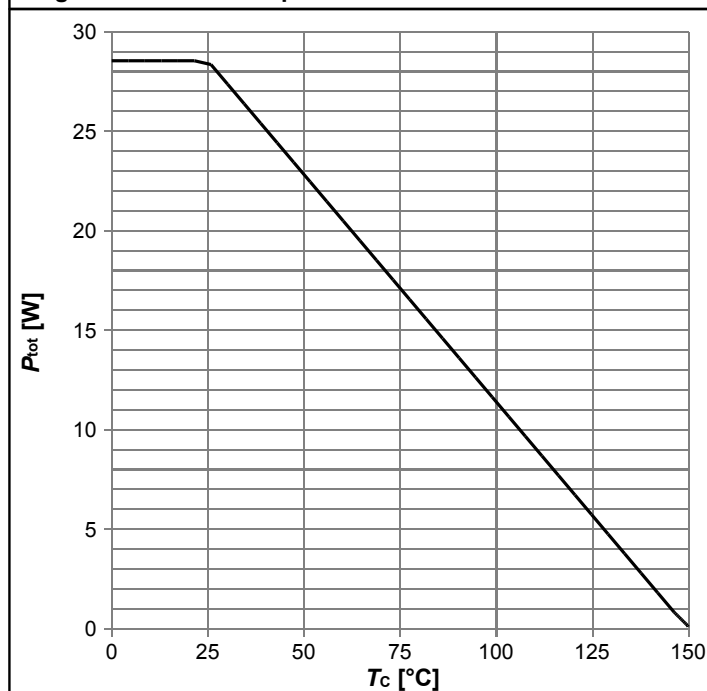
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

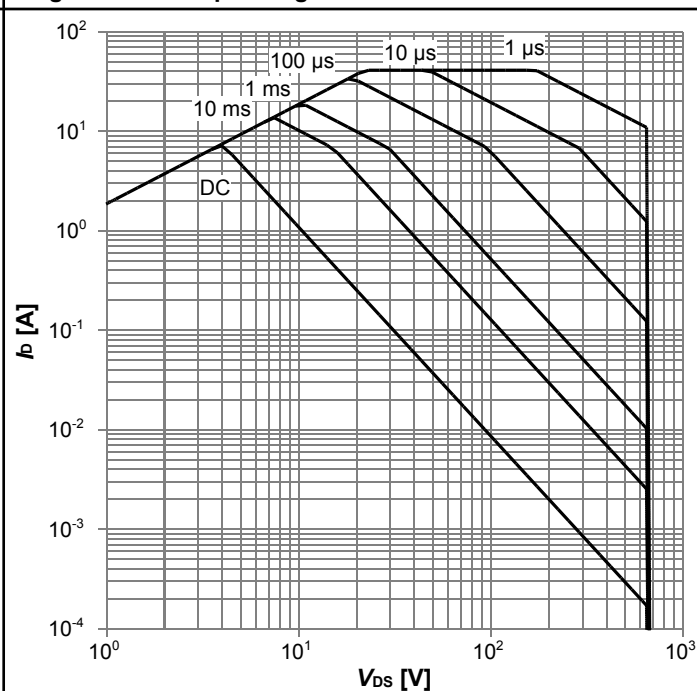
Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V$, $I_F=4.8A$, $T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	890	-	ns	$V_R=400V$, $I_F=7A$, $di_F/dt=55A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	6	-	μC	$V_R=400V$, $I_F=7A$, $di_F/dt=55A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	16	-	A	$V_R=400V$, $I_F=7A$, $di_F/dt=55A/\mu s$; see table 8

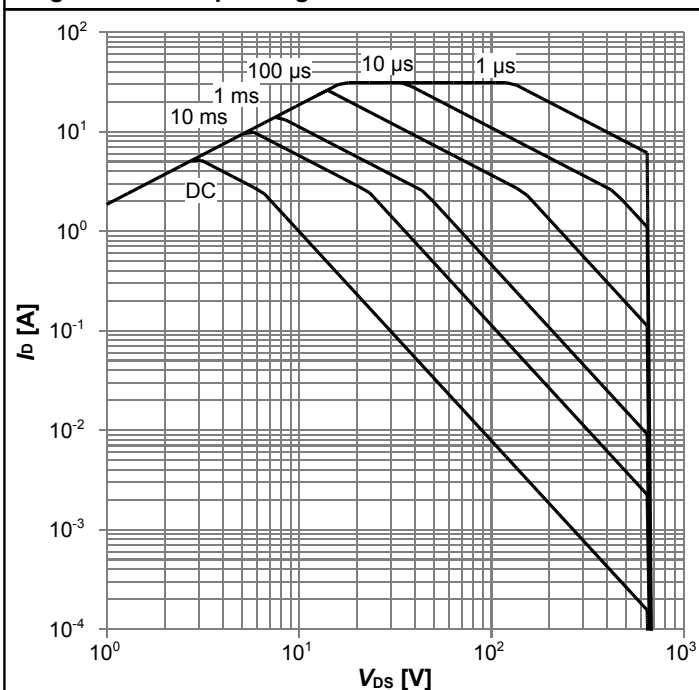
5 Electrical characteristics diagrams

Diagram 1: Power dissipation


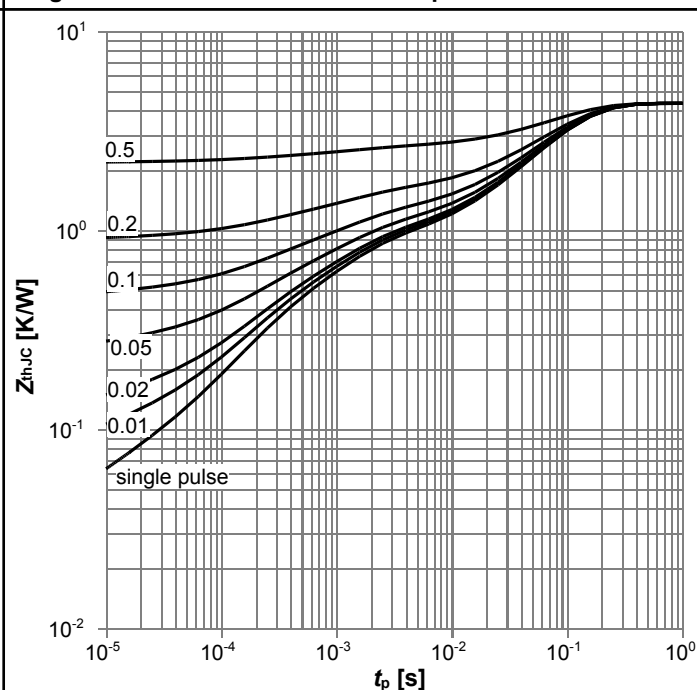
$$P_{\text{tot}} = f(T_c)$$

Diagram 2: Safe operating area


$$I_D = f(V_{DS}); T_c = 25\text{ °C}; D = 0; \text{ parameter: } t_p$$

Diagram 3: Safe operating area


$$I_D = f(V_{DS}); T_c = 80\text{ °C}; D = 0; \text{ parameter: } t_p$$

Diagram 4: Max. transient thermal impedance


$$Z_{thJC} = f(t_p); \text{ parameter: } D = t_p / T$$

Diagram 5: Typ. output characteristics

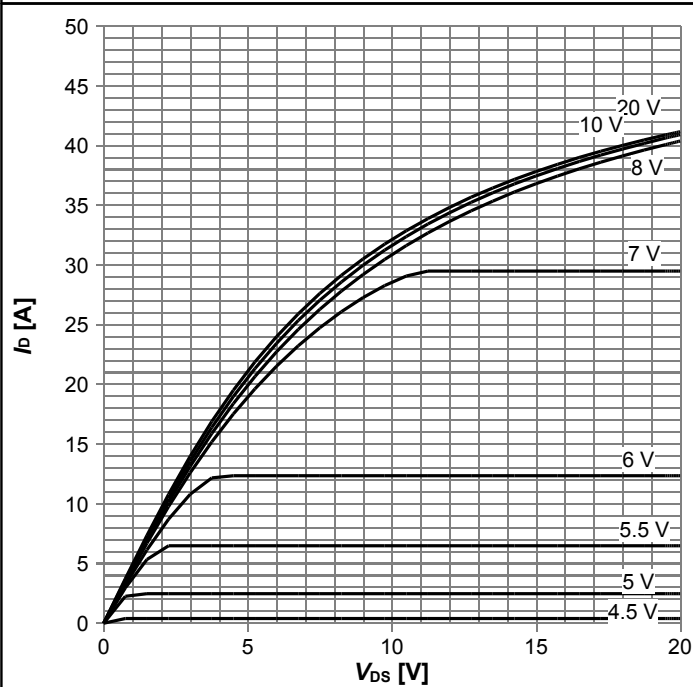

 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. output characteristics

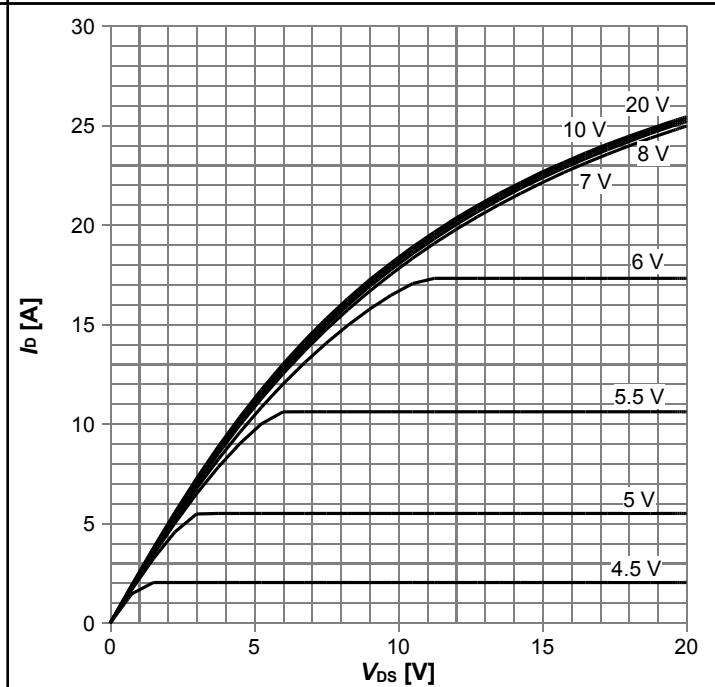

 $I_D = f(V_{DS}); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. drain-source on-state resistance

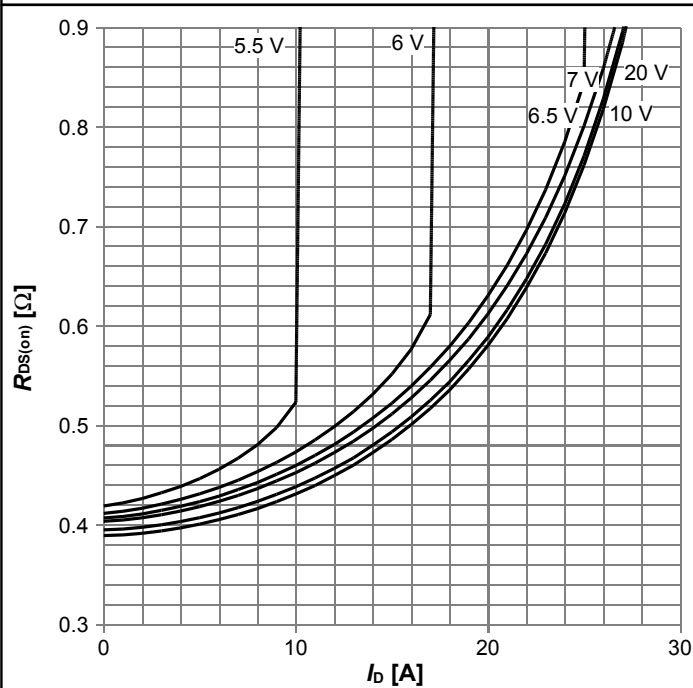

 $R_{DS(on)} = f(I_D); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 8: Drain-source on-state resistance

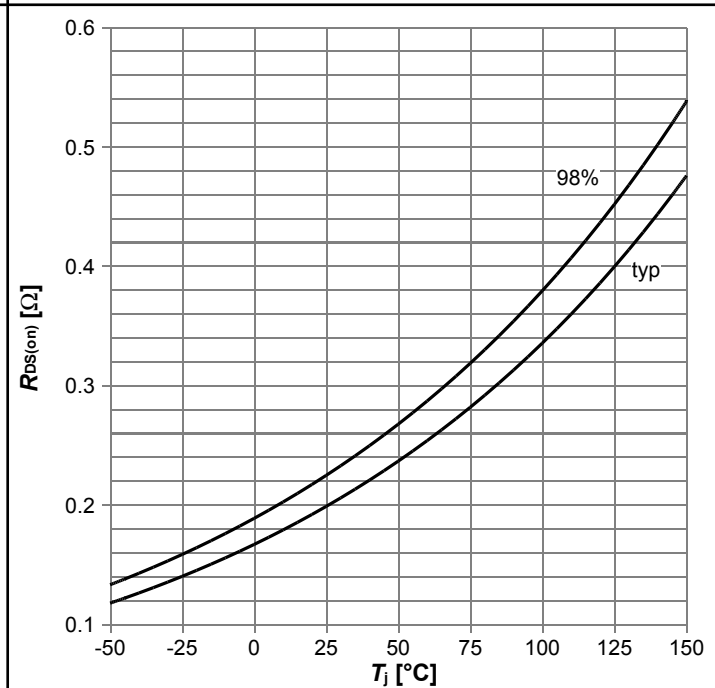

 $R_{DS(on)} = f(T_J); I_D = 4.8\text{ A}; V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics

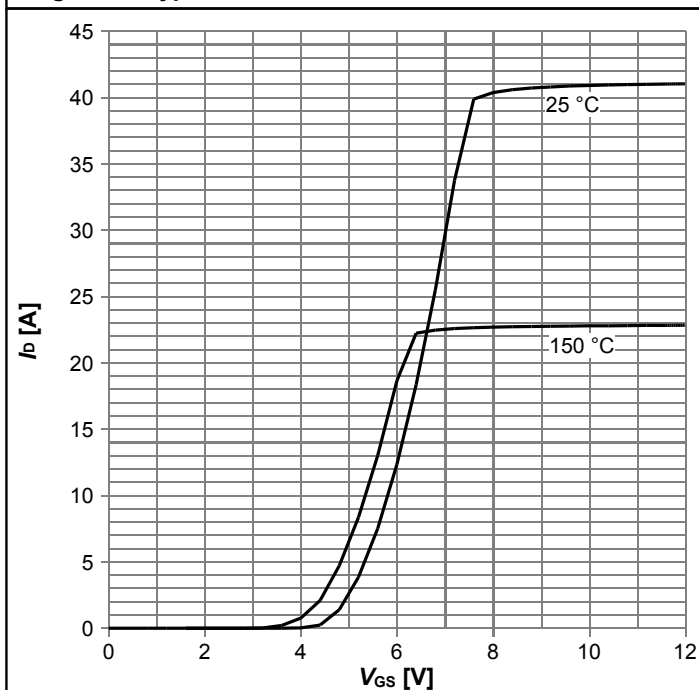

 $I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge

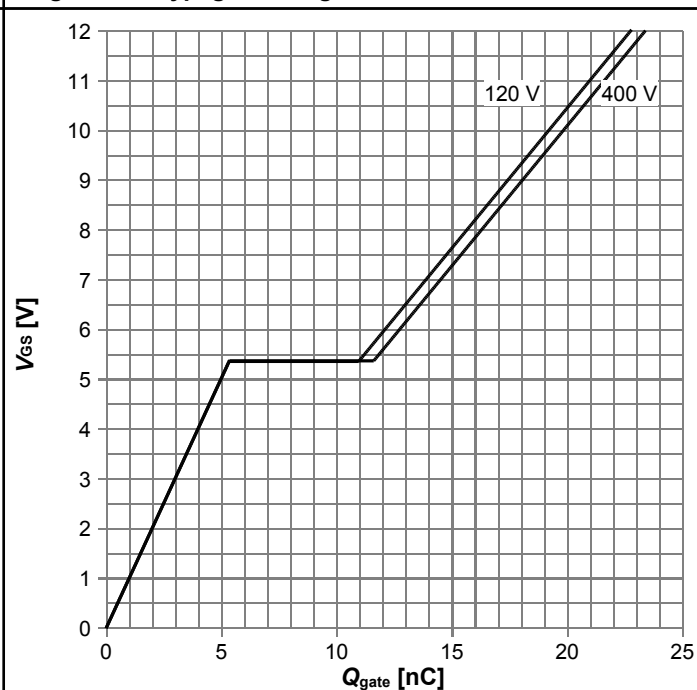

 $V_{GS} = f(Q_{gate}); I_D = 4.8 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode

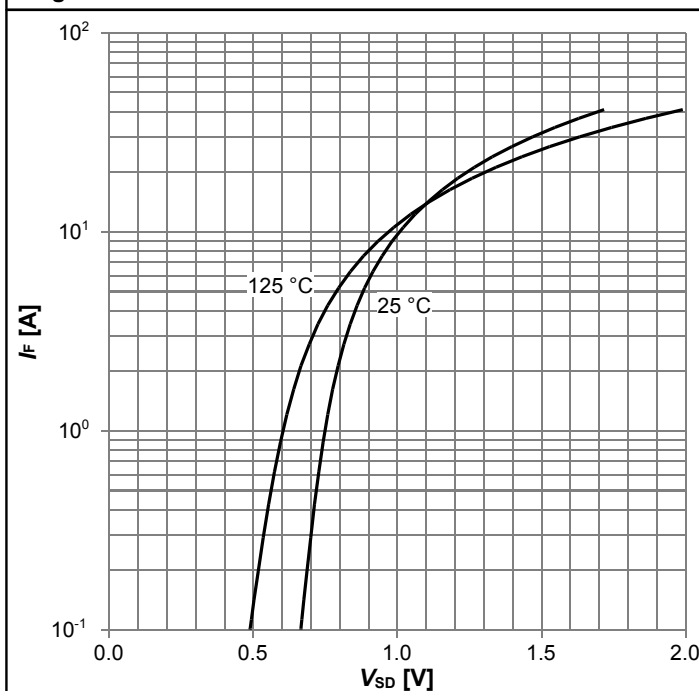

 $I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy

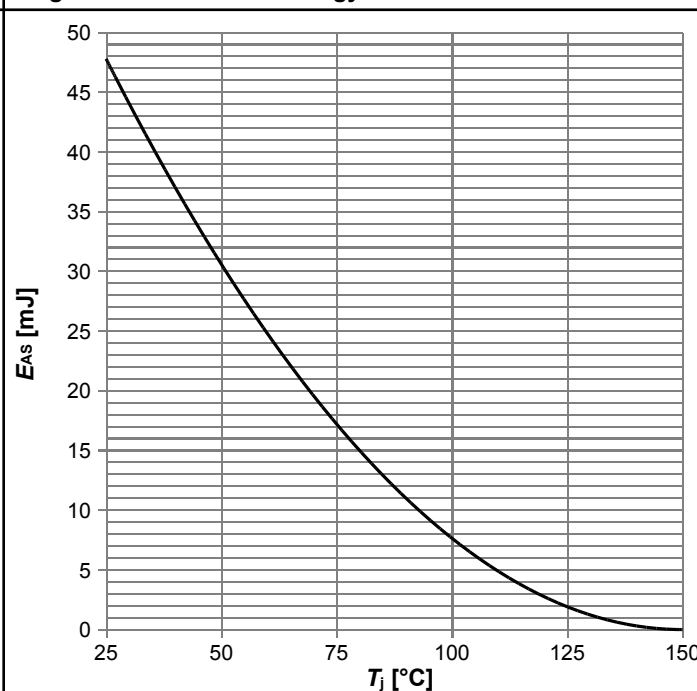
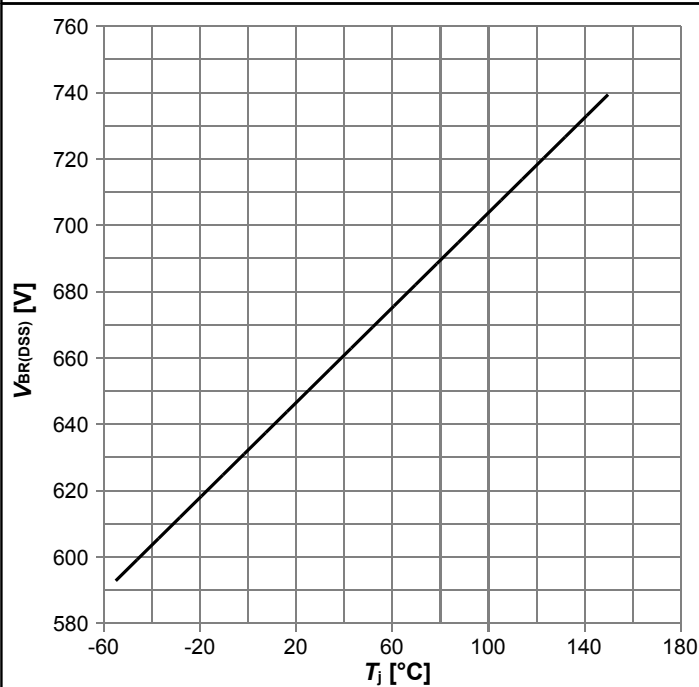
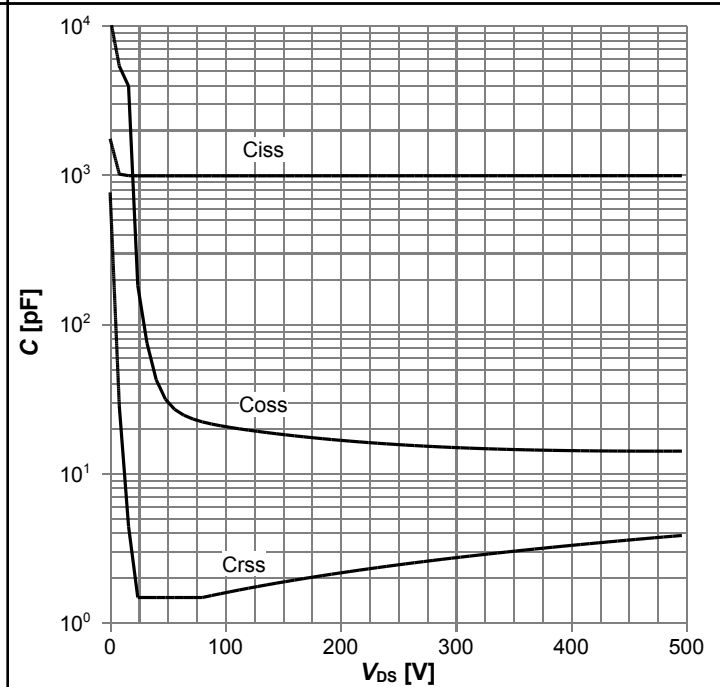

 $E_{AS} = f(T_j); I_D = 4.8 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



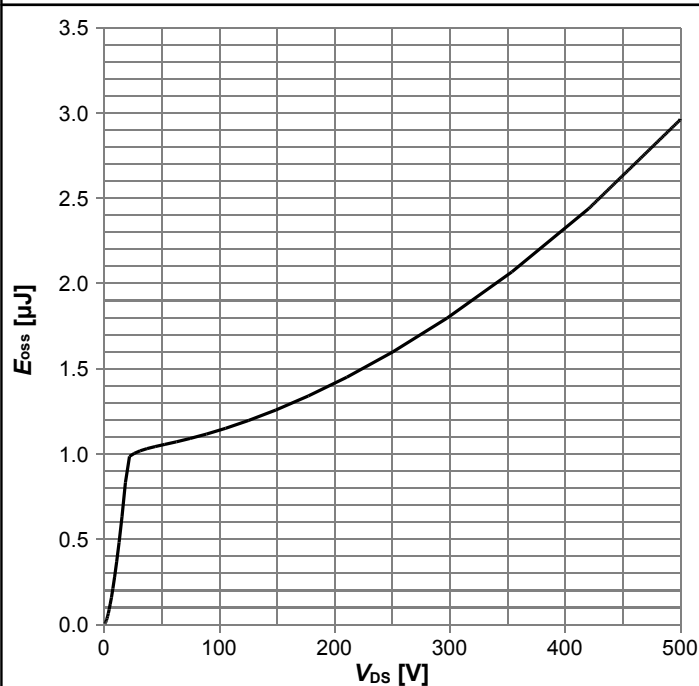
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

Diagram 14: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$$

Diagram 15: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

6 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics

$R_{g1} = R_{g2}$

Diode recovery waveform

$t_{rr} = t_F + t_S$
 $Q_{rr} = Q_F + Q_S$

Table 9 Switching times

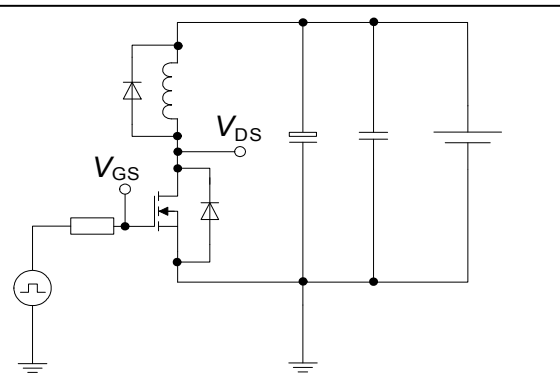
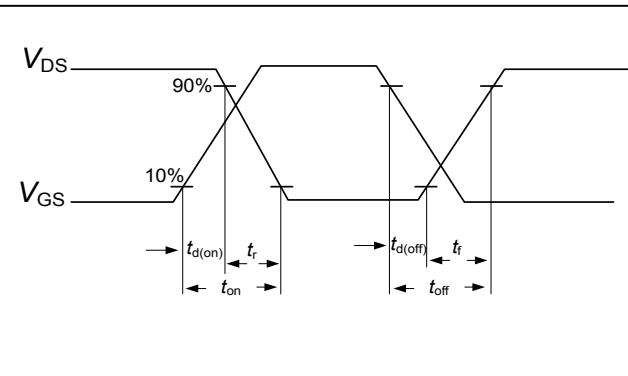
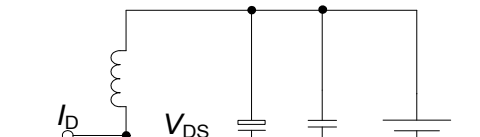
Switching times test circuit for inductive load	Switching times waveform
 The circuit diagram illustrates a MOSFET switching an inductive load. A pulse generator is connected to the gate of the MOSFET through a resistor. The drain of the MOSFET is connected to a load consisting of an inductor and a diode in parallel, which is then connected to a DC source. The drain voltage V_{DS} is measured across the load. The MOSFET's body diode is also shown.	 The waveform diagram shows the switching transitions for the MOSFET. The top trace is the drain voltage V_{DS} and the bottom trace is the gate voltage V_{GS}. The transitions are marked at 10% and 90% voltage levels. The timing parameters are defined as follows: $t_{d(on)}$: Delay time from the 10% V_{GS} level to the 90% V_{DS} level during turn-on. t_r: Rise time from the 90% V_{DS} level to the steady-state high level during turn-on. t_{on}: Total turn-on time from the 10% V_{GS} level to the steady-state high V_{DS} level. $t_{d(off)}$: Delay time from the 90% V_{DS} level to the 10% V_{GS} level during turn-off. t_f: Fall time from the 90% V_{DS} level to the steady-state low level during turn-off. t_{off}: Total turn-off time from the 90% V_{DS} level to the 10% V_{GS} level.

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines

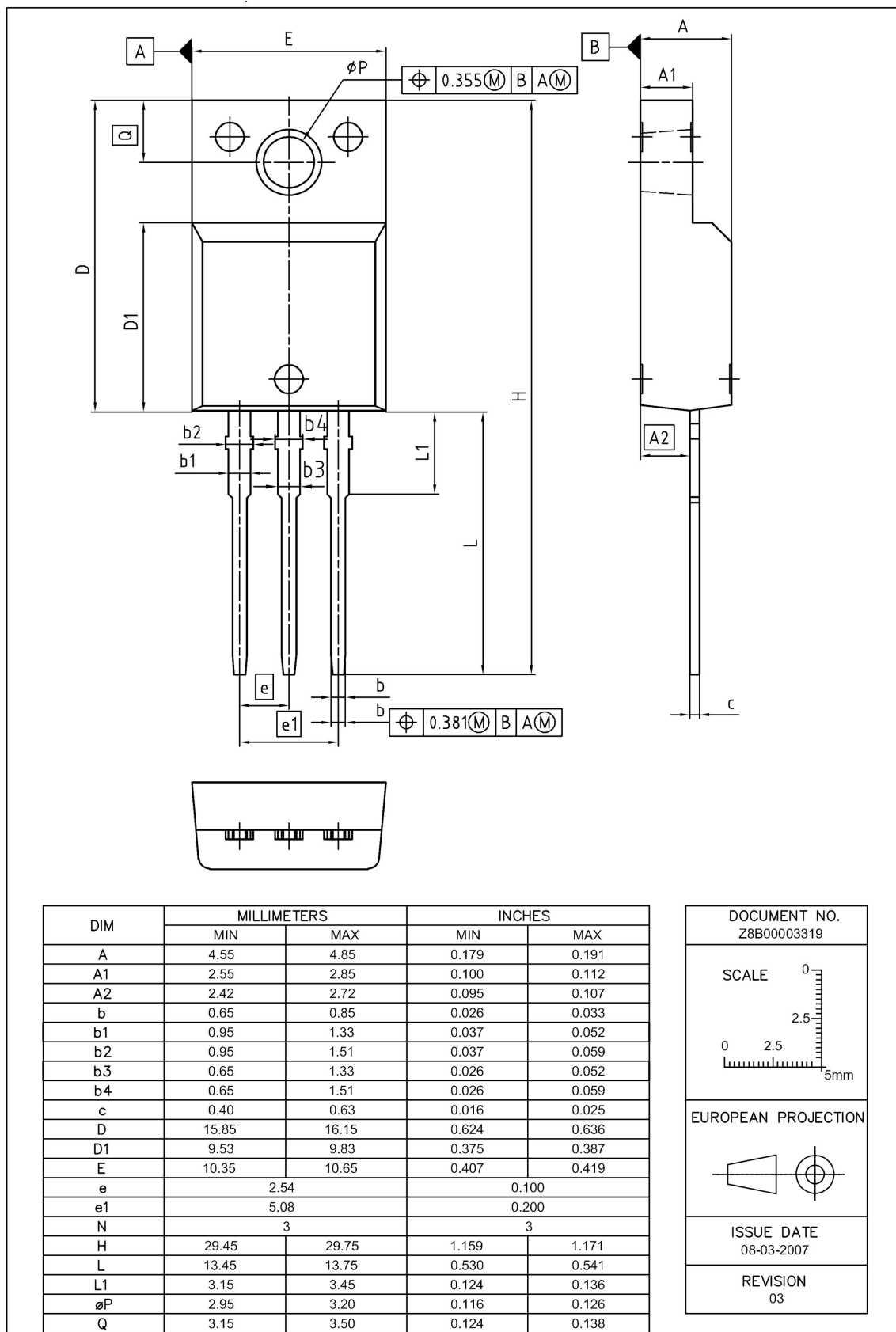


Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- IFX CoolMOS™ C7 Webpage: www.infineon.com
- IFX CoolMOS™ C7 application note: www.infineon.com
- IFX CoolMOS™ C7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPA65R225C7

Revision: 2013-10-22, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-10-22	Release of final version

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

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