



Description

The PHKD6N02LT uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 20V$ $I_D = 6A$

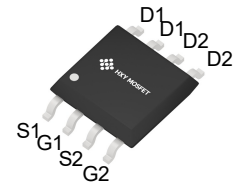
$R_{DS(ON)} < 25m\Omega$ @ $V_{GS}=4.5V$

Application

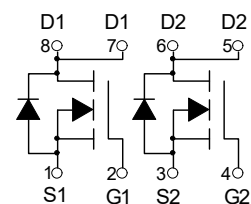
Battery protection

Load switch

Uninterruptible power supply



SOP-8
(SOIC-8)



Dual N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
PHKD6N02LT	SOP-8(SOIC-8)	HXY MOSFET	3000

Absolute Maximum Ratings@ $T_J=25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D@T_A=25^\circ C$	Drain Current, V_{GS} @ 4.5V ³	6	A
$I_D@T_A=70^\circ C$	Drain Current, V_{GS} @ 4.5V ³	4.8	A
I_{DM}	Pulsed Drain Current ¹	26	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	2	W
	Linear Derating Factor	0.016	W/ $^\circ C$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
R_{thja}	Maximum Thermal Resistance, Junction-ambient ³	62.5	$^\circ C/W$



Electrical Characteristics@T_j=25 °C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	20	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =4.5V, I _D =6A	-	21	25	mΩ
		V _{GS} =2.5V, I _D =4A	-	32	45	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	-	1.2	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =6A	-	6	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =20V, V _{GS} =0V	-	-	25	uA
	Drain-Source Leakage Current (T _j =70°C)	V _{DS} =20V, V _{GS} =0V	-	-	250	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±12V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =6A	-	11	17.6	nC
Q _{gs}	Gate-Source Charge	V _{DS} =16V	-	1.1	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	4.1	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =10V	-	4.2	-	ns
t _r	Rise Time	I _D =1A	-	9	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω, V _{GS} =10V	-	23	-	ns
t _f	Fall Time	R _D =10Ω	-	3.5	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V V _{DS} =20V f=1.0MHz	-	570	910	pF
C _{oss}	Output Capacitance		-	90	-	pF
C _{rss}	Reverse Transfer Capacitance		-	85	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.6	2.4	Ω
V _{SD}	Forward On Voltage ²	I _S =1.7A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time ²	I _S =6A, V _{GS} =0V, dI/dt=100A/μs	-	21	-	ns
Q _{rr}	Reverse Recovery Charge		-	14	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in² copper pad of FR4 board, t_≤10sec ; 135 °C/W when mounted on Min. copper pad.



Typical Characteristics

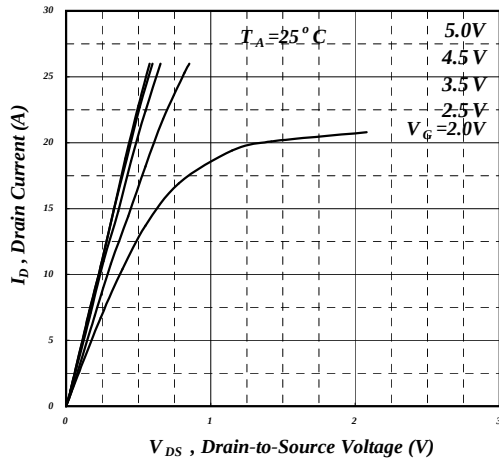


Fig 1. Typical Output Characteristics

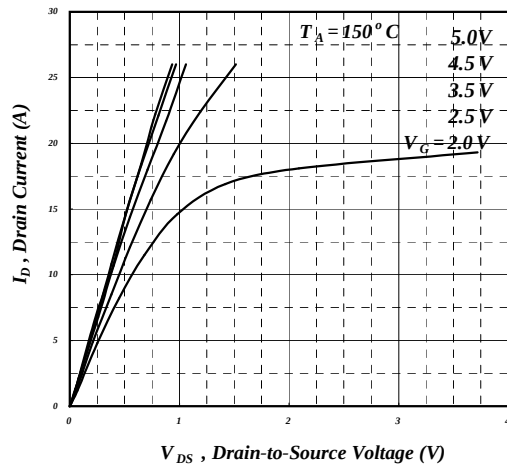


Fig 2. Typical Output Characteristics

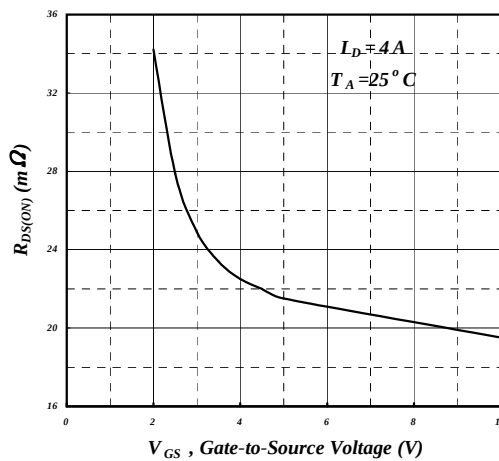


Fig 3. On-Resistance v.s. Gate Voltage

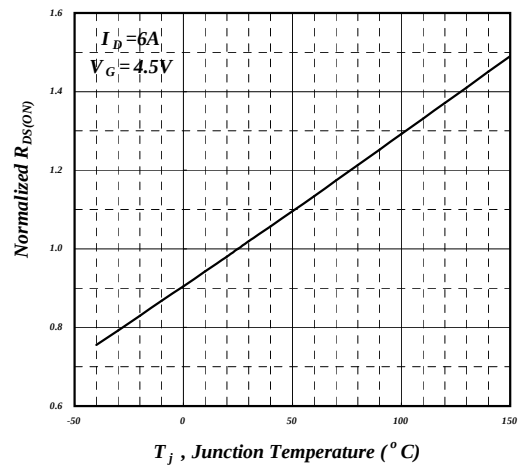


Fig 4. Normalized On-Resistance
v.s. Temperature

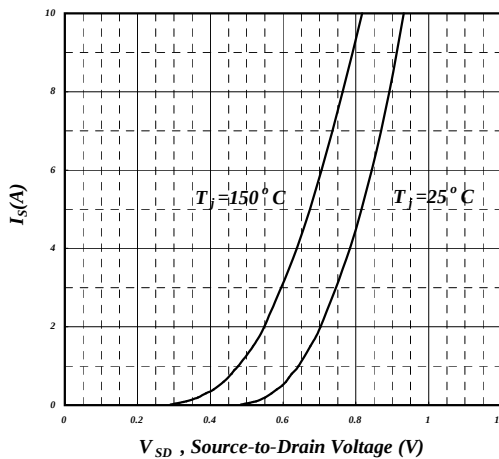


Fig 5. Forward Characteristic of
Reverse Diode

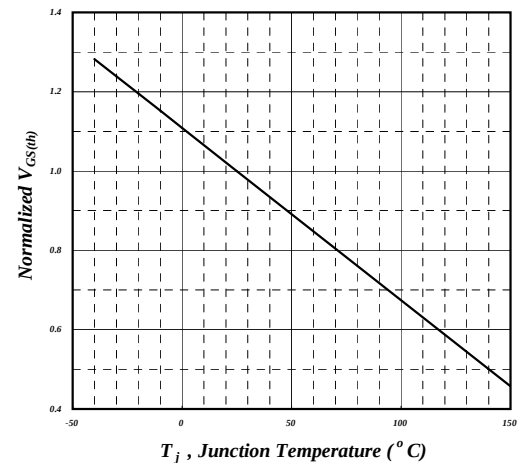


Fig 6. Gate Threshold Voltage v.s.
Junction Temperature

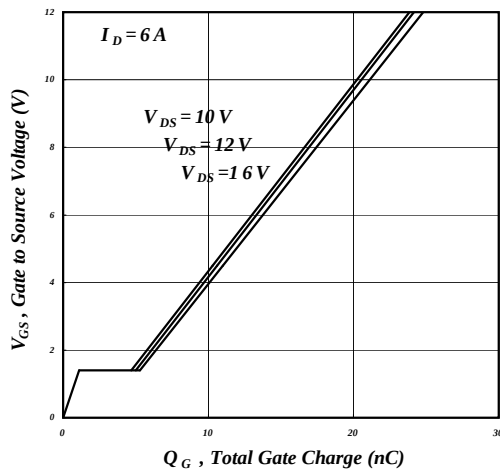


Fig 7. Gate Charge Characteristics

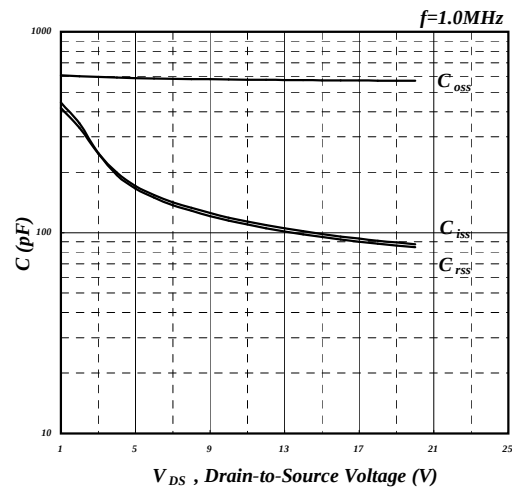


Fig 8. Typical Capacitance Characteristics

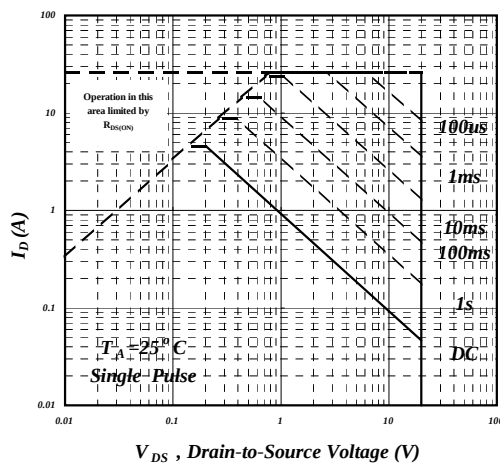


Fig 9. Maximum Safe Operating Area

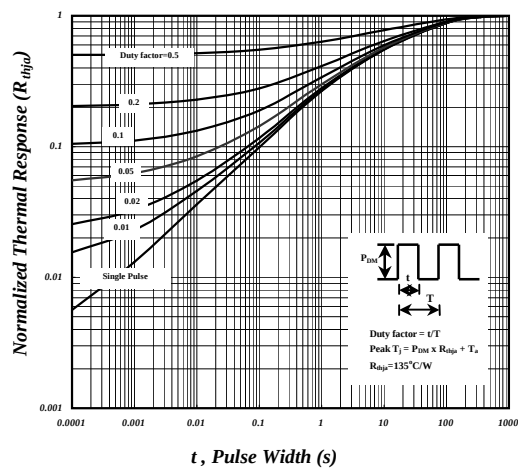


Fig 10. Effective Transient Thermal Impedance

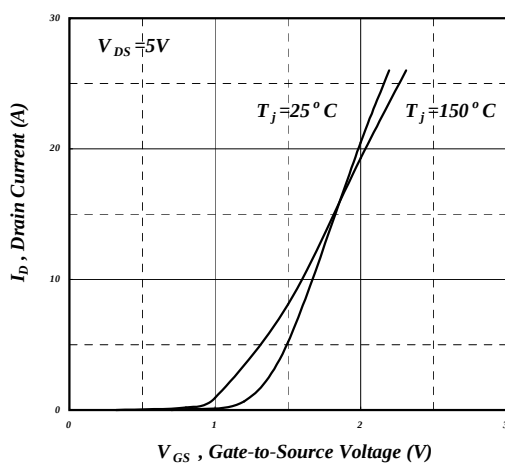


Fig 11. Transfer Characteristics

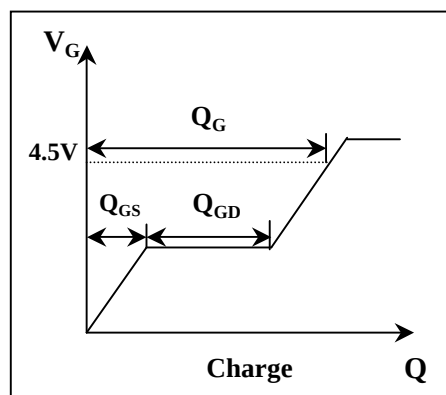
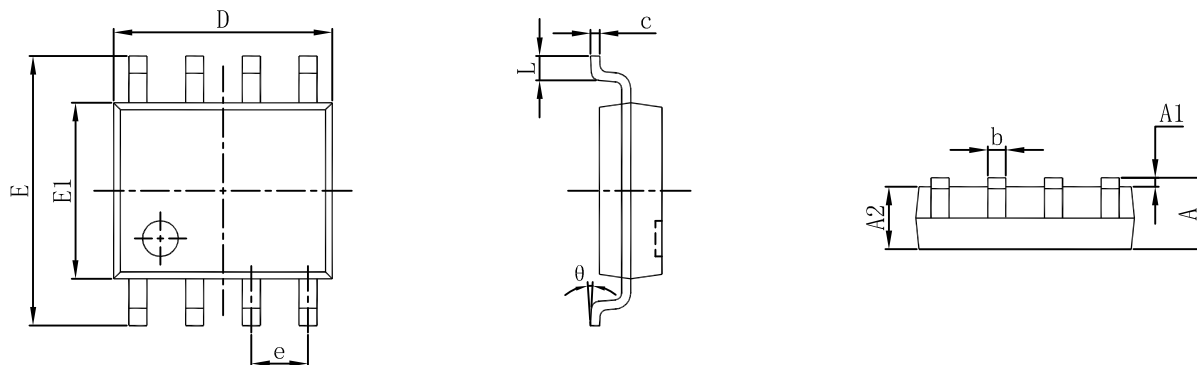


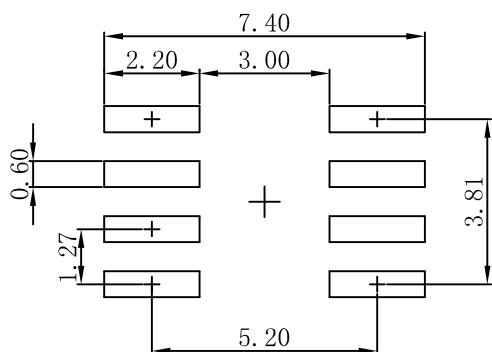
Fig 12. Gate Charge Waveform



SOP-8(SOIC-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1. Controlling dimension; in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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