

Dual P-channel Enhancement Mode Power MOSFET

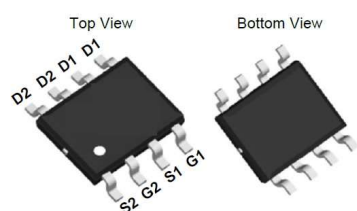
Features

- $V_{DS} = -60V$, $I_D = -5.3A$
 $R_{DS(ON)} < 54m\Omega$ @ $V_{GS} = -10V$
 $R_{DS(ON)} < 60m\Omega$ @ $V_{GS} = -4.5V$

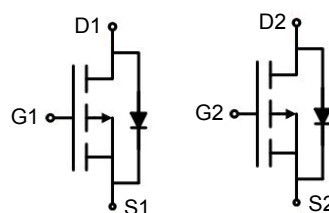
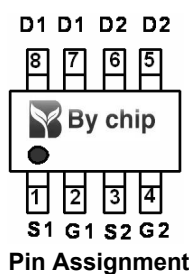
General Features

- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

100% UIS TESTED!
100% ΔV_{ds} TESTED!



SOP-8 (Dual)



Schematic diagram

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	- 60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ C$)	$T_C = 25^\circ C$	I_D	- 5.3 ^e	A
	$T_C = 70^\circ C$		- 5.0 ^e	
	$T_A = 25^\circ C$		- 5.3 ^{a, b}	
	$T_A = 70^\circ C$		- 5.0 ^{a, b}	
Pulsed Drain Current		I_{DM}	- 32 ^e	
Continuous Source-Drain Diode Current	$T_C = 25^\circ C$	I_S	- 4.1	
	$T_A = 25^\circ C$		- 2.0 ^{a, b}	
Avalanche Current	L = 0.1 mH	I_{AS}	- 20	mJ
Single-Pulse Avalanche Energy		E_{AS}	20	
Maximum Power Dissipation	$T_C = 25^\circ C$	P_D	4.0	W
	$T_C = 70^\circ C$		2.5	
	$T_A = 25^\circ C$		2.0 ^{a, b}	
	$T_A = 70^\circ C$		1.4 ^{a, b}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	$t \leq 10s$	R_{thJA}	38	50	$^\circ C/W$
Maximum Junction-to-Foot	Steady State	R_{thJF}	20	25	

Notes:

- Surface mounted on 1" x 1" FR4 board.
- $t = 10s$.
- Maximum under Steady State conditions is 85 $^\circ C/W$.
- Based on $T_C = 25^\circ C$.
- Limited by package.

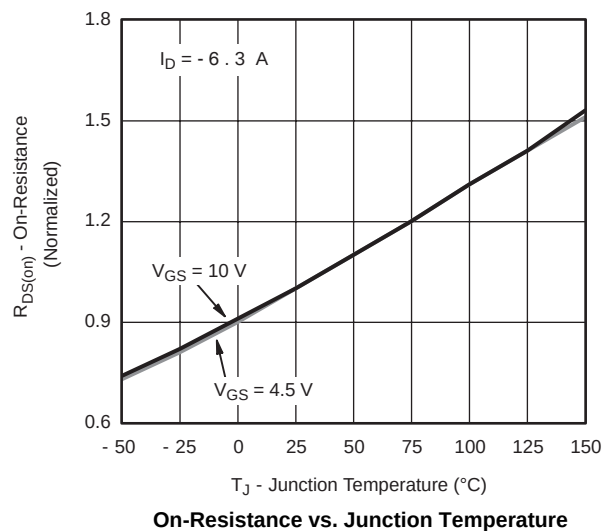
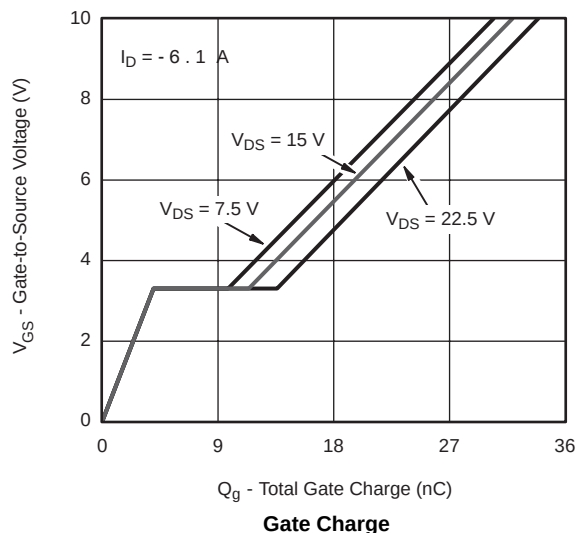
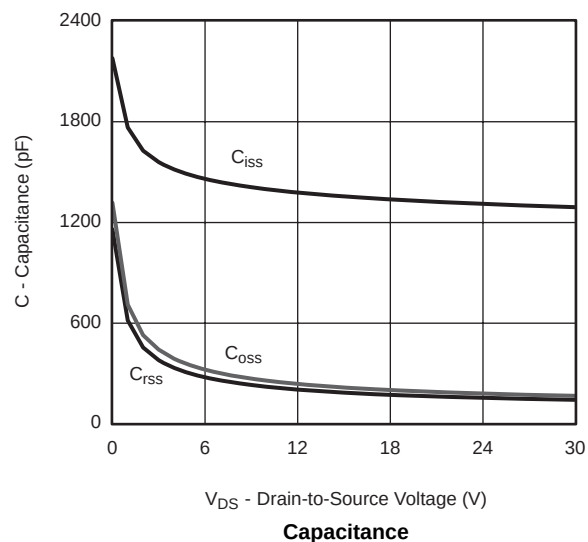
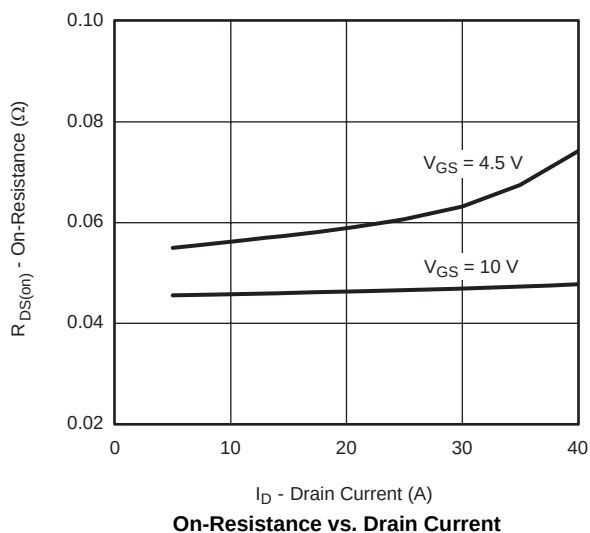
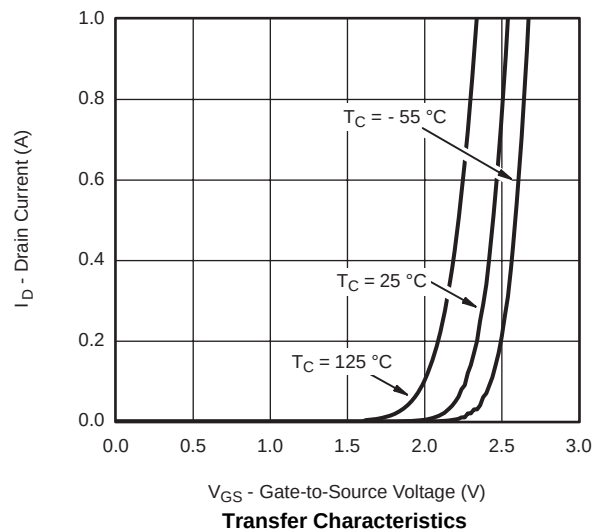
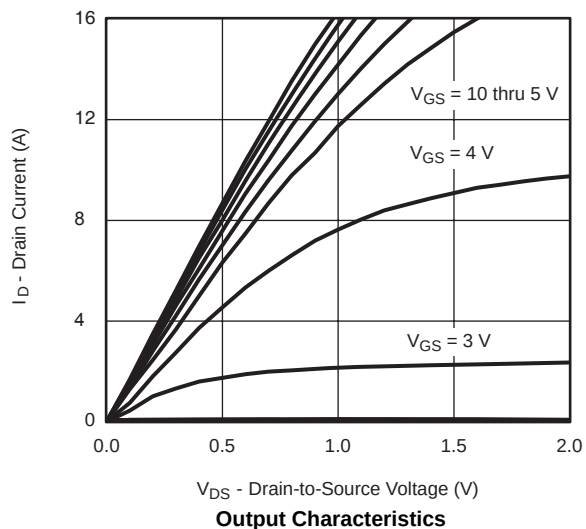
SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 60			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 31		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			4.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1.0		- 3.0	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 30 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 30 V, V _{GS} = 0 V, T _J = 55 °C			- 5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ - 10 V, V _{GS} = - 10 V	- 30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 5 A		0.054		Ω
		V _{GS} = - 4.5 V, I _D = - 4.5 A		0.060		
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 5 A		23		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz		1345		pF
Output Capacitance	C _{oss}			210		
Reverse Transfer Capacitance	C _{rss}			180		
Total Gate Charge	Q _g	V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 5 A		32	50	nC
		V _{DS} = - 15 V, V _{GS} = - 4.5 V, I _D = - 5 A		15	25	
Q _{gs}			4			
Q _{gd}			7.5			
Gate Resistance	R _g	f = 1 MHz		5.8		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 15 V, R _L = 15 Ω I _D ≡ - 1 A, V _{GEN} = - 10 V, R _g = 1 Ω		10	15	ns
Rise Time	t _r			8	15	
Turn-Off DelayTime	t _{d(off)}			45	70	
Fall Time	t _f			12	25	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 15 V, R _L = 15 Ω I _D ≡ - 1 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		42	70	
Rise Time	t _r			35	60	
Turn-Off DelayTime	t _{d(off)}			40	70	
Fall Time	t _f			16	30	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			- 4.1	A
Pulse Diode Forward Current	I _{SM}				- 32	
Body Diode Voltage	V _{SD}	I _S = - 2 A, V _{GS} = 0 V		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 2 A, dI/dt = 100 A/μs, T _J = 25 °C		34	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			22	40	nC
Reverse Recovery Fall Time	t _a			11		ns
Reverse Recovery Rise Time	t _h			23		

Notes:

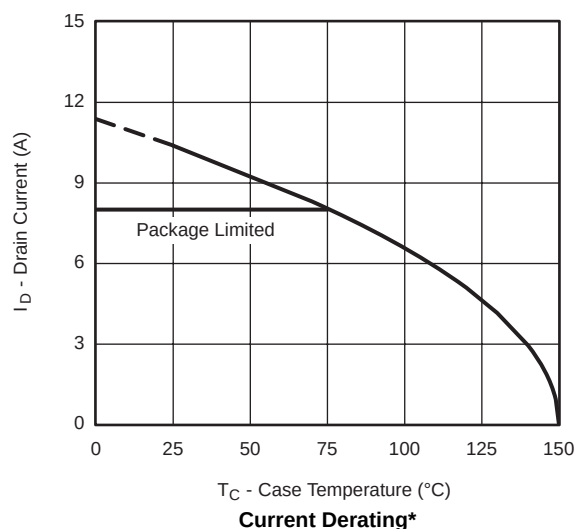
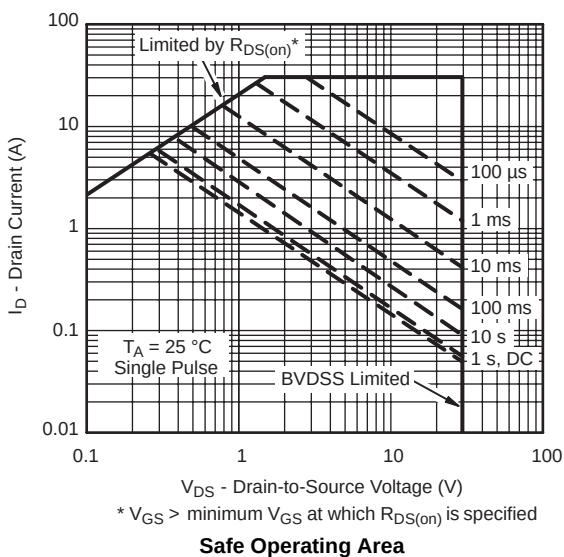
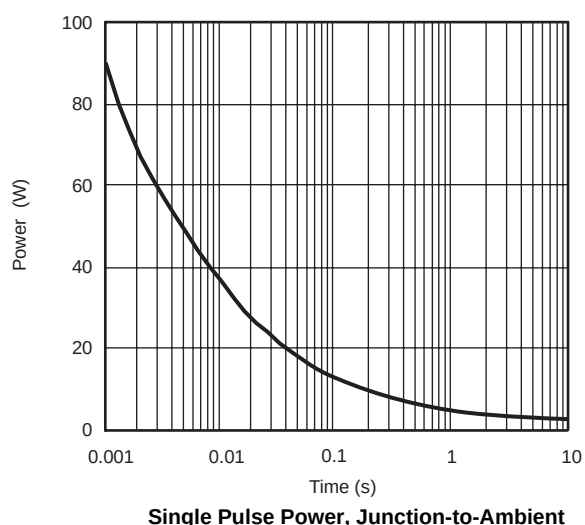
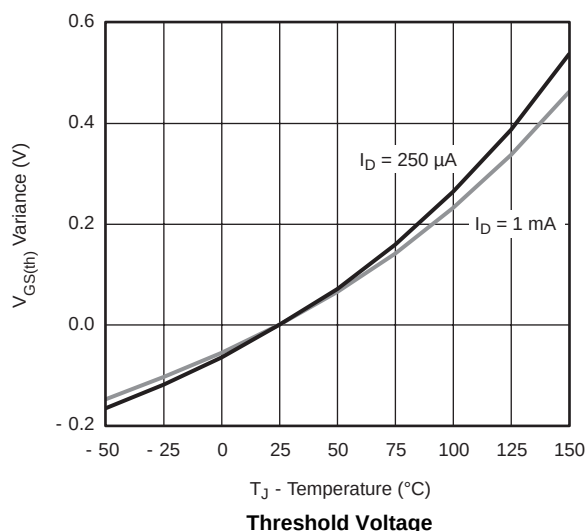
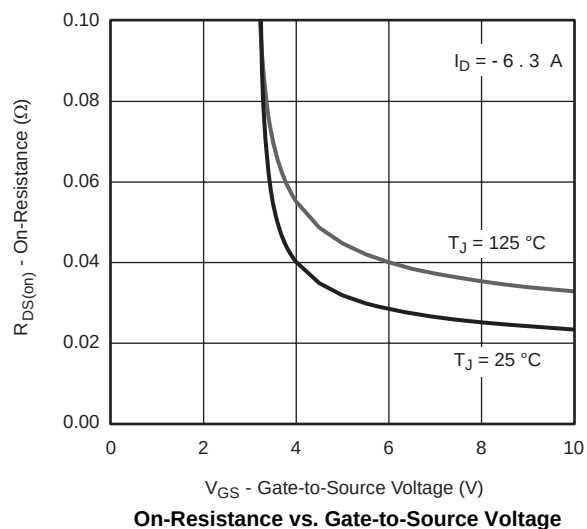
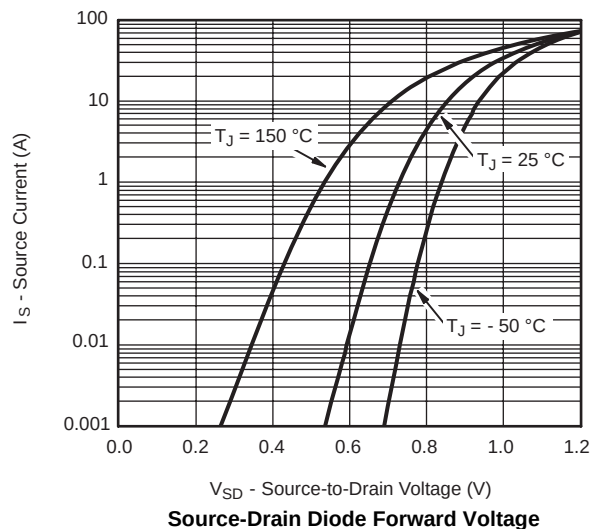
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

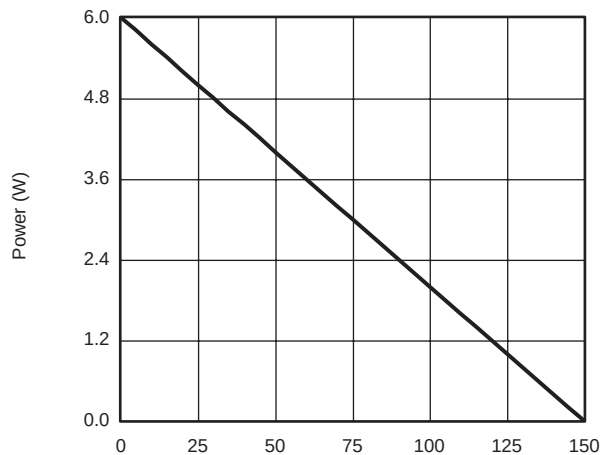
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


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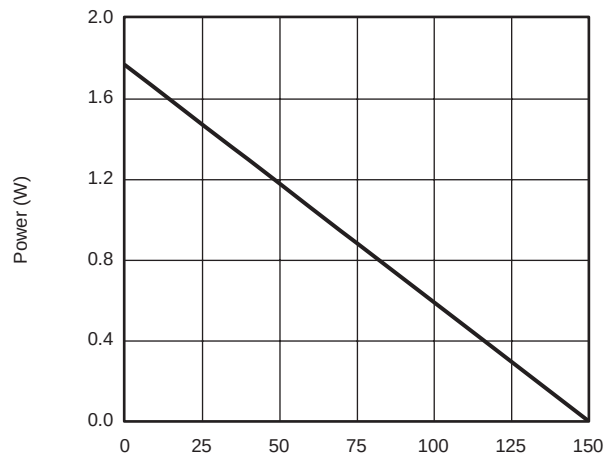


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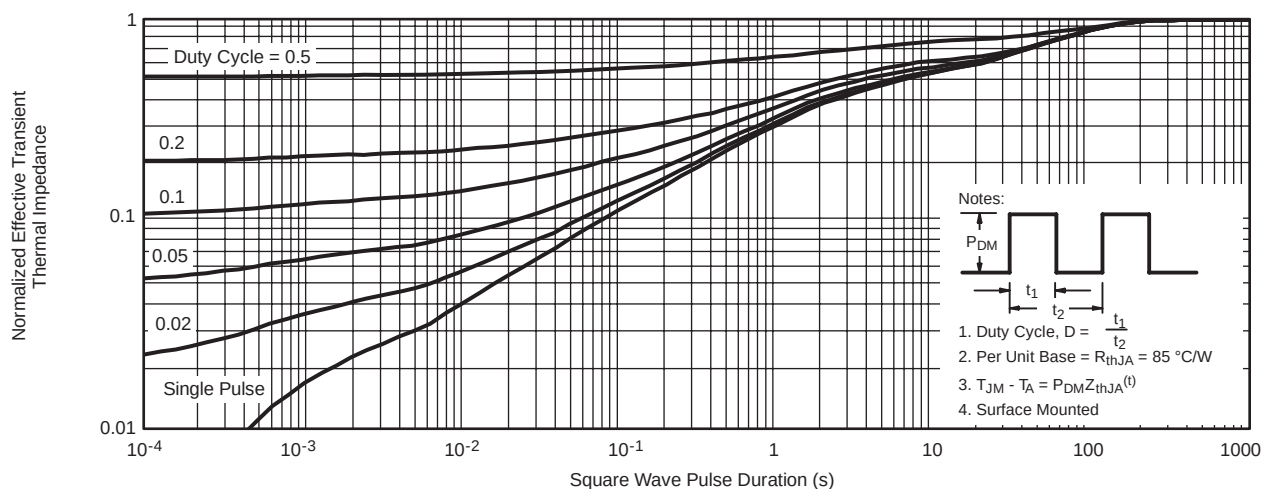
T_C - Case Temperature (°C)

Power, Junction-to-Foot

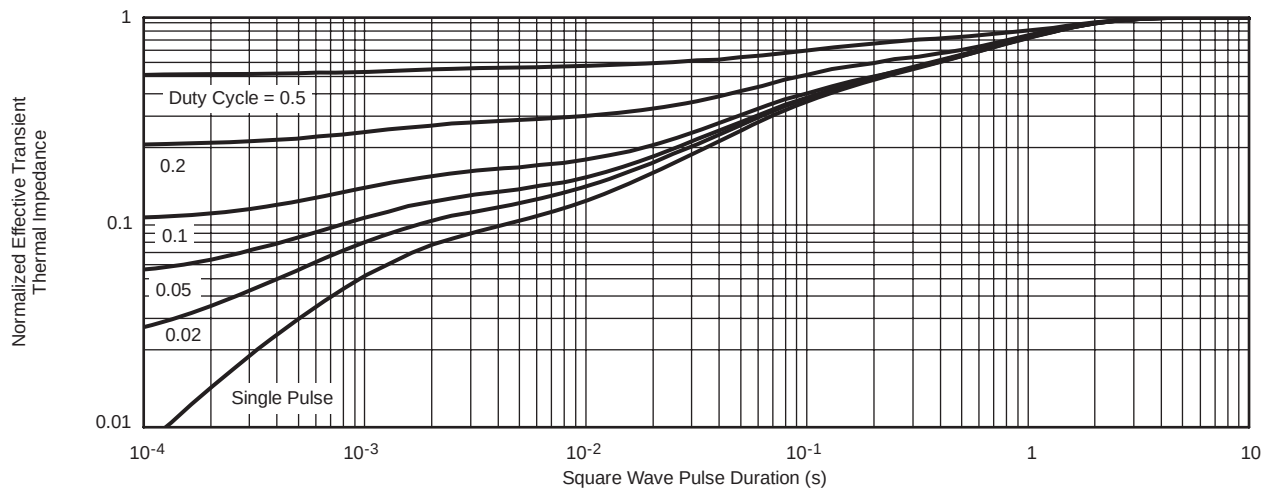


T_A - Ambient Temperature (°C)

Power Derating, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot