

Description

The IRLR3410TRRPBF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



TO-252-2L

General Features

 $V_{DS} = 100V I_{D} = 20A$

 $R_{DS(ON)}$ < 87 m Ω @ V_{GS} =10V

Application

Battery protection

Load switch

Uninterruptible power supply

N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
IRLR3410TRRPBF	TO-252-2L	HXY MOSFET	2500

Absolute Maximum Ratings Tc=25°C unless otherwise noted

Symbol	Parameter	Rating	Units	
V _{DS}	Drain-Source Voltage	100	V	
Vgs	Gate-Source Voltage	±20	V	
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	20	А	
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ¹	10	Α	
Ідм	Pulsed Drain Current ²	30	А	
EAS	Single Pulse Avalanche Energy ³	6.1	mJ	
las	Avalanche Current	15	Α	
P _D @T _C =25°C	Total Power Dissipation ⁴	34.7	W	
P _D @T _A =25°C	Total Power Dissipation ⁴	2	W	
Тѕтс	Storage Temperature Range	-55 to 150	°C	
TJ	Operating Junction Temperature Range	-55 to 150	°C	
R ₀ JA	Thermal Resistance Junction-ambient ¹	62	°C/W	
Rejc	Thermal Resistance Junction-Case ¹	3.6	°C/W	

N-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	100			V	
$\triangle BV_{DSS}/\triangle T$	BVDSS Temperature Coefficient	Reference to 25°C , I _D =1mA		0.098		V/°C	
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V , I _D =10A		80	87	mΩ	
INDS(ON)	Static Drain-Source On-Nesistance	V_{GS} =4.5 V , I_{D} =8 A	_	95	105	mΩ	
V _{GS(th)}	Gate Threshold Voltage	──V _{GS} =V _{DS} , I _D =250uA	1.0		2.5	V	
$\triangle V_{GS(th)}$	V _{GS(th)} Temperature Coefficient	VGS-VDS , ID -230UA		-4.57		mV/°C	
I _{DSS}	Drain-Source Leakage Current	V _{DS} =80V , V _{GS} =0V , T _J =25°C			1		
IDSS		V _{DS} =80V , V _{GS} =0V , T _J =55°C			5	- uA	
I _{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$			±100	nA	
gfs	Forward Transconductance	V _{DS} =5V , I _D =10A		13		S	
Rg	Gate Resistance	V _{DS} =0V , V _{GS} =0V , f=1MHz		2		Ω	
Qg	Total Gate Charge (10V)			26.2			
Qgs	Gate-Source Charge	V_{DS} =80V , V_{GS} =10V , I_{D} =10A		4.6		nC	
Q _{gd}	Gate-Drain Charge			5.1			
T _{d(on)}	Turn-On Delay Time			4.2			
Tr	Rise Time	V_{DD} =50V , V_{GS} =10V , R_{G} =3.3 Ω		8.2		ns	
T _{d(off)}	Turn-Off Delay Time	I _D =10A		35.6			
Tf	Fall Time			9.6			
Ciss	Input Capacitance			1535			
Coss	Output Capacitance	V _{DS} =15V , V _{GS} =0V , f=1MHz		60		pF	
Crss	Reverse Transfer Capacitance			37			
ls	Continuous Source Current ^{1,5}	V _G =V _D =0V , Force Current			20	Α	
Isм	Pulsed Source Current ^{2,5}	vg-vb-ov , Force Current			30	Α	
V_{SD}	Diode Forward Voltage ²	V _{GS} =0V , I _S =1A , T _J =25°C			1.2	>	
t _{rr}	Reverse Recovery Time			37		nS	
Qrr	Reverse Recovery Charge	lF=10A , dl/dt=100A/μs , T _J =25°C		27.3		nC	

Note:

^{1.} The data tested by surface mounted on a 1 inch $^2\,\text{FR-4}$ board with 2OZ copper.

^{2.}The data tested by pulsed , pulse width $\,\leq\,300\text{us}$, duty cycle $\,\leq\,2\%$

^{3.}The EAS data shows Max. rating . The test condition is V_{DD} =25V, V_{GS} =10V,L=0.1mH, I_{AS} =11A

^{4.}The power dissipation is limited by 150°C junction temperature

^{5.} The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.



Typical Characteristics

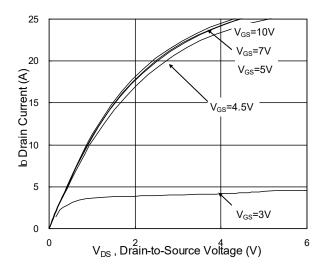


Fig.1 Typical Output Characteristics

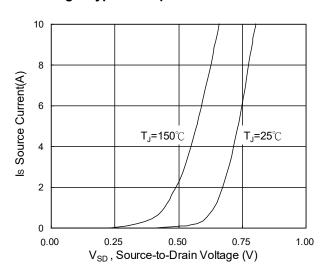


Fig.3 Forward Characteristics Of Reverse

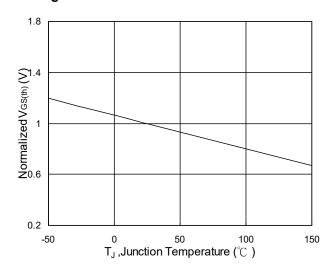


Fig.5 Normalized $V_{\text{GS(th)}}$ vs. T_{J}

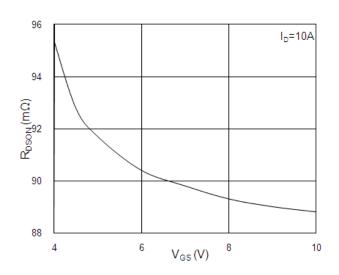


Fig.2 On-Resistance vs. Gate-Source

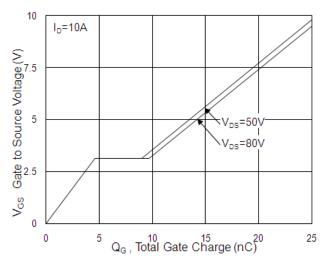


Fig.4 Gate-Charge Characteristics

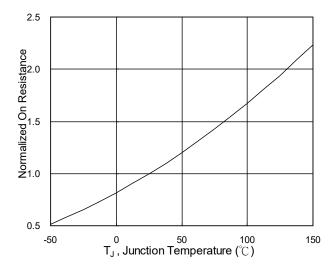
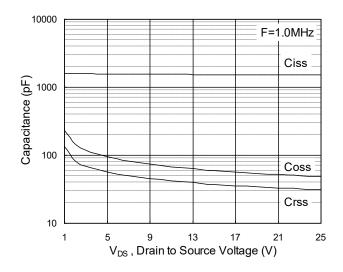


Fig.6 Normalized R_{DSON} vs. T_J



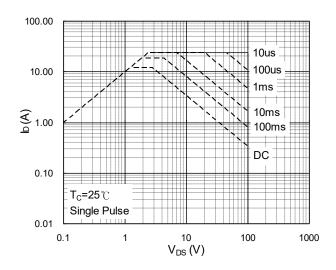


Fig.7 Capacitance

Fig.8 Safe Operating Area

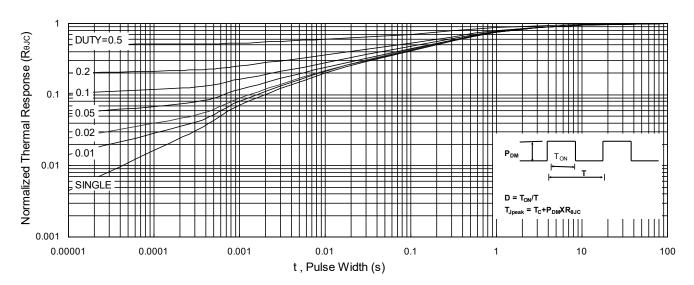
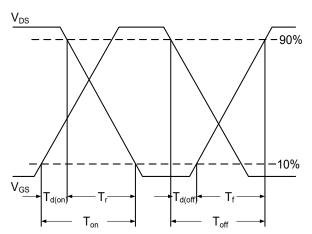


Fig.9 Normalized Maximum Transient Thermal Impedance





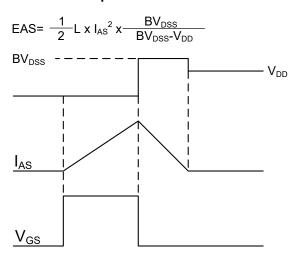
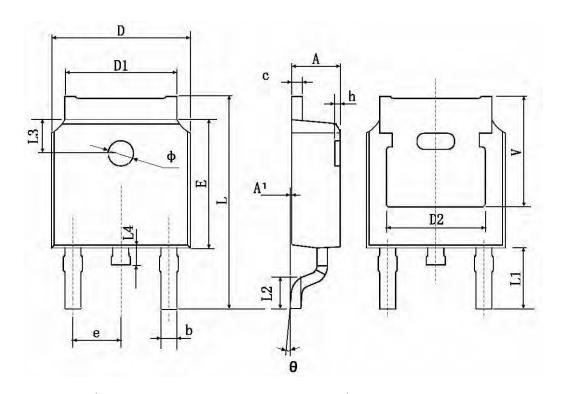


Fig.11 Unclamped Inductive Switching Waveform

N-Channel Enhancement Mode MOSFET

TO-252-2L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches			
	Min.	Max.	Min.	Max.		
Α	2.200	2.400	0.087	0.094		
A1	0.000	0.127	0.000	0.005		
b	0.660	0.860	0.026	0.034		
С	0.460	0.580	0.018	0.023		
D	6.500	6.700	0.256	0.264		
D1	5.100	5.460	0.201	0.215		
D2	0.483	0.483 TYP.		0.190 TYP.		
E	6.000	6.200	0.236	0.244		
е	2.186	2.386	0.086	0.094		
L	9.800	10.400	0.386	0.409		
L1	2.900	TYP.	0.114 TYP.			
L2	1.400	1.700	0.055	0.067		
L3	1.600	TYP.	0.063 TYP.			
L4	0.600	1.000	0.024	0.039		
Ф	1.100	1.300	0.043	0.051		
θ	0°	8°	0°	8°		
h	0.000	0.300	0.000	0.012		
V	5.350	TYP.	0.211 TYP.			



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