Automotive Dual DrMOS with Integrated Current and Temperature Sense

NCV81341, NCV81341P

The NCV81341/P (NCV81341 – Single Phase and Two Independent Phases Mode, NCV81341P – Parallel Mode) integrates two MOSFET drivers, high−side MOSFET and low−side MOSFET into a single package with current sense and temperature monitoring into a compact 3.5x3.5 QFN.

The driver and MOSFETs have been optimized for high−current DC−DC buck power conversion applications. The NCV81341/P integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Qualified for Automotive Applications
- AEC−Q100, Grade 2 Qualified
- Switching Frequency of up to 2 MHz
- Capable of Currents up to 5 A/phase
- Integrated Current Sense Replaces Inductor DCR Sensing
- Integrated Short Circuit Protection
- Compatible with 3.3 V PWM Input
- Responds Properly to 3−level PWM Inputs
- VCCA/VCCP Under−voltage Lockout
- Thermal Warning Output
- Thermal Shutdown
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

Applications

- Advanced Driver Assistance Systems (ADAS)
- Automotive Applications

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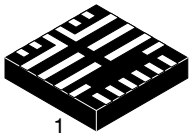
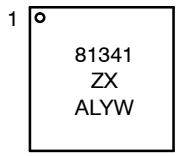


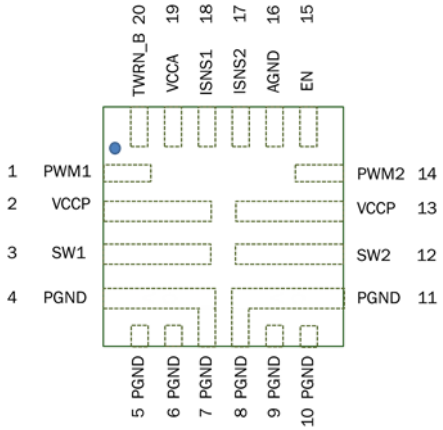
WQFNW20 3.5x3.5
CASE 512AB

MARKING DIAGRAM



81341 = Specific Device Code
Z = Optional Marking (Planarized Passivation = A)
X = Optional Marking (Parallel Mode = P)
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCV81341MTWTXG	QFN20 (Pb−Free)	3000 / Tape & Reel
NCV81341PMTWTXG	QFN20 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

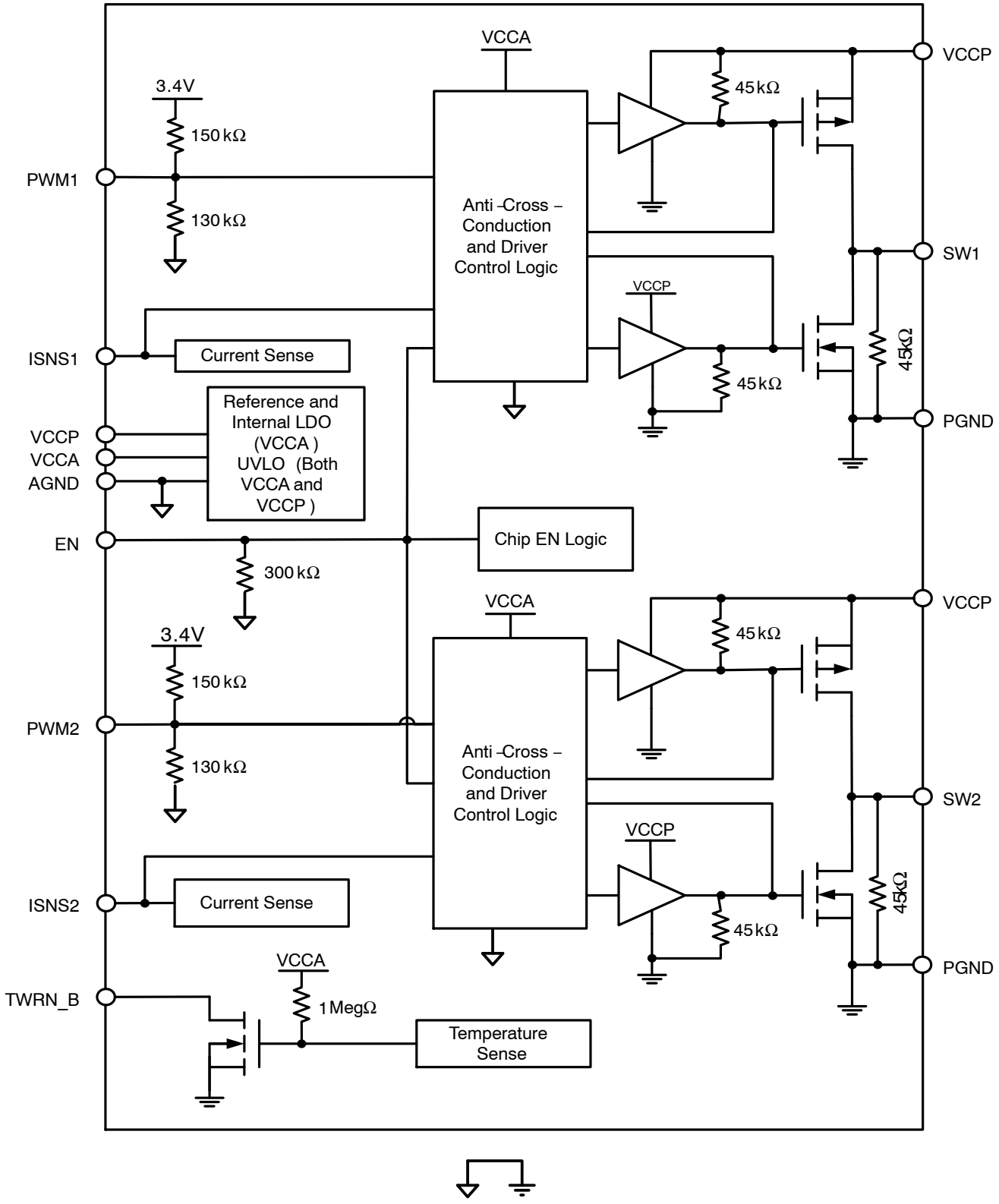


Figure 1. Block Diagram

PIN LIST AND DESCRIPTIONS

Pin No.	Symbol	Description
1	PWM1	PWM control input of DrMOS1
2, 13	VCCP	Exposed pad connection to power supply input of both DrMOS1/2. Minimum 10 μF decoupling recommended on each VCCP pin.
3	SW1	Switch node output of DrMOS1
4−11	PGND	Power ground to both DrMOS1/2
12	SW2	Switch node output of DrMOS2
14	PWM2	PWM control input of DrMOS2
15	EN	Enable input to device.
16	AGND	Signal ground
17	ISNS2	Current sense output of DrMOS2
18	ISNS1	Current sense output of DrMOS1
19	VCCA	Signal power supply input. Recommend minimum filter to VCCP of 5−10 Ω and 100 nF.
20	TWRN_B	Open drain thermal warning flag. Recommend applying a pullup of 1 kΩ to VCCP/A

ABSOLUTE MAXIMUM RATINGS (Electrical Information − all signals referenced to PGND unless noted otherwise)

Pin Name / Parameter	Min	Max	Unit
VCCP, VCCA	−0.3	6.0	V
SW1/2, (DC)	−0.3	6.0	V
SW1/2, (< 10 ns) (Notes 1 and 2)	−5	8.0	V
VCCP−VSW (< 4ns) (Notes 1 and 2)	−2	9	V
All Other Pins	−0.3	V_{VCC} + 0.3	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Parameter is not tested in production ATE.
2. Values are based on wafer fab data.

THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Resistance (Note 3)	$R_{\Psi J-A}$	15	°C/W
	$R_{\Psi J-BT}$	11	°C/W
	$R_{\Psi J-CT}$	1	°C/W
Operating Junction Temperature Range (Note 4)	T_J	−40 to +150	°C
Operating Ambient Temperature Range	T_A	−40 to +105	°C
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Maximum Power Dissipation		3.5	W
Moisture Sensitivity Level	MSL	1	

3. Thermal characterization will be finalized on rev release.
4. The maximum package power dissipation must be observed.
5. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
6. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Conditions	Min	Typ	Max	Unit
Supply Voltage Range	VCCA, VCCP		4.0	5.0	5.5	V
VCCP – VSW (< 4ns) (Notes 1 and 2)		F_{SW} = 2 MHz, V_{IN} = 5.5 V, V_{OUT} = 1.2 V Iout = 4 A (per phase), L = 150 nH	–1.8		8.5	V
SW – GND (< 10ns) (Notes 1 and 2)			–1.8		7	V
Continuous Output Current Single Phase Operation Two Phases Operation (In parallel)		F_{SW} = 2 MHz, V_{IN} = 5 V, V_{OUT} = 1.5 V			 5 10	 A A
Peak Output Current Single Phase Operation Two Phases Operation (In parallel) (Note 7)		F_{SW} = 2.0 MHz, V_{IN} = 5 V, V_{OUT} = 1.5 V, Duration = 10 ms, Period = 1 s			 10 20	 A A

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. Parameters are guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS

(V_{VCCA} = V_{VCCP} = 4.0–5.5 V, V_{EN} = 2.0 V, C_{VCCA} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test or statistical correlation. Min/Max values are valid for temperatures up to $T_{J\,=}$ 150°C, unless noted otherwise. These parameters are guaranteed by design and characterization.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCCA SUPPLY CURRENT						
Operating		EN = 5 V, PWM = 2.0 MHz Single Phase Operation Two Phase Operation (Independent) Parallel Mode Operation	5 5 5		10 15 15	mA
No switching		EN = 5 V, PWM = 0 V	2	4	6	mA
Disabled		EN = 0 V PWM = High Z	300	600	900	μA
UVLO Start Threshold	V_{UVLO}	VCCA rising	3.4	3.7	4	V
UVLO Stop Threshold		VCCA falling	3.3	3.5	3.7	V
UVLO Hysteresis		VCCA falling	50	200	600	mV
VCCP SUPPLY CURRENT						
Operating		EN = 5 V, PWM = 2.0 MHz, Single Phase Operation Two Phase Operation (Independent) Parallel Mode Operation	20 20 20		78 156 156	mA
No switching		EN = 5 V, PWM = 0 V	50	150	300	μA
Disabled		EN = 0 V PWM = High Z	10	35	120	μA
EN INPUT						
Input Resistance		To Ground	225	300	400	kΩ
Upper Threshold	V_{UPPER}		1.45	1.75	2.0	V
Lower Threshold	V_{LOWER}		0.8	1.25	1.5	V
Hysteresis		V_{UPPER} – V_{LOWER}	150	500	850	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Critical or Safety Parameters.
9. Parameter may shift over operation life.
10. Values represent T_J = 150°C continuous operation for given hours and guaranteed by test and statistical correlation.

ELECTRICAL CHARACTERISTICS (continued)
(V_{VCCA} = V_{VCCP} = 4.0–5.5 V, V_{EN} = 2.0 V, C_{VCCA} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test or statistical correlation. Min/Max values are valid for temperatures up to T_J = 150°C, unless noted otherwise. These parameters are guaranteed by design and characterization.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Enable Delay Time		EN = L→H (90%) to SW = L→H (10%) 0 A Load	0.6		30	μs
Disable Delay Time		EN = H→L (10%) to SW = H→L (90%) −180 mA Load on SW	10	40	100	ns
Enable Pull Down Voltage	V_{OL_ENABLE}	I_{PULLUP} = 5 mA (V = 5 V)	50	100	400	mV
PWM1/2 INPUT / SW1/2 OUTPUT						
Input High Voltage	V_{PWM_HI}		2.65			V
Input Mid−state Voltage	V_{PWM_MID}	Rising edge	1.4		1.8	V
Input Low Voltage	V_{PWM_LO}				0.7	V
Input Resistance	R_{PWM_BIAS}		30	50	70	kΩ
PWM Input Bias Voltage	V_{PWM_BIAS}		1.4	1.6	1.8	V
PWM Propagation Delay, Rising	T_{PWM,PD_R}	PWM = L→H (90%) to SW = L→H (10%) 0 A Load	10	20	36	ns
PWM Propagation Delay, Falling	T_{PWM,PD_F}	PWM = H→L (10%) to SW = H→L (90%) 0 A Load	10	20	36	ns
SW rise time	T_{RISE}	V = 5 V, 10% → 90%, 0 A Load	1	2.5	5	ns
SW fall time	T_{FALL}	V = 5 V, 90% → 10%, 0 A Load	1	2	5	ns
Exiting PWM Mid−state Propagation Delay, Mid−to−Low	$T_{PWM\_EXIT\_Z-L}$	PWM = M→L (0.425 V) to SW = HiZ→L (90%) 0A Load	15	25	35	ns
Exiting PWM Mid−state Propagation Delay, Mid−to−High	$T_{PWM\_EXIT\_Z-H}$	PWM = M→H (4.175 V) to SW = HiZ→H (10%) 0A Load	20	32	45	ns
Entering PWM Mid−state Propagation Delay, Low−Mid	$T_{PWM\_EXIT\_L-Z}$	PWM = L→M (1.275 V) to SW = L→HiZ (10%) 0A Load	20	40	55	ns
P−Channel MOSFET On Resistance (Note 6)	R_{ONHS}	Buck Power Supply1 − From PVIN1 to SW1 pins (V = 5 V)	10	16	23	mΩ
N−Channel MOSFET On Resistance (Note 6)	R_{ONLS}	Buck Power Supply1 − From SW1 to PGND1 pins (V = 5 V)	5	10	16	mΩ
ISNS1/2 OUTPUT / OVERCURRENT PROTECTION						
Current Sense Gain			19	20	21	uA/A
High Side Current Sense Accuracy (Note 8, Note 9)		Iout = 1.5 A Iout = 3 A Iout = 5 A	−30 −15 −10		30 15 10	% % %

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Critical or Safety Parameters.
9. Parameter may shift over operation life.
10. Values represent T_J = 150°C continuous operation for given hours and guaranteed by test and statistical correlation.

ELECTRICAL CHARACTERISTICS (continued)
(V_{VCCA} = V_{VCCP} = 4.0–5.5 V, V_{EN} = 2.0 V, C_{VCCA} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test or statistical correlation. Min/Max values are valid for temperatures up to T_J = 150°C, unless noted otherwise. These parameters are guaranteed by design and characterization.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low Side Current Sense Accuracy (Note 8, Note 9)		Iout = 1.5 A Iout = 3 A Iout = 5 A	−62 −26 −11		62 26 11	% % %
High and Low Side Current Sense Life Drift (Note 10)		Iout = 5 A Operation time: 500 hours 5000 hours 15000 hours 50000 hours 500000 hours	 0 0 0 0 0		 20 25 28 30 35	%
High Side Sourcing Overcurrent Protection Threshold (Note 8, Note 9)	I_{OCP_H}	NCV81341	9.8	10.8	12.3	A
		NCV81341P (SWN pins are required to be shorted together)	18.2	20.2	23.2	A
Low Side Sinking Overcurrent Protection Threshold (Note 8, Note 9)	I_{OCP_L}	NCV81341	5.4	7.2	8.4	A
		NCV81341P (SWN pins are required to be shorted together)	12.2	15.8	18.2	A
High and Low Side Sourcing Overcurrent Protection Threshold Life Drift (Note 10)	ΔI_{OCP_H} ΔI_{OCP_L}	Operation time: 500000 hours Sourcing Iout = 10 A Sinking Iout = 7 A	 0 0		 1.75 1.75	 A A
TWRN_B OUTPUT / THERMAL WARNING & SHUTDOWN						
Thermal Warning Temperature	T_{THWN}		115	120	125	°C
Thermal Warning Hysteresis (Note 5)	T_{THWN_HYS}			5		°C
Thermal Shutdown Temperature	T_{THDN}		140	145	150	°C
Thermal Shutdown Hysteresis	T_{THDN_HYS}			10		°C
TWRN_B Pull Down Voltage	$V_{OL\_TWRN\_B}$	I_{PULLUP} = 5 mA	10	100	400	mV
TWRN_B Pulse Frequency	$TWRN_{CLK}$	Thermal Warning	21		34	kHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
8. Critical or Safety Parameters.
9. Parameter may shift over operation life.
10. Values represent T_J = 150°C continuous operation for given hours and guaranteed by test and statistical correlation.

Table 1. INPUT TRUTH TABLE

EN	PWM (Note 7)	GH	GL
L	X	L	L
H	H	H	L
H	L	L	H
H	MID	L	L (Note 8)

11. PWM input is driven to mid−state with internal divider resistors when PWM input is not externally driven.
12. There is no delay before GL goes low.

POWER LOSS AND THERMAL INFORMATION

NOTE: Typical thermal data is taken on applications eval board. For details on test setup and conditions refer to NCV81341/P Power Loss and Thermal Evaluation.

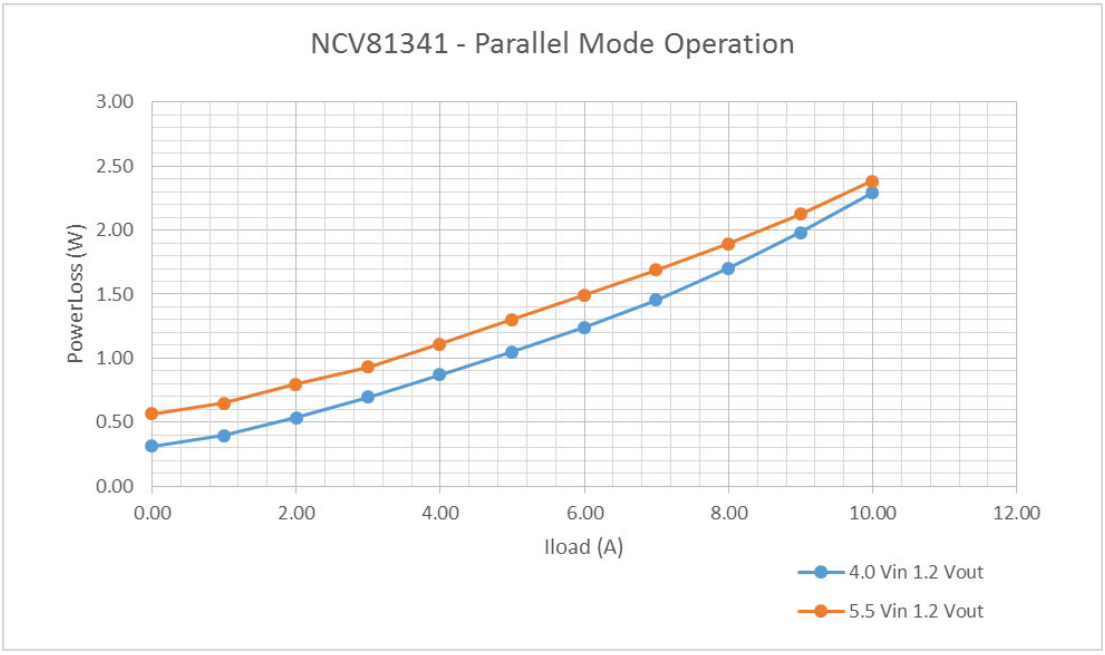


Figure 2. Power Loss vs Iload, T_A = 25°C

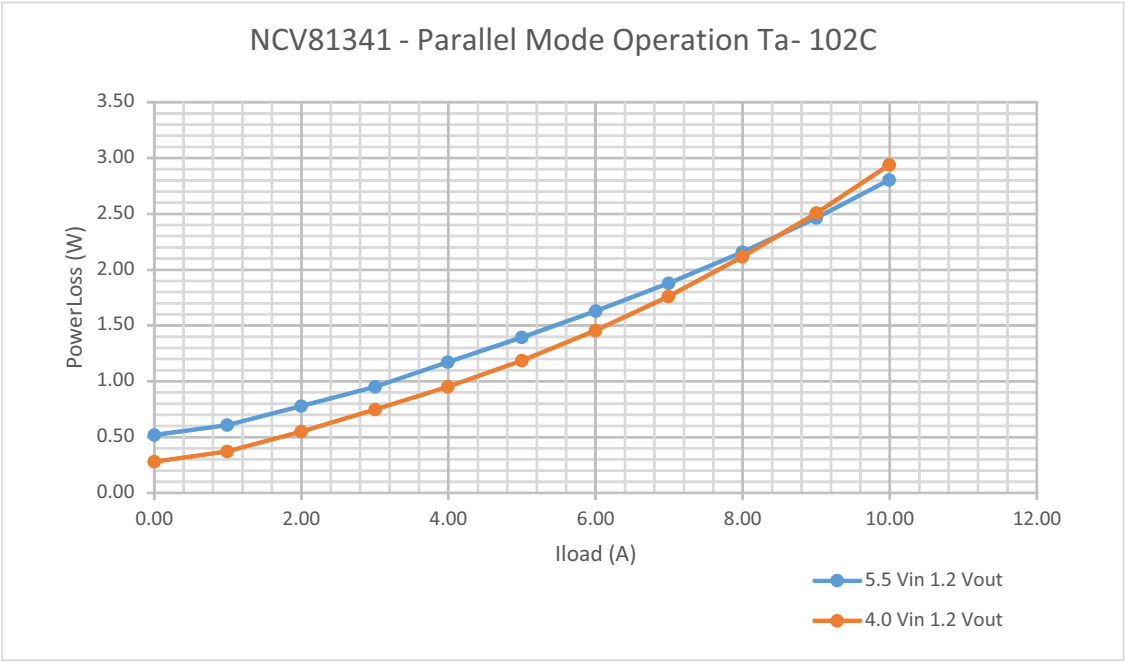


Figure 3. Power Loss vs Iload, T_A = 102°C

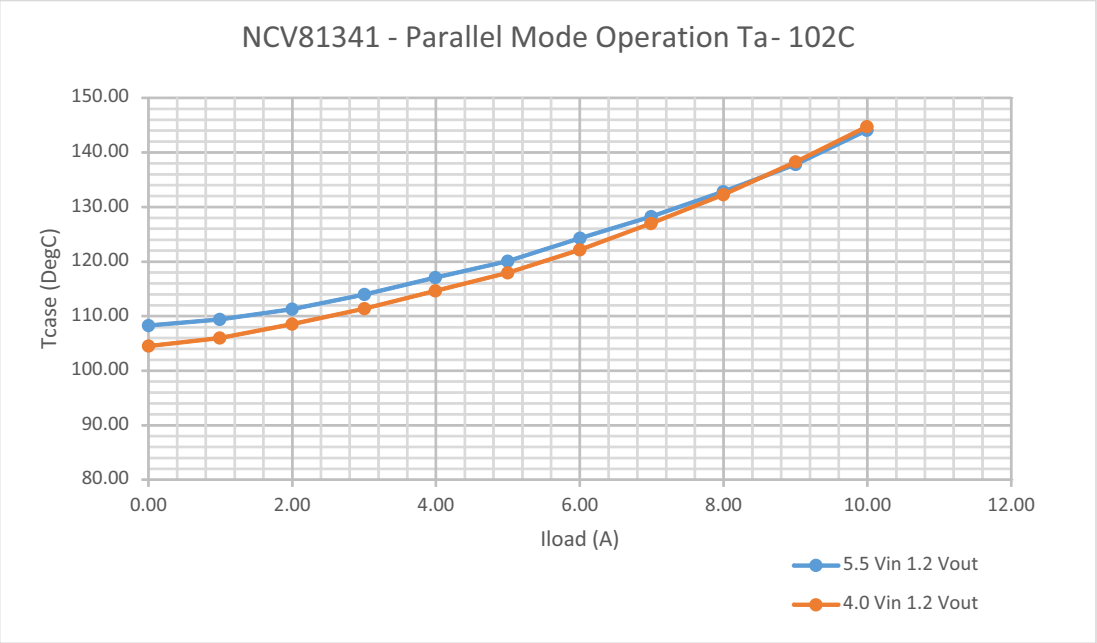


Figure 4. Case Temperature vs Iout, T_A = 102°C

APPLICATIONS INFORMATION

Theory of Operation

The NCV81341/P is a dual integrated driver and MOSFET module designed for use in a synchronous buck converter topology for automotive applications. The NCV81341/P supports numerous application control definitions including Pin enable and PWM Tristate control. A PWM input signal is required to control the drive signals to the high−side and low−side integrated MOSFETs.

Low−Side Driver

The low−side driver drives an internal, ground−referenced low−R_{DS}(on) N−Channel MOSFET. The voltage supply for the low−side driver is internally connected to the VCCP and PGND pins.

High−Side Driver

The high−side driver drives an internal, ground−referenced low−R_{DS}(on) P−Channel MOSFET. The voltage supply for the high−side driver is internally connected to the VCCP and PGND pins.

Power Supply Decoupling

The NCV81341/P will source relatively large currents into the MOSFET gates. In order to maintain a constant and stable supply voltage (VCCP) a low−ESR capacitor should be placed near the power and ground pins. In addition to bulk decoupling, a multi−layer ceramic capacitor (MLCC) between 0.1 μF and 0.47 μF is typically used per each phase. It is important to place these capacitors on the same layer, right next to the DrMOS to maintain high voltage spikes across the high−side MOSFET within spec limits.

A separate supply pin (VCCA) is used to power the analog and digital circuits within the driver. A 0.1 μF to 0.47 μF ceramic capacitor should be placed on this pin in close proximity to the NCV81341. It is good practice to separate the VCCP and VCCA decoupling capacitors with a resistor (5−12 Ω typical) to avoid coupling driver noise to the analog and digital circuits that control driver function. VCCA and VCCP should not be more than 300 mV apart.

Safety Timer and Overlap Protection Circuit

It is important to avoid cross−conduction of the two MOSFETS which could result in a decrease in the power conversion efficiency or damage to the device.

The NCV81341 prevents cross conduction by monitoring the status of the MOSFETs and applying the appropriate amount of non−overlap (NOL) time (the time between the turn−off of one MOSFET and the turn−on of the other MOSFET). When the PWM input pin is driven high, the gate of the low−side MOSFET (LSGATE) will go low after a propagation delay (tpdlGL). The time it takes for the low−side MOSFET to turn off is dependent on the total charge on the low−side MOSFET gate.

The NCV81341 monitors the gate voltage of both MOSFETs and the switch node voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer will delay (tpdhGH) the turn−on of the high−side MOSFET. When the PWM input pin goes low, the gate of the high−side MOSFET (HSGATE) will go low after the propagation delay (tpdlGH). The time to turn off the high−side MOSFET (tfGH) is dependent on the total gate charge of the high−side MOSFET. A timer is triggered once the high−side MOSFET has stopped conducting, to delay (tpdhGL) the turn−on of the low−side MOSFET.

PWM Input

The PWM Input pin is a tri−state input used to control the HS and LS MOSFET ON/OFF states.

Enable Input (EN)

The EN pin is used to disable the GH to the High−Side FET to prevent power transfer. The pin has a pull−down resistance to force a disabled state when it is left unconnected. EN can be driven from the output of a logic device or set high with a pull−up resistance to VCCA. If EN pin is left floating, it will be pulled−down to ground level through a 300 kΩ internal resistor.

Prior to enabling the NCV81341/P, any PWM signals supplied to the DrMOS should be placed in tri−state. After EN goes Hi, there is at least 100 μs or more before PWM starts switching. This time is used for fuse read−in.

EN is also used to alert the NCV81340 whether the NCV81341 exceeded its UVLO threshold or not. The EN pin has an open drain output that will pull down whenever NCV81341 is below its UVLO level (rising or falling). It will release once the UVLO has been exceeded and the part is done initializing.

VCCA Under−voltage Lockout

The VCCA pin is monitored by an Under−voltage Lockout Circuit (UVLO). VCCA voltage above the rising threshold enables the NCV81341.

Table 2. UVLO/EN LOGIC TABLE

VCCP/VCCA	EN	Driver State
< UVLO	X	Disabled (GH = GL = 0)
> UVLO	L	Disabled (GH = GL = 0)
> UVLO	H	Enabled (See Table 1)
> UVLO	Open	Disabled (GH = GL = 0)

Thermal Warning Output

The TWRN_B pin is an open drain output. When the temperature of the driver exceeds T_{THWN}, the THWN pin will be pulsed low at 29 kHz with a 3.125% duty cycle signal (1.077 μs on, 33.406 μs off) indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops T_{THWN_HYS} below T_{THWN}, the TWRN_B pin will go high. If the driver temperature exceeds T_{THDN}, the part will enter thermal shutdown, TWRN_B will pull down

continuously and both MOSFETs will turn off. Once the temperature falls, T_{THDN_HYS} below T_{THDN}, the part will resume normal operation.

When multiple DrMOS in a system declare TWARN at once, the duty cycle on the pin will show overlays of low pulses.

A 1 kΩ pull−up resistor is recommended on TWARN pin for ADAS systems using 6 or more DrMOS devices. For systems with less than 6 DrMOS, a 2 kΩ pull−up resistor is sufficient.

Current Sense (ISNS1/2)

NCV81341/P provides a current sense output for each channel to the NCV81341 to use for the regulation loop and over current protection. The NCV81341/P measures the current in the high and low side MOSFET and provides a proportional buffered current to its corresponding ISNSx output. This corresponds to a 20 uA/A relationship for High Side and for Low Side. Positive current sources from the ISNSx pin and negative current sinks into the ISNSx pin. To minimize noise spikes during switching, the current at the peak and trough is sampled and held for t_{HOLD_ISNS}. There is also a propagation delay time of t_{DELAY_ISNS} between inductor current and ISNSx current.

ISNS signals are sensitive and subject to noise injection. They are recommended to be routed in parallel and surrounded by Ground planes. In addition, a 220 pF filtering capacitor is recommended to be connected per each ISNS signal to Ground (location: closer to NCV81340). For further detail please refer to NCV81341 – ADAS DrMOS Layout Guidelines.

As a safety feature, NCV81341 monitors ISNSx pins to verify if the pins are out range. When ISNSx pins are outside of the 0.9 V – 2.1 V range, the DrMOS will pull TWRN pin low. The device will continue to switch regularly, while NCV81340 (ADAS PMIC) will detect this as a fault.

Overcurrent Protection (OCP)

NCV81341 provides an onboard cycle−by−cycle short circuit protection which monitors the peak current in the high−side and low−side MOSFETs and stops switching if it exceeds I_{OCP}. PWM High pulses will be shortened on a cycle by cycle basis until the internal PWM pulse width reduces to the 50 ns leading edge blanking timer for the high−side and 150 ns for the low−side. Both FET's latch off after eight consecutive HS I_{OCP} events that are longer than the 50 ns blanking and the ISNS pin output is forced high. The input voltage (VCCA/VCCP) must be cycled or EN toggled to restart switching.

NCV81341 looks for 8 consecutive counts of cycle−by−cycle HS OCP to capture OCP events. If during a switch cycle an OCP event is detected, the count is incremented. If no OCP event is detected, then the count is reset.

Figure 5 below shows a block diagram of the OCP circuit.

Configurations

There are two configurations for the ADAS DrMOS: NCV81341 and NCV81341P. NCV81341 is configured as two independent channels (single phase mode) while NCV81341P is configured as one paralleled channel (parallel mode). Each configuration has a different part number.

In single mode, both PWM1/2 inputs are used to drive each channel and both ISNS outputs send current sense signals back to the NCV81340. In parallel mode, only PWM1 is used as an input. PWM2 should be left floating or set to tristate. ISNS1/2 should be tied together to sum the current sense signals before sending to the NCV81340.

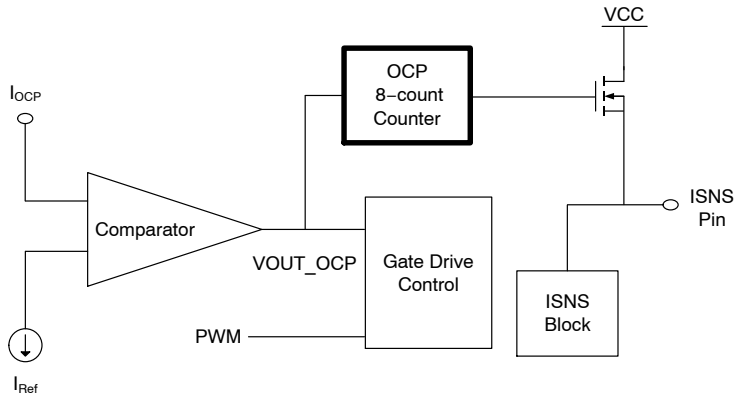
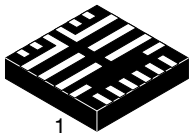


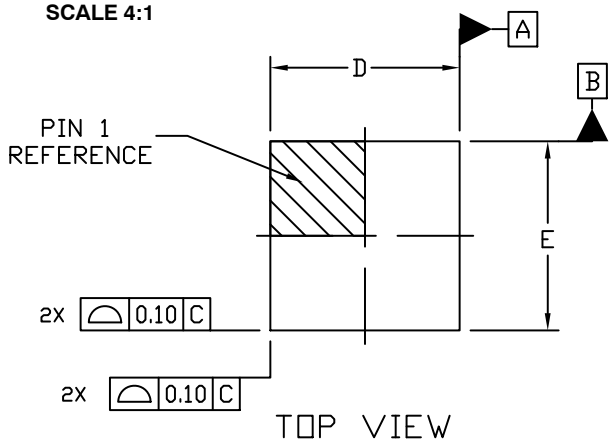
Figure 5. OCP Circuit Block Diagram

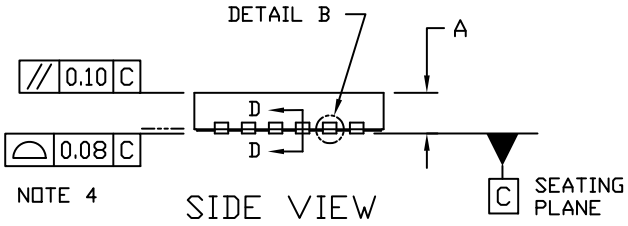


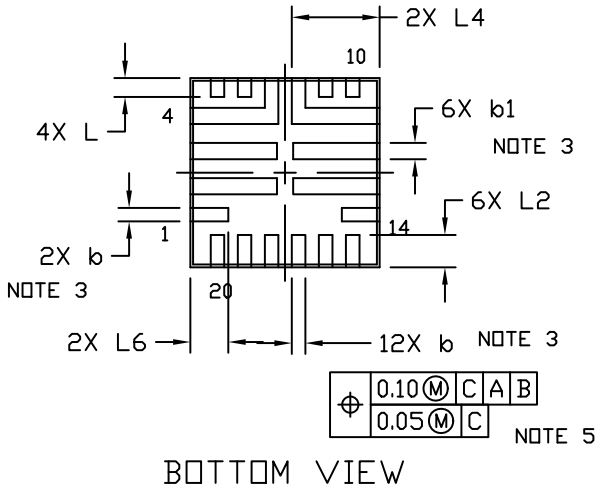
SCALE 4:1

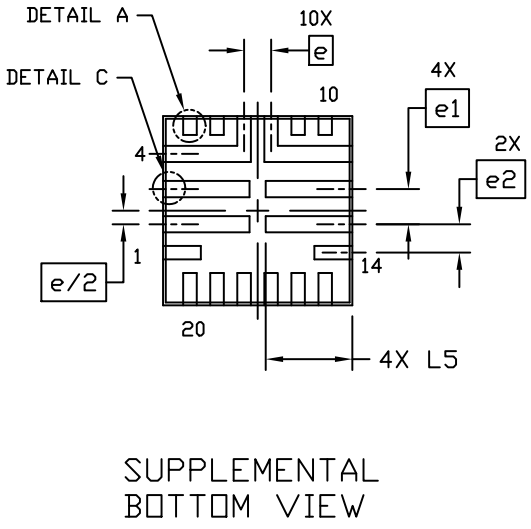
WQFNW20 3.5x3.5
CASE 512AB
ISSUE A

DATE 06 OCT 2017







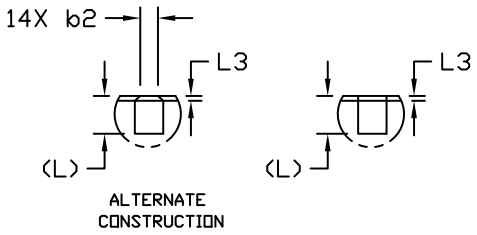


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINAL AND ARE MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO ALL OF THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL OF THE TERMINALS.

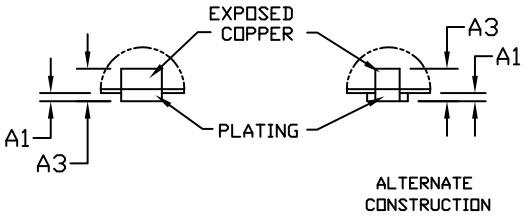
	MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.20	0.25	0.30
b1	0.25	0.30	0.35
b2		0.15 REF	
b3		0.18 REF	
D	3.40	3.50	3.60
E	3.40	3.50	3.60
e		0.50 BSC	
e1		0.65 BSC	
e2		0.525 BSC	
L	0.30	0.35	0.40
L2	0.55	0.60	0.65
L3	0.01	0.05	0.09
L4	1.525	1.625	1.725
L5	1.50	1.60	1.70
L6	0.60	0.70	0.80

WQFNW20 3.5x3.5
CASE 512AB
ISSUE A

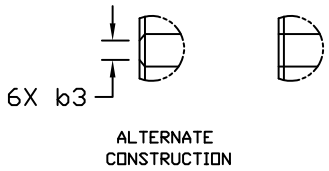
DATE 06 OCT 2017



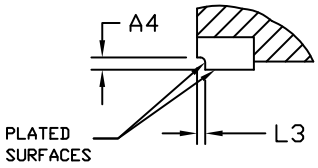
DETAIL A



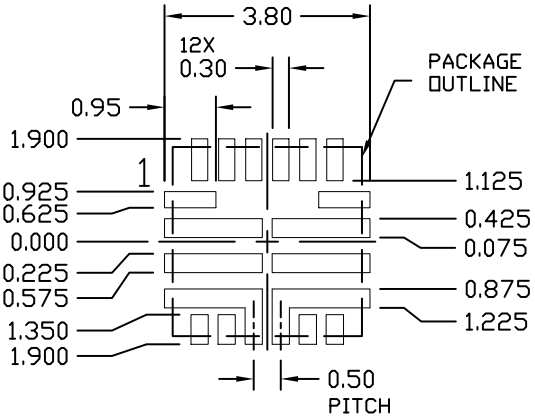
DETAIL B



DETAIL C



SECTION D-D



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*

XXXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WQFNW20 3.5 X 3.5**		**PAGE 2 OF 2**

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