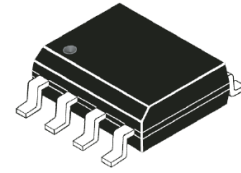


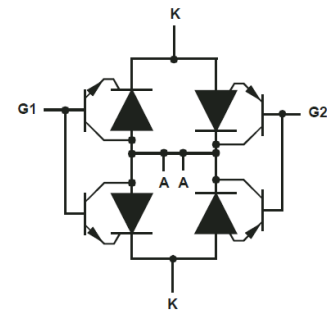
Description

This device is especially designed to protect modern dual polarity supply rail ringing SLICs against overvoltages on the telephone line. Overvoltages can be caused by lightning, a.c. power contact and induction. Four separate protection structures are used; two positive and two negative to provide optimum protection during Metallic (Differential) and Longitudinal (Common Mode) protection conditions in both polarities. Dynamic protection performance is specified under typical international surge waveforms from Telcordia GR-1089-CORE, ITU-T K.44 and YD/T 950.

SLIC Battery supplies respectively. This creates a protector operating at typically +1.4 V above $+V_{(BAT)}$ and -1.4 V below $-V_{(BAT)}$ under a.c. power induction and power contact conditions. The protector gate circuitry incorporates 4 separate buffer transistors designed to provide independent control for each protection element. The gate buffer transistors minimize supply regulation issues by reducing the gate current drawn to around 5 mA, while the high voltage base emitter structures eliminate the need for expensive reverse bias protection gate diodes.



SOP-8EIAJ



Schematic Diagram

Features

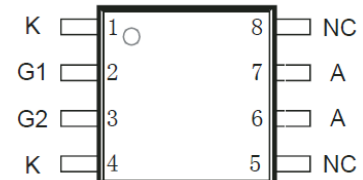
- High performance protection for SLICs with +ve and -ve battery supplies
- Wide -110V to +110V programming range
- Low gate triggering current
- ESD Immunity(HBM): JESD22 Class 3B, $\geq 8\text{KV}$
- MLS: Lever 1 - unlimited

Applications

- Wireless local loop
- Access equipment
- Regenerated POTS
- VoIP applications

Pin Configuration

Pin #	Pin Name	Description
1, 4	K	Connect to subscriber lines (Tip or Ring)
2	G1	Connect to battery ($-V_{(BAT)}$)
3	G2	Connect to battery ($+V_{(BAT)}$)
6, 7	A	Connect ground
5, 8	NC	Not connected



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Parameter	Symbol	Value	Unit
Repetitive peak off-state voltage $V_{G1(\text{Line})} = 0, V_{G2} \geq +5\text{ V}$ $V_{G2(\text{Line})} = 0, V_{G1} \geq -5\text{ V}$	V_{DRM}	-120 +120	V
Non-repetitive peak impulse current (see Notes 1, 2, 3 and 4) 2/10 μs (Telcordia GR-1089-CORE) 5/310 μs (ITU-T K.20, K.21 & K.45, K.44 open-circuit voltage wave shape 10/700 μs) 10/1000 μs (Telcordia GR-1089-CORE)	I_{PPSM}	± 100 ± 45 ± 30	A
Non repetitive peak on-state current, 50Hz / 60Hz (see Notes 1, 2, 3 and 5) 0.2s 1s 900s	I_{TSM}	9.0 5.0 1.7	A

Programmable Overvoltage Protector

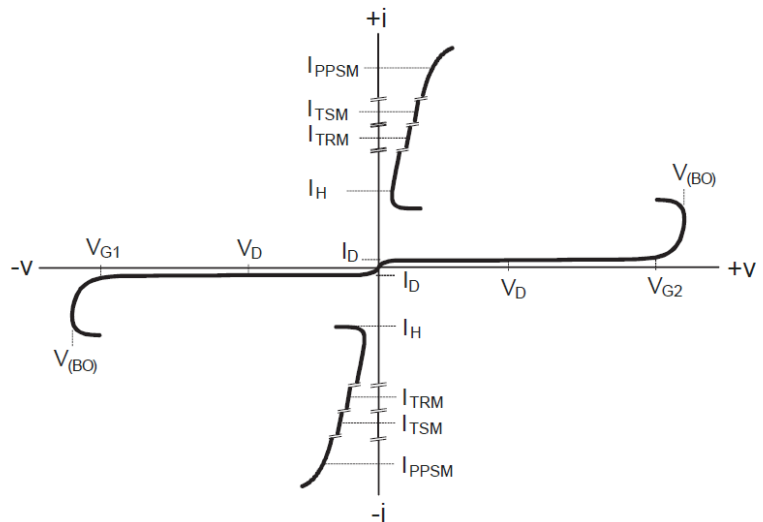
Maximum negative battery supply voltage	V_{G1M}	-110	V
Maximum positive battery supply voltage	V_{G2M}	+110	V
Maximum differential battery supply voltage	$\Delta V_{(BAT)M}$	220	V
Storage temperature range	T_{STG}	-40-150	°C
Junction temperature	T_J	-40-150	°C
Maximum lead temperature for soldering during 10s	T_L	260	°C
Storage temperature range	T_{stg}	-65-150	°C
Junction to ambient thermal resistance	$R_{\theta JA}$	55	°C /W

NOTES:

- Initially the device must be in thermal equilibrium with $T_J = 25^\circ \text{C}$. The surge may be repeated after the device returns to its initial conditions.
- The rated current values may be applied to either of the Line to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of a single terminal pair).
- Rated currents only apply if pins 6 & 7 (Ground) are connected together.
- Applies for the following bias conditions: $V_{G1} = -20 \text{ V to } -110 \text{ V}$, $V_{G2} = 0 \text{ V to } +110 \text{ V}$.
- EIA/JESD51-2 environment and EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.

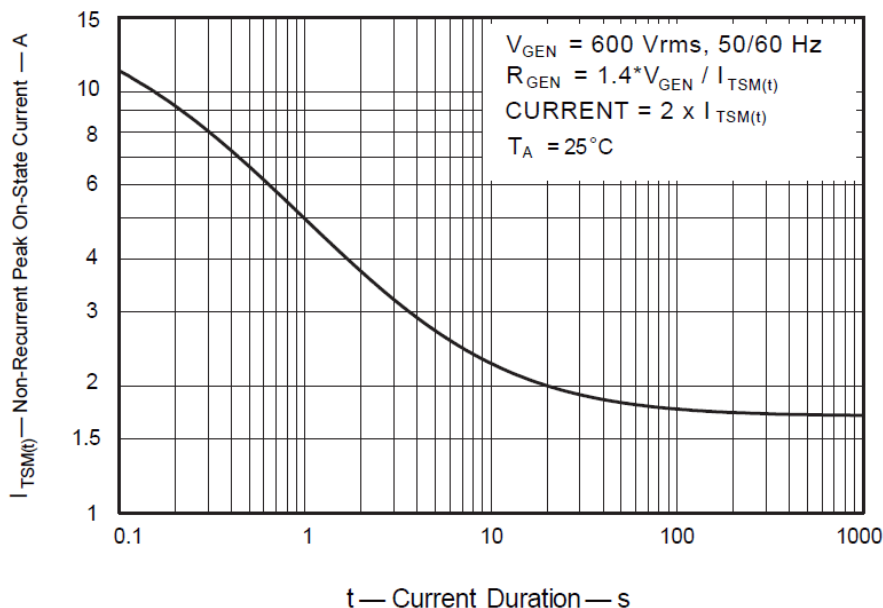
Parameter Measurement Information

Parameter	Symbol
Off-state current	I_D
Holding current	I_H
Non-repetitive peak impulse current	I_{PPSM}
Non repetitive peak on-state current	I_{TSM}
Breakover voltage	$V_{(BO)}$
Gate-Line impulse breakover voltage	V_G
Line-ground off-state capacitance	C_0



Electrical Characteristics for any Section ($T_A = 25^\circ \text{C}$)

Non-Repetitive Peak On-state Current against Duration

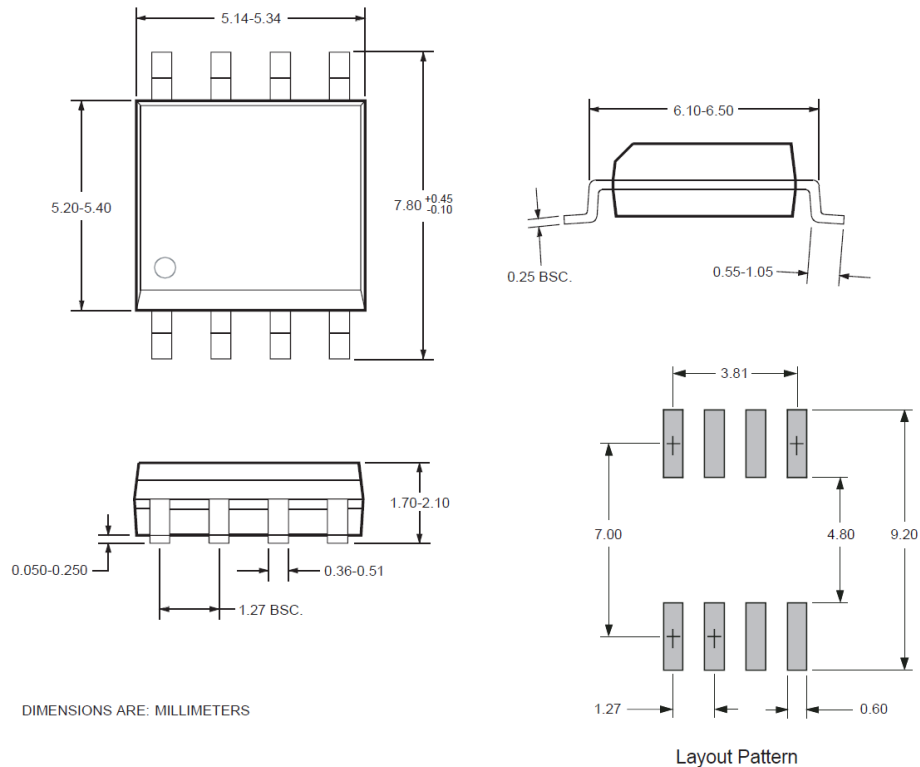


Symbol	Test Conditions	Min.	Typ.	Max.	Unit
I_D Off-state current	$V_D=V_{DRM}$, $V_{G1(Line)} = 0$, $V_{G2} \geq +5V$ $T_A=25^\circ C$ $T_A=85^\circ C$ $V_D=V_{DRM}$, $V_{G1(Line)} = 0$, $V_{G2} \geq +5V$ $T_A=25^\circ C$ $T_A=85^\circ C$			-5 -50 +5 +50	μA
$I_{G1(Line)}$ Negative-gate Leakage current	$V_{G1(Line)} = -220V$			-5	μA
$I_{G2(Line)}$ Positive-gate Leakage current	$V_{G2(Line)} = +220V$			+5	μA
$V_{G1L(BO)}$ Gate-Line impulse breakover voltage	$V_{G1}=-100V$, $I_T=-100A$ (see Note 6) $2/10\mu s$ $V_{G1}=-100V$, $I_T=-100A$ $10/100\mu s$			-15 -11	V
$V_{G2L(BO)}$ Gate-Line impulse breakover voltage	$V_{G2}=+100V$, $I_T=+100A$ (see Note 6) $2/10\mu s$ $V_{G2}=+100V$, $I_T=+100A$ $10/100\mu s$			+15 +11	V
I_H Negative holding current	$V_{G1}=-60V$, $I_T=-1A$, $di/dt=1A/ms$	-150			mA
I_{G1T} Negative-gate trigger current	$I_T=-5A$, $t_{p(g)} \geq 20\mu s$, $V_{G1}=-60V$			+5	mA
I_{G2T} Positive-gate trigger current	$I_T=+5A$, $t_{p(g)} \geq 20\mu s$, $V_{G2}=+60V$			+5	mA
C_O Line-ground off-state capacitance	$f=1MHz$, $V_D=-3V$, G1 & G2 open circuit			110	pF

NOTE:

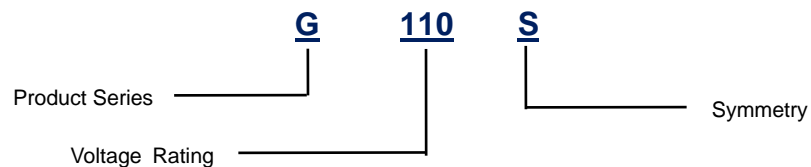
6. Voltage measurements should be made with an oscilloscope with limited bandwidth (20 MHz) to avoid high frequency noise.

Product Dimension



Marking and Order Information

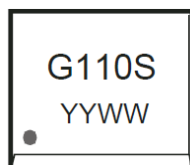
Part Number System



Order Information

Device	Package	Net Weight	Carrier	Quantity	HSF Status
G110S	SOP-8EIAJ	0.135	Tape & Reel	2,000pcs/reel	RoHS compliant

Marking



YYWW = Date Code

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