

Description

The SXJ50N65MP protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. They feature large cross-sectional area junctions for conducting high transient currents, offer desirable electrical characteristics for board level protection, such as fast response time, low operating voltage. It gives designer the flexibility to protect one bi-directional line in applications where arrays are not practical.

General Features

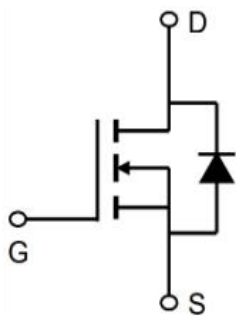
$V_{DS} = 650V$ (Type: 740V) $IDM = 50A$

$R_{DS(ON)} < 190m\Omega$ @ $V_{GS} = 10V$

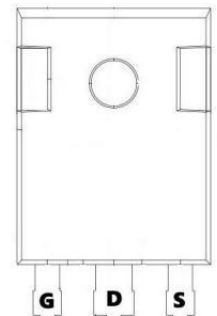
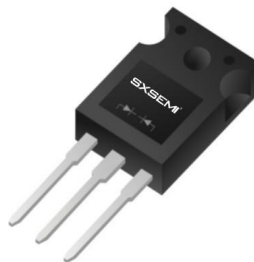
Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



TO-247-3L



Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage ($V_{GS} = 0V$)	650	V
I_D	Continuous Drain Current	21	A
I_{DM}	Pulsed Drain Current (note1)	50	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	500	mJ
P_D	Power Dissipation ($T_c = 25^\circ C$)	151	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	$-55 \sim +150$	$^\circ C$
R_{thJC}	Thermal Resistance, Junction-to-Case	0.82	$^\circ C/W$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	62	$^\circ C/W$

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain to source breakdown voltage	V _{GS} =0V, I _D =250uA	650	740	--	V
ΔBV _{DSS} / ΔT _J	Breakdown voltage temperature coefficient	I _D =250uA, referenced to 25°C	--	0.7	--	V/°C
IDSS	Drain to source leakage current	V _{DS} =650V, V _{GS} =0V	--	--	1	uA
		V _{DS} =520V, T _C =125°C	--	--	50	uA
IGSS	Gate to source leakage current, forward	V _{GS} =30V, V _{DS} =0V	--	--	100	nA
	Gate to source leakage current, reverse	V _{GS} =-30V, V _{DS} =0V	--	--	-100	nA
VGS(TH)	Gate threshold voltage	V _{DS} =V _{GS} , I _D =250uA	2.5	3.3	4.5	V
RDS(ON)	Drain to source on state resistance	V _{GS} =10V, I _D =3.2A	--	150	190	mΩ
Ciss	Input capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz	--	1510	--	pF
Coss	Output capacitance		--	65	--	
Crss	Reverse transfer capacitance		--	2.4	--	
td(on)	Turn on delay time	V _{DS} =400V, I _D =13A, R _G =4.7Ω , V _{GS} =13V	--	10	--	ns
tr	Rising time		--	19.8	--	
td(off)	Turn off delay time		--	45.4	--	
tf	Fall time		--	41.4	--	
Qg	Total gate charge	V _{DS} =480V, V _{GS} =10V, I _D =11A	--	7.27	--	nC
Qgs	Gate-source charge		--	17.4	--	
Qgd	Gate-drain charge		--	43.9	--	
IS	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	--	--	21	A
ISM	Pulsed source current		--	--	63	A
VSD	Diode forward voltage drop.	I _S =7.3A, V _{GS} =0V	--	0.812	1.5	V
Trr	Reverse recovery time	I _S =11A, V _{GS} =0V, V _{DD} =400V, dI _F /dt=100A/us,	--	288	--	ns
Qrr	Reverse recovery Charge		--	3.66	--	uC

Note :

- 1、The data tested by surface mounted on a 1 inch2 FR-4 board with 20Z copper.
- 2、The EAS data shows Max. rating . L=0.5mH, IAS =7A, VDD =50V, RG=25Ω
- 3、The test condition is Pulse Test: ISD ≤ ID, di/dt = 100A/us, VDD≤ BVDSS, Starting at TJ =25°C
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

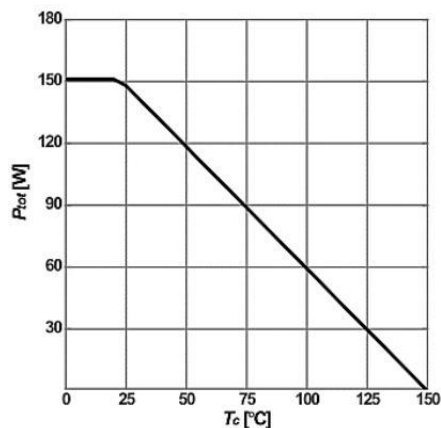


Figure1: Power dissipation (Non FullPAK)

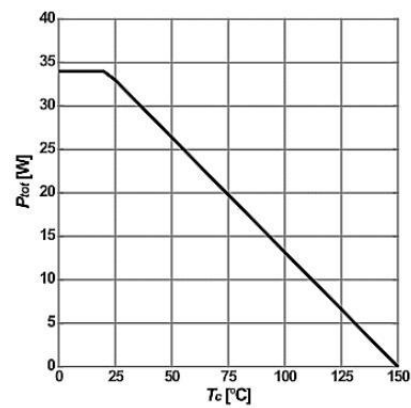


Figure2: Power dissipation (FullPAK)

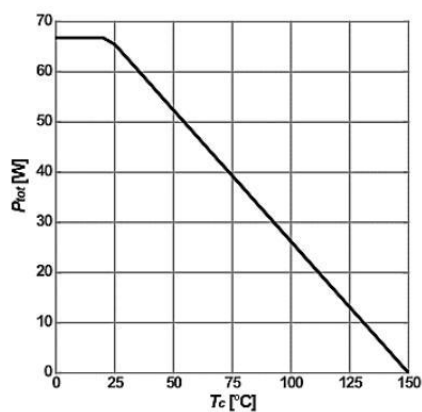


Figure3: Power dissipation
 $P_{tot}=f(T_c)$

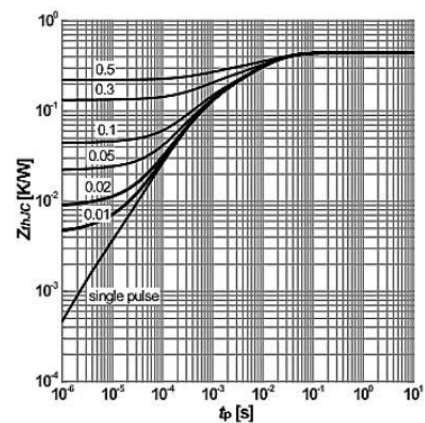


Figure4: Max. transient thermal impedance
 $Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

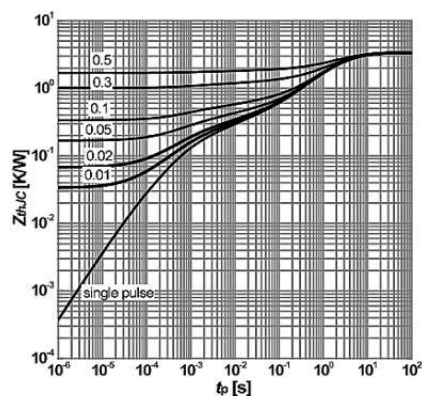


Figure5: Max. transient thermal impedance
 $Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

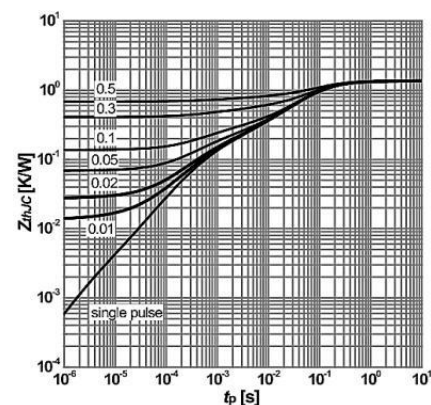


Figure6: Max. transient thermal impedance
 $Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Typical Characteristics

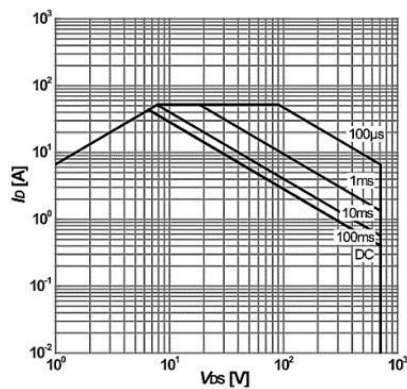


Figure 7: Safe operating area (Non FullPAK)

$I_D = f(V_{DS}); T = 25^\circ\text{C}; D = 0; \text{parameter: } t$

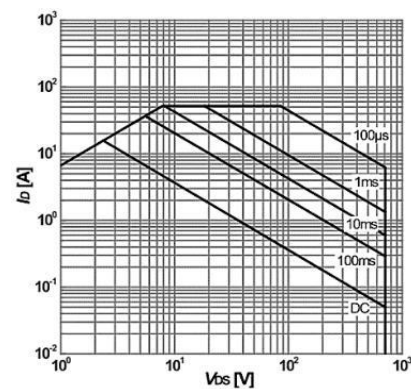


Figure 8: Safe operating area (Non FullPAK)

$I_D = f(V_{DS}); T = 25^\circ\text{C}; D = 0; \text{parameter: } t$

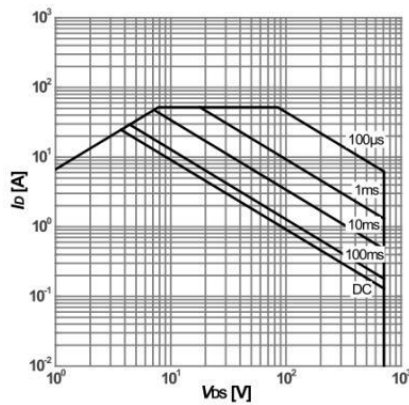


Figure 9: TSafe operating area (FullPAK-TO220A)

$R_{DS(on)} = f(I_D); T = 25^\circ\text{C}; \text{parameter: } V_{DS}$

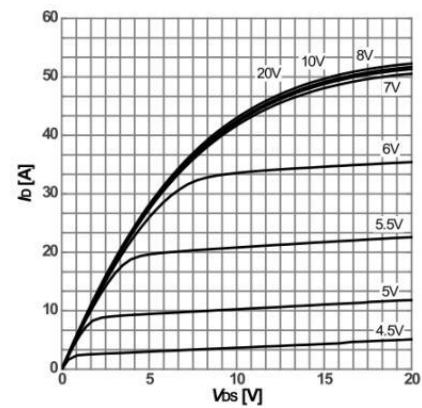


Figure 10: Typ. output characteristics

$R_{DS(on)} = f(T); I_D = 3.2\text{A}; V_{GS} = 10\text{V}$

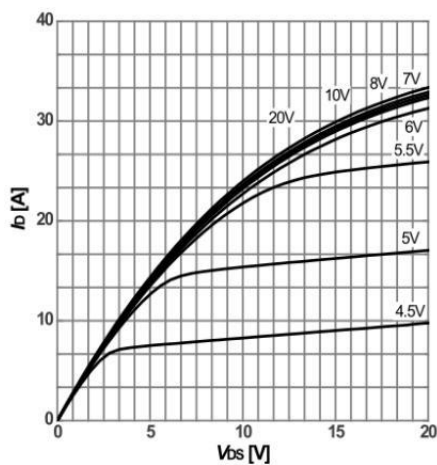


Figure 11: Typ. output characteristics

$I_D = f(V_{DS}); T = 125^\circ\text{C}; \text{parameter: } V_{GS}$

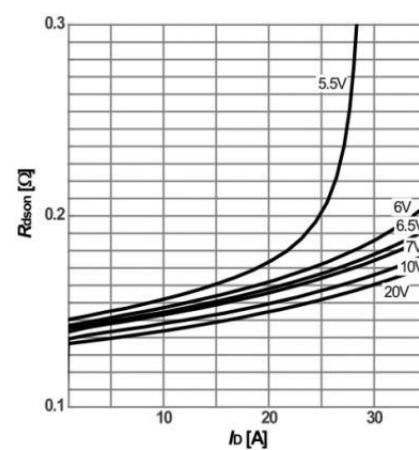
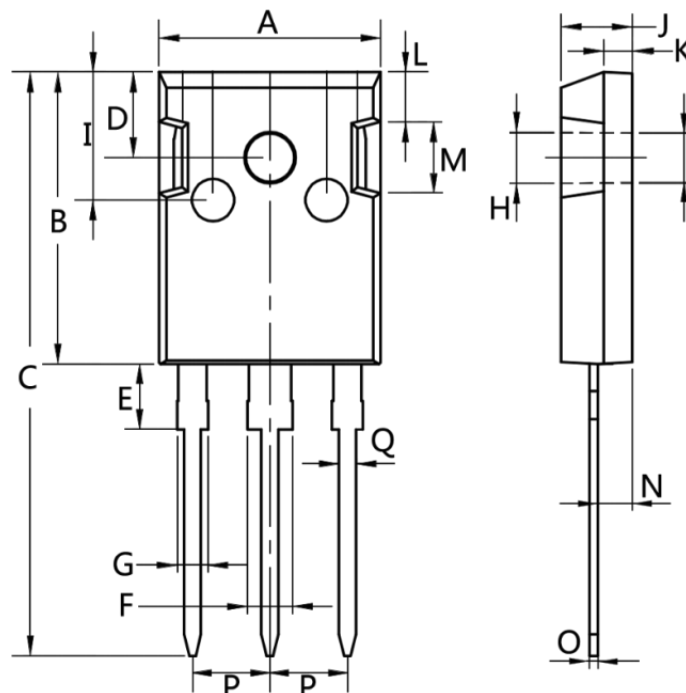


Figure 12: Type. gate charge

$R_{DS(on)} = f(I_D); T = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Package Mechanical Data-TO-247-3L


Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	TO-247-3L		330