

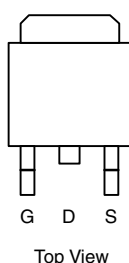
IRF640NSTRL-VB Datasheet

N-Channel 200 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
200	0.048 at $V_{GS} = 10$ V	40
	0.060 at $V_{GS} = 6.5$ V	35

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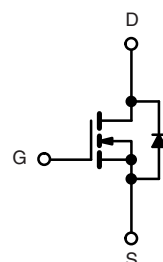
FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- Low Thermal Resistance Package
- PWM Optimized for Fast Switching
- Compliant to RoHS Directive 2002/95/EC


RoHS
 COMPLIANT

APPLICATIONS

- Isolated DC/DC Converters
- Primary-Side Switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	40	A
		25	
Pulsed Drain Current	I_{DM}	80	
Avalanche Current	I_{AR}	20	mJ
Repetitive Avalanche Energy ^a	E_{AR}	16.2	
Maximum Power Dissipation ^a	P_D	200 ^b	W
		4.5	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R_{thJA}	40	°C/W
Junction-to-Case (Drain)	R_{thJC}	1	

Notes:

a. Duty cycle ≤ 1 %.

b. See SOA curve for voltage derating.

c. When mounted on 1" square PCB (FR-4 material).

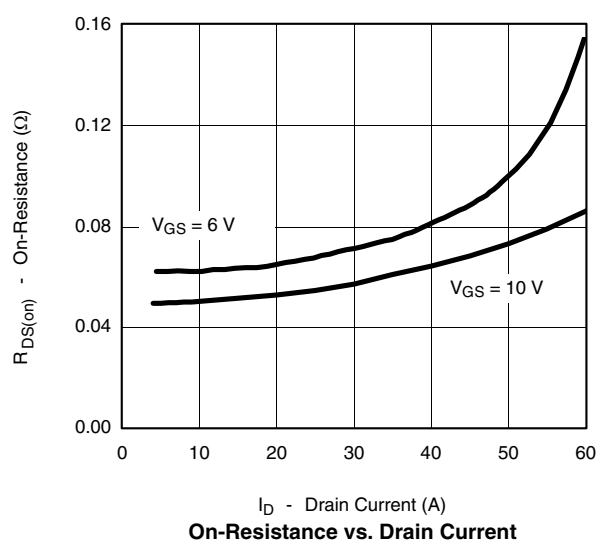
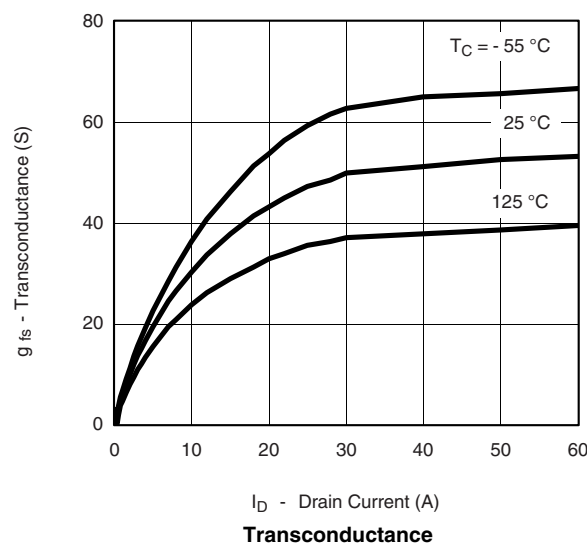
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min .	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	200			V
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2		4	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 160 V, V _{GS} = 0 V			1	μA
		V _{DS} = 160 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 160 V, V _{GS} = 0 V, T _J = 175 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 15 V, V _{GS} = 10 V	60			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.048		Ω
		V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C		0.150		
		V _{GS} = 10 V, I _D = 20 A, T _J = 175 °C		0.180		
Drain-Source on State Resistance		V _{GS} = 6.5 V, I _D = 15 A		0.060		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 30 A	15			S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		2820		pF
Output Capacitance	C _{oss}			300		
Reverse Transfer Capacitance	C _{rss}			120		
Total Gate Charge ^c	Q _g	V _{DS} = 100 V, V _{GS} = 10 V, I _D = 20 A		35		nC
Gate-Source Charge ^c	Q _{gs}			11		
Gate-Drain Charge ^c	Q _{gd}			14		
Gate Resistance	R _G			2		Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 100 V, R _L = 5 Ω I _D ≅ 20 A, V _{GEN} = 10 V, R _G = 2.5 Ω		15	25	ns
Rise Time ^c	t _r			35	55	
Turn-Off Delay Time ^c	t _{d(off)}			40	60	
Fall Time ^c	t _f			30	45	
Source-Drain Diode Ratings and Characteristics (T _C = 25 °C) ^b						
Continuous Current	I _S				40	A
Pulsed Current	I _{SM}				60	
Forward Voltage ^a	V _{SD}	I _F = 20 A, V _{GS} = 0 V		1	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 50 A, dl/dt = 100 A/μs		115	170	ns
Peak Reverse Recovery Charge	I _{RM(REC)}			7.5	12	A
Reverse Recovery Charge	Q _{rr}			0.43	1.02	μC

Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

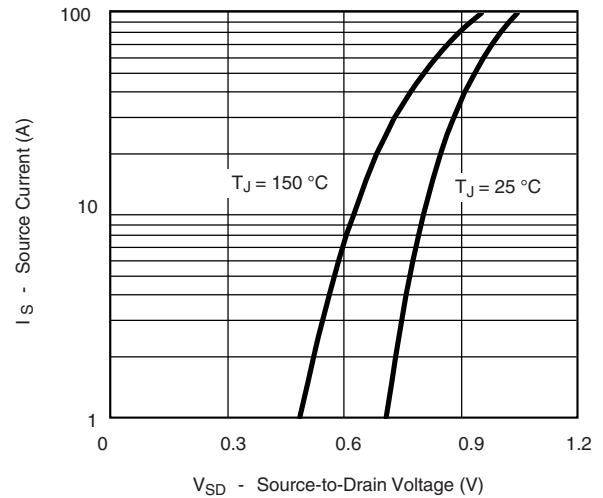
TYPICAL CHARACTERISTICS (25 °C unless noted)



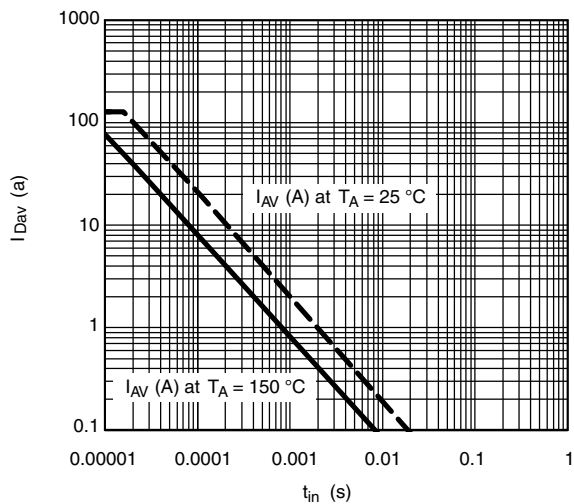
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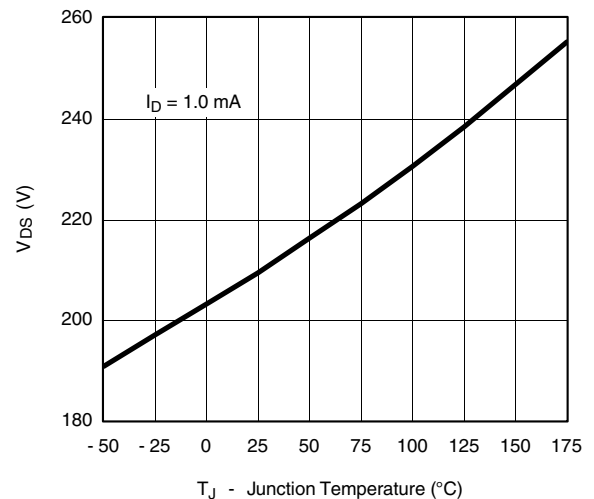
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

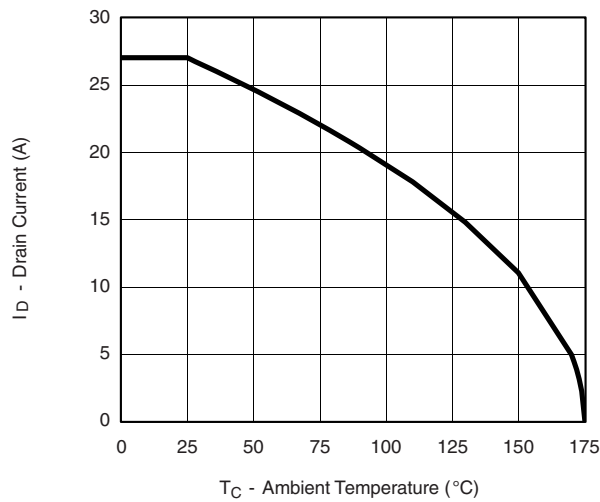


Avalanche Current vs. Time



Drain Source Breakdown vs. Junction Temperature

THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

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