



QPL6220Q Datasheet 0.1 – 6GHz Ultra Low-Noise LNA

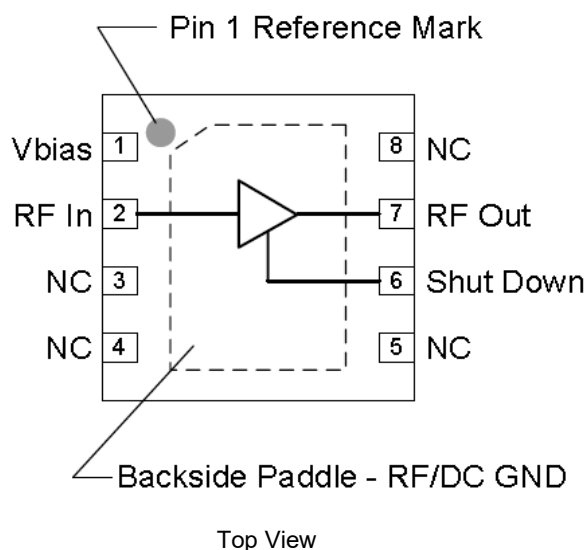
Product Overview

The QPL6220Q is a high-linearity, ultra-low-noise amplifier in a small 2 x 2 mm surface-mount package. At 2.33GHz, the amplifier typically provides 17.5dB gain, +38dBm OIP3 at a 65mA bias setting, and 0.38dB noise figure. The LNA can be biased from a single positive supply ranging from 3.3 to 5.25V.

The QPL6220Q is bias adjustable and requires minimal external components to operate. The LNA also has integrated power down control capability for TDD applications.

The QPL6220Q architecture and interface are ideal for next generation Automotive wireless solutions and to support the extended temperature requirements and lifetime of Automotive applications.

Functional Block Diagram



8 Pin 2X2 mm DFN Package

Key Features

- Qualified to AEC-Q100 Grade 2
- 0.1-6 GHz Operational Bandwidth
- Ultra-low 0.38 dB NF @ 2.33 GHz
- 38 dBm OIP3
- 17.5 dB small signal gain
- Bias adjustable for linearity optimization
- Unconditionally stable
- Shut-down mode pin with 1.8V logic
- Maintains OFF state with high Pin drive

Applications

- SDARS Active Antenna
- Automotive C-V2X Applications
- Automotive Infotainment
- Automotive Telematics
- TDD or FDD systems
- Other Automotive Applications

Ordering Information

Part No.	Description
QPL6220QSB	5pc sample bag
QPL6220QSQ	25pc sample bag
QPL6220QSR	Standard 100-piece reel
QPL6220QEVb	Evaluation Board
QPL6220QTR7	2500 pieces on a 7" reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150°C
Supply Voltage (V _{DD})	7 V
RF Input Power, CW, 50Ω, T=25°C	22 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Operating above recommended condition up to and including Absolute Maximum Ratings conditions may reduce device reliability. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V _{DD})	+3.3	+5	+5.25	V
T _{AMBIENT} ⁽¹⁾	-40		+105	°C
T _j for >10 ⁶ hours MTTF			190	°C

¹Case temperature allows 10°C max rise over Ambient Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions ^(1,2)	Min	Typ	Max	Units
Operational Frequency Range		100		6000	MHz
Test Frequency			2330		MHz
Gain		16.3	17.5	18.8	dB
Input Return Loss			12		dB
Output Return Loss			12		dB
Noise Figure ⁽³⁾			0.38	0.52	dB
Output P1dB		+21	+22.5		dBm
Output IP3	P _{out} =+2 dBm/tone, Δf=1 MHz	+32	+38		dBm
Power Shutdown Control (pin 6)	On state	0		0.63	V
	Off state (Power down)	1.17		V _{DD}	V
Current, I _{DD}	On state	50	65	85	mA
	Off state (Power down)		3		mA
Shutdown pin current, I _{SD}	V _{PD} = 1.8 V		150		μA
Switching Time (LNA On)	50% DC to 0.5dB of settled power/gain		100		ns
Switching Time (LNA Off)	50% DC to -20dB from LNA On power/gain		100		ns
Thermal Resistance	Channel to case		74		°C/W

Notes:

- Test conditions unless otherwise noted: V_{DD} = +5.0 V, Temp = +25 °C, 50 Ω system.
- Recommended EVB schematic/layout/BOM/PCB should be followed in order to achieve specified performance.
- Input trace loss de-embedded for NF data.

S-Parameters

Test Conditions: $V_{DD}=+5$ V, $I_{DD}=65$ mA (typ.), $T=+25^{\circ}\text{C}$, unmatched 50 Ω system, calibrated to device leads

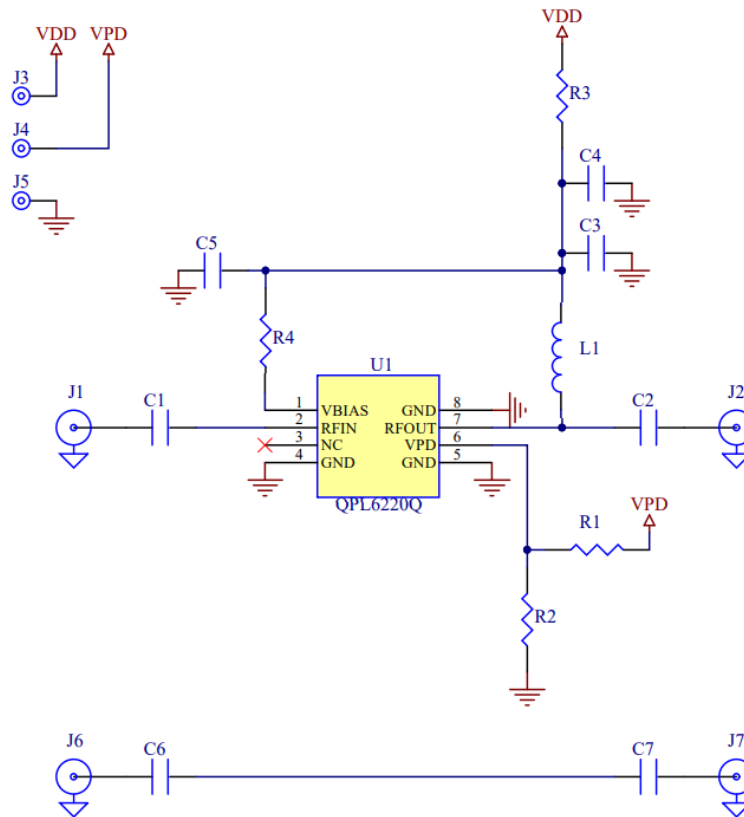
Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
0.7	-7.9	-71	25.8	114	-33.4	32	-10.9	-14
0.9	-9.1	-84	24.5	103	-32.1	34	-10.9	-20
1.1	-10.2	-96	23.3	93	-31.0	35	-11.1	-25
1.3	-11.2	-107	22.2	85	-30.0	35	-11.3	-31
1.5	-12.0	-117	21.2	77	-29.1	34	-11.5	-37
1.7	-12.7	-128	20.3	70	-28.3	32	-11.8	-44
1.9	-13.2	-138	19.5	64	-27.6	30	-12.2	-51
2.1	-13.6	-148	18.8	57	-26.9	27	-12.4	-59
2.3	-13.8	-157	18.1	51	-26.4	25	-12.6	-68
2.5	-14.0	-166	17.5	44	-25.9	22	-12.8	-76
2.6	-14.0	-170	17.2	41	-25.7	20	-12.8	-81
2.7	-14.0	-174	16.9	38	-25.4	19	-12.8	-86
2.9	-13.7	-175	16.4	33	-25.0	16	-13.2	-96
3.1	-13.9	179	15.9	27	-24.6	13	-13.0	-104
3.3	-14.1	174	15.4	21	-24.3	9	-12.7	-112
3.5	-14.4	170	15.0	15	-24.0	6	-12.4	-120
3.7	-14.6	166	14.5	9	-23.7	3	-12.1	-128
3.9	-14.9	162	14.1	4	-23.4	-1	-11.7	-135
4.1	-15.2	158	13.8	-2	-23.2	-4	-11.4	-142
4.3	-15.4	154	13.4	-8	-23.0	-7	-11.1	-149
4.5	-15.6	150	13.0	-14	-22.8	-11	-10.8	-157
4.7	-15.7	146	12.7	-20	-22.6	-15	-10.5	-164
4.9	-15.8	143	12.3	-26	-22.5	-18	-10.2	-172
5.1	-15.8	139	12.0	-32	-22.3	-22	-9.9	179
5.3	-15.7	137	11.6	-38	-22.2	-26	-9.6	171
5.5	-15.6	135	11.2	-45	-22.2	-30	-9.2	163

Noise Parameters

Test Conditions: $V_{DD}=+5$ V, $I_{DD}=65$ mA (typ.), $T=+25^{\circ}\text{C}$, unmatched 50 ohm system, calibrated to device leads

Freq (GHz)	NF _{min} (dB)	GammaOpt (mag)	GammaOpt (deg)	Rn (Ω)
0.6	0.16	0.20	12	2.09
0.7	0.15	0.21	17	1.91
0.8	0.17	0.25	27	1.99
0.9	0.23	0.21	23	2.06
1	0.23	0.18	32	2.01
1.1	0.22	0.17	39	1.93
1.2	0.21	0.15	36	1.97
1.3	0.20	0.15	38	2.06
1.4	0.17	0.15	59	2.05
1.6	0.17	0.13	62	1.83
1.7	0.16	0.13	79	1.71
1.8	0.15	0.11	78	1.79
1.9	0.13	0.14	96	1.65
2	0.11	0.13	103	1.70
2.1	0.15	0.11	109	1.66
2.2	0.17	0.12	127	1.58
2.3	0.18	0.13	141	1.50
2.4	0.21	0.10	143	1.67
2.5	0.23	0.13	160	1.65
2.6	0.25	0.15	159	1.51
2.7	0.27	0.14	165	1.59
2.8	0.28	0.18	173	1.42
2.9	0.27	0.18	178	1.50

Evaluation Board – QPL6220QEVB



Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. R3 (0 Ω jumper) may be replaced with copper trace in the target application layout.
3. All components are of 0402 size.
4. For TDD Applications: R1 = 0 Ω & R2 = 100K
5. For FDD Applications: R2 = 100K 'OR' Pin 6 tied to ground. R1 = DNP/Omitted
6. A through line is included on the evaluation board to de-embed the board losses.
7. R4 sets the current draw. Can be changed for the desired bias point.
8. Do not leave pin 6 floating. It is acceptable to GND pin 6.

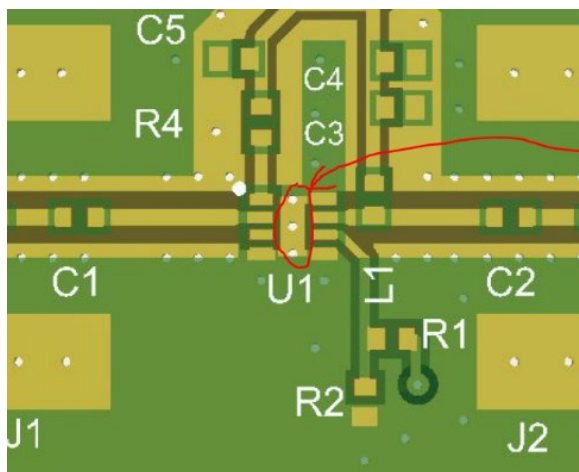
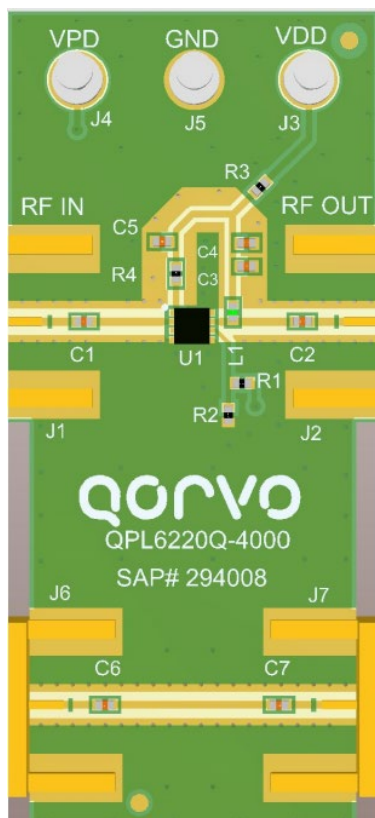
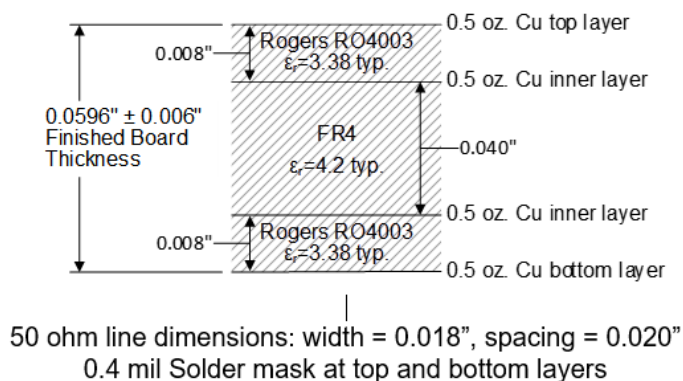
Ref Des	Qty	Material #	Alt Grp	Usage Prob %	Description	Manufacturer	Manufacturer Part #
U1	1	QPL6220QSB			SDARS LNA		
PCB	1	294008			PCB, QPL6220Q	TTM TECHNOLOGIES INC	QPL6220Q-4000 A
C2,C7	2	21925			CAP, 100pF, 5%, 50V, C0G, 0402	MURATA ELECTRONICS SINGAPORE PTE LT	GRM1555C1H101JA01D
C3	1	21930			CAP, 1000pF, 10%, 50V, X7R, 0402	MURATA ELECTRONICS SINGAPORE PTE LT	GRM155R71H102KA01D
C1,C5,C6	3	273962			CAP, 22pF, 2%, 50V, HI-Q, 0402	MURATA ELECTRONICS SINGAPORE PTE LT	GJM1555C1H220GB01D
C4	1	285115			CAP, 1uF, 10%, 10V, X7S, 0402	MURATA ELECTRONICS SINGAPORE PTE LT	GRM155C71A105KE11D
R4	1	010-0401-3321LF			RES, 3.32K OHM, 1%, 0.1W, 0402	Kamaya, Inc	RMC1/16SK3321FTH
R1,R3	2	21592			RES, 0 OHM, 5%, 1/10W, 0402	Kamaya, Inc	RMC1/16SJPTH
R2	1	25111			RES, 100K, 5%, 1/16W, 0402	KOA Speer Electronics, Inc.	RK73B1ETTP104J
L1	1	23847			IND, 18nH, 5%, W/W, 0402	Coilcraft, Inc.	0402CS-18NXJRW
J1,J2,J6,J7	4	1068996			862000-422 CONN .062 RF SMA F STRT FLANG	Cinch Connectivity Solutions, Inc	142-0701-851
J3,J4,J5	3	1068789			862000-055 TERM. SOLDER TURRET .062 PCB	MOUSER ELECTRONICS INC	2533-0-00-44-00-00-07-0

Evaluation Board PCB Information

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Silkscreen Top				
	Soldermask Top	Solder Resist	0.40mil	3.5	
1	Metal 1 Top	Copper	0.70mil		
	Dielectric1	RO4003	8.00mil	3.38	
2	Metal 2	Copper	0.70mil		
	Dielectric 3	FR-4	40.00mil	4.2	
3	Metal 3	Copper	0.70mil		
	Dielectric 2	RO4003	8.00mil	3.38	
4	Metal 4 Bottom	Copper	0.70mil		
	Soldermask Bottom	Solder Resist	0.40mil	3.5	

Total Thickness: 59.6mil

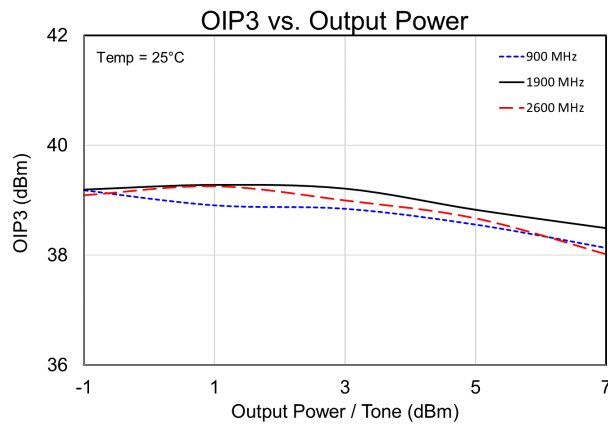
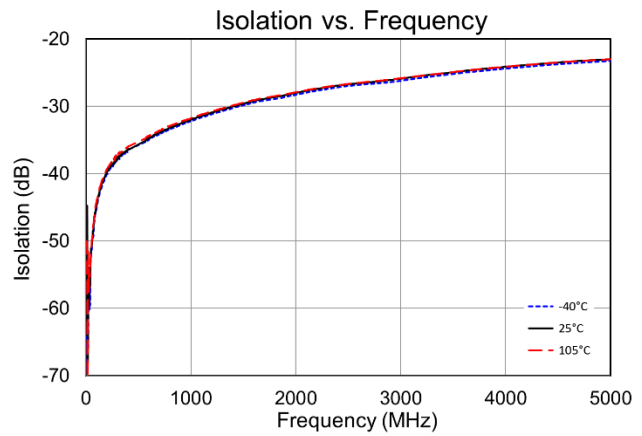
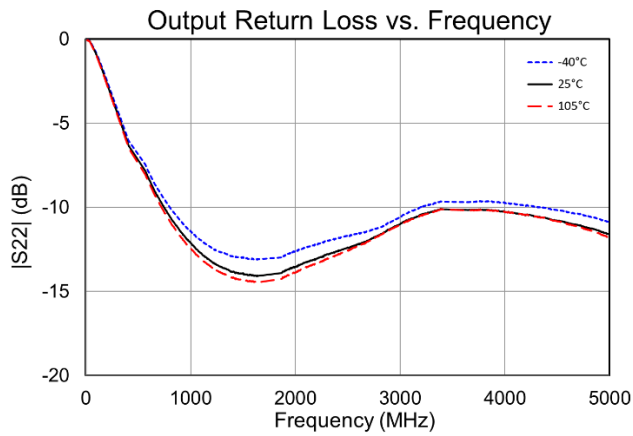
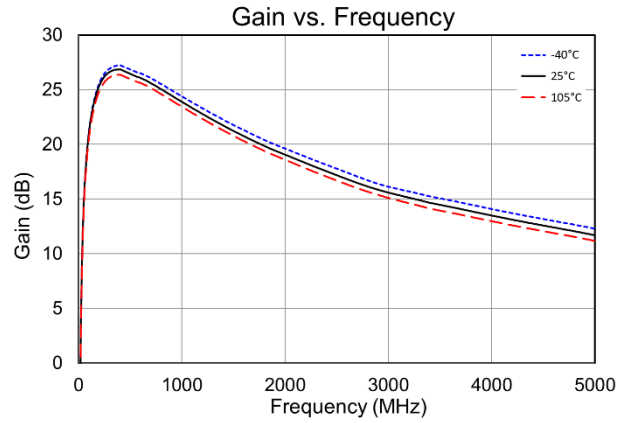
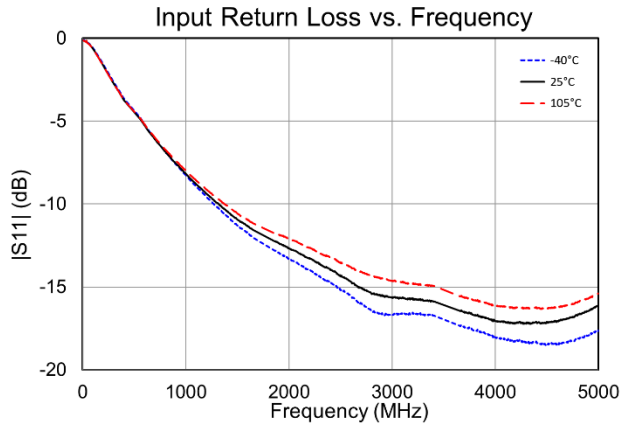
Qorvo PCB Material and Stack-up



3 Vias under DUT for thermal transfer

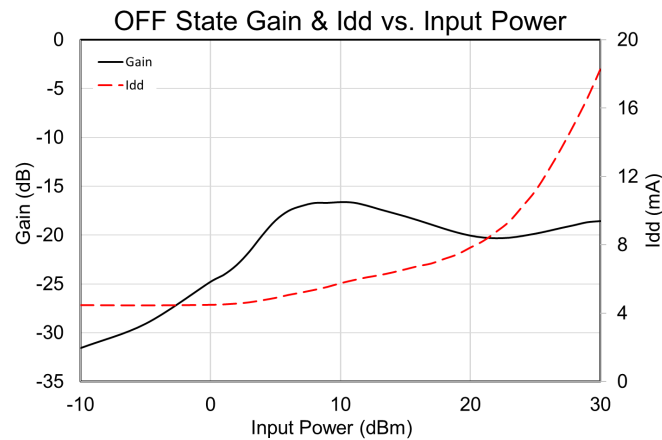
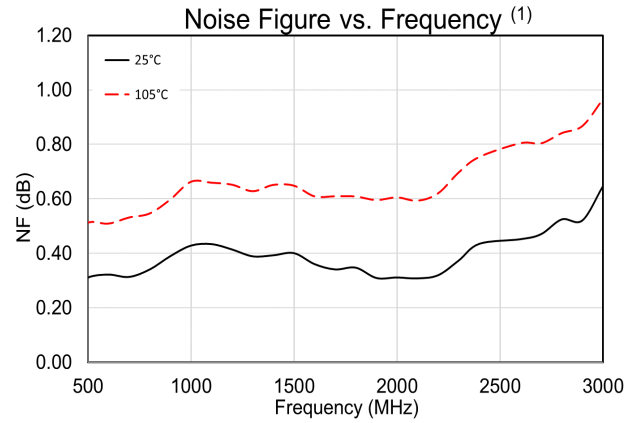
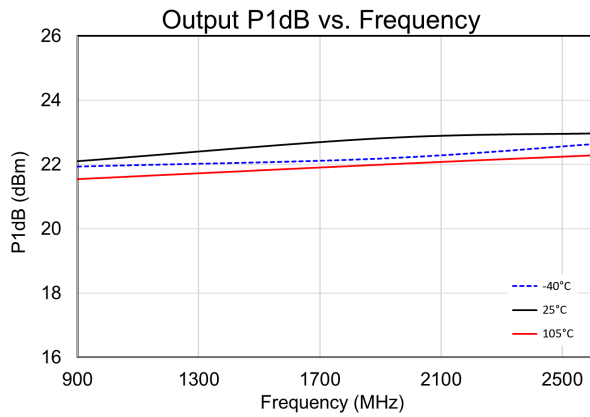
Performance Plots – QPL6220QEVB

Test conditions unless otherwise noted: $V_{DD} = +5\text{ V}$, $I_{DD} = 65\text{ mA}$.

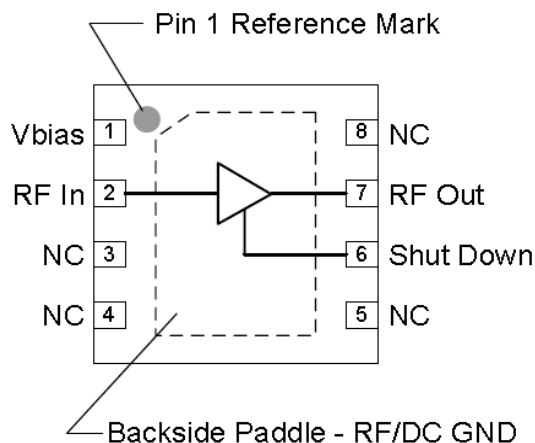


Performance Plots – QPL6220Q EVB Continued

Test conditions unless otherwise noted: $V_{DD} = +5\text{ V}$, $I_{DD} = 65\text{ mA}$.



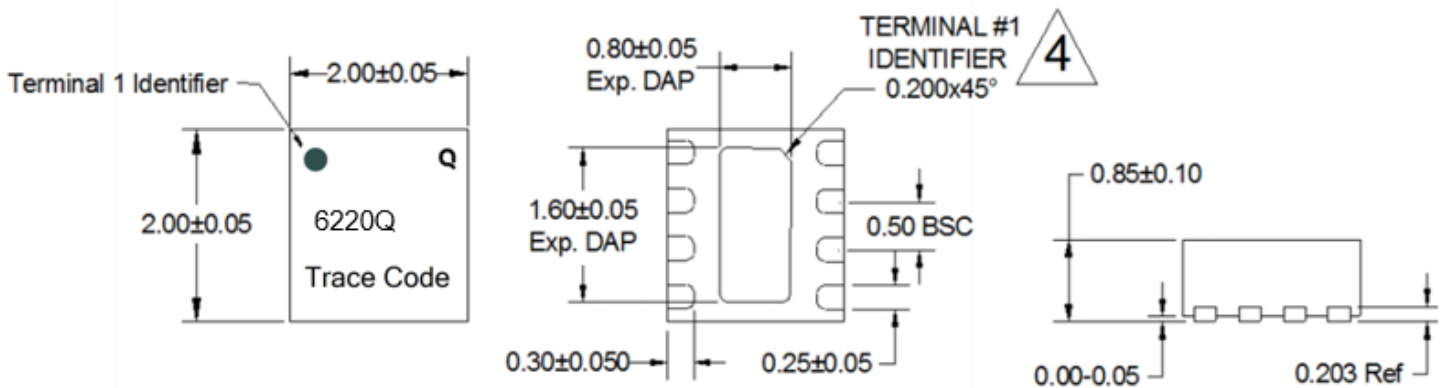
Pad Configuration and Description



Pad No.	Label	Description
1	V _{bias}	Sets the LNA bias current for the device.
2	RF In	RF Input pin internally matched to 50 ohms. A DC block is required.
6	Shut Down	A high voltage (>1.17V) turns off the device. If the pin is pulled to ground or driven with a voltage less than 0.63V, then the device will operate under LNA ON state. Do not leave the pin floating, it is acceptable to GND the pin 6.
7	RF Out	RF Output pin internally matched to 50 ohms. A DC block is required. V _{DD} supply pin.
3, 4, 5, 8	NC	Not connected internally. This pin may be left floating or connected to ground.
Backside Paddle	RF/DC GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB vias under the device are recommended.

Package Marking and Dimensions

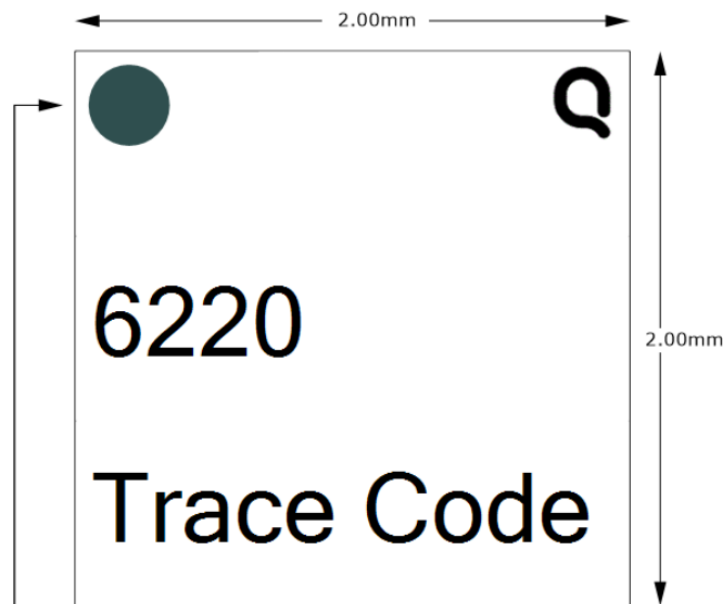
Marking: Part Number – 6220Q
Trace Code – XXXX up to 4 Characters assigned by sub-contractor



Notes:

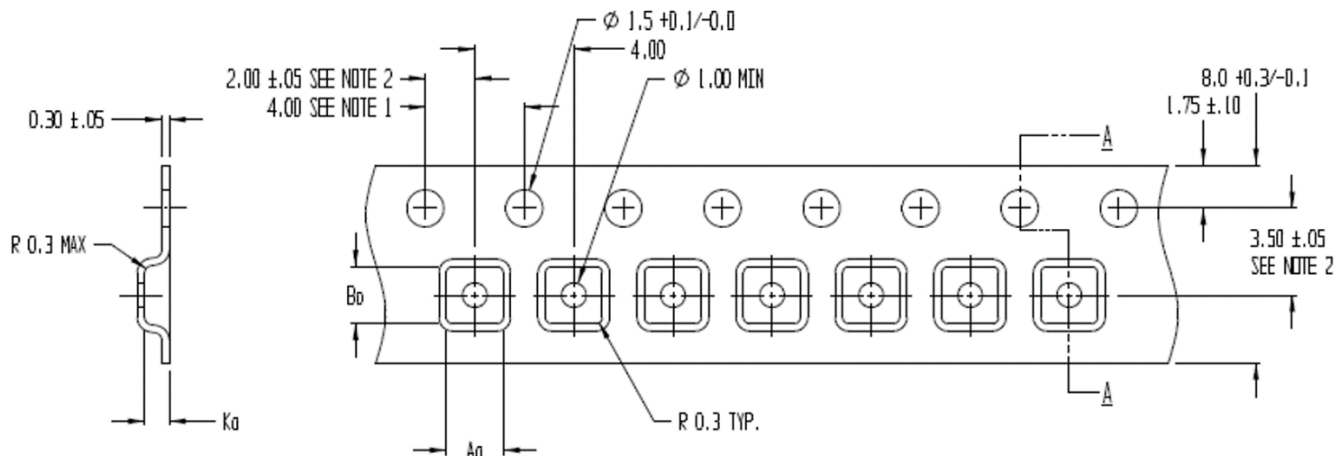
1. All dimensions are in millimeters, Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to SPE-000677
3. Contact plating NiPdAu

Package Marking

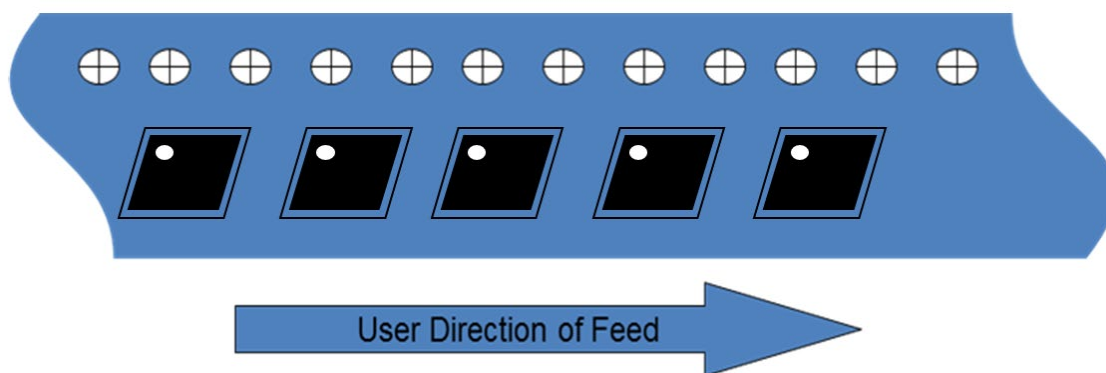


Pin 1 Indicator
Qorvo Logo - Use Q5D
Trace Code to be assigned by SubCon

Tape and Reel Information – Carrier and Cover Tape Dimensions

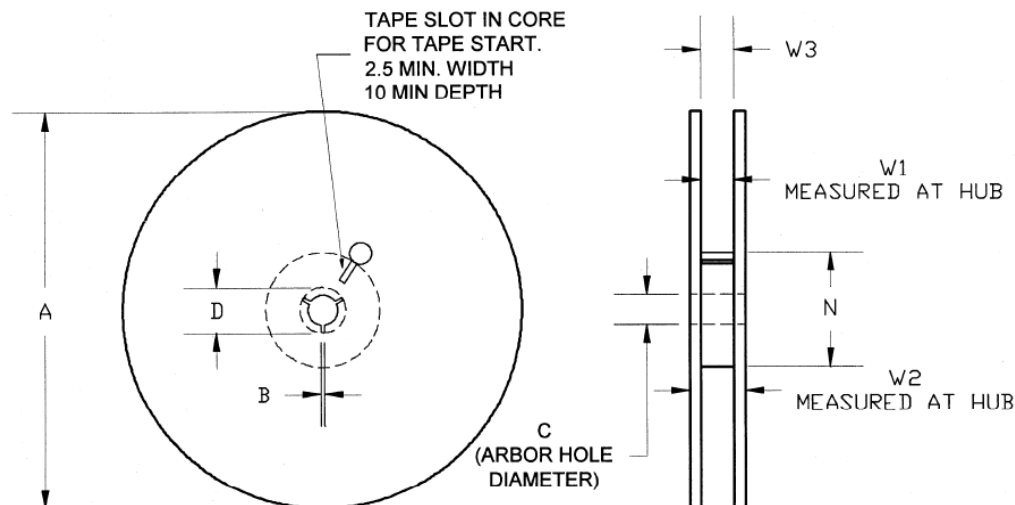


Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.091	2.30
	Width	B0	0.091	2.30
	Depth	K0	0.039	1.00
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.138	3.50
Cover Tape	Width	C	0.213	5.40
Carrier Tape	Width	W	0.315	8.00



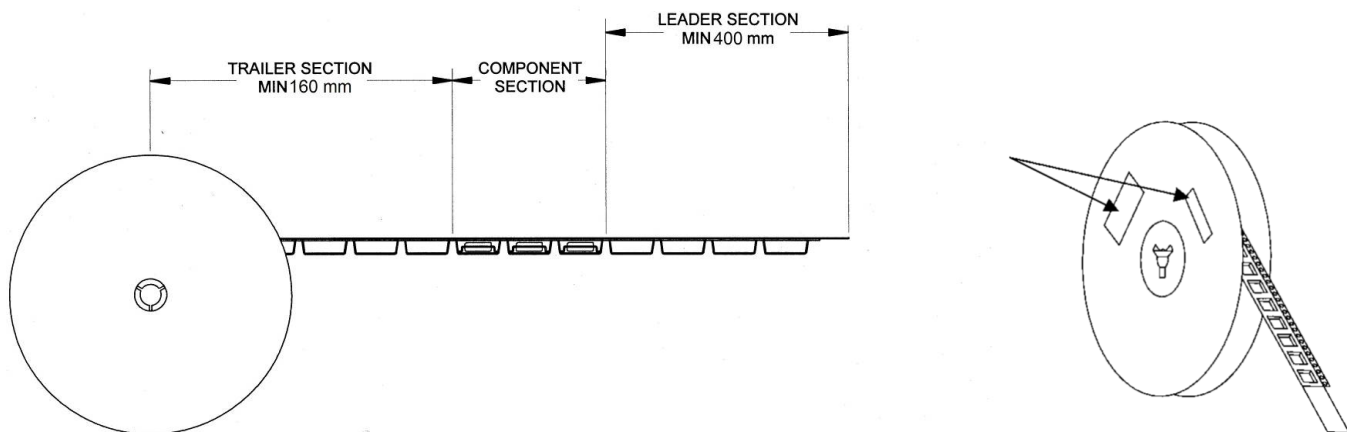
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2500 pieces on a 7" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.559	14.2
	Space Between Flange	W1	0.346	8.8
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B 750V	ESDA / JEDEC JS-001-2017
ESD – Charged Device Model (CDM)	Class C3 1500V	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020E



Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes. Solder profiles available upon request.

Contact plating: NiPdAu (*Thickness: Ni 0.508 ~ 1.524 μm; Pd 0.023 ~ 0.1016 μm; Au 0.00254 ~ 0.01016 μm*)



Detailed Revision History

Revision	Description
5/20/20	Rev A Initial release
11/24/20	Rev B release: updated EVB and BOM
9/9/21	Rev C release from post PT runs setting min/max values; updated ESD/MSL info; added shot with 3 vias under DUT; changed Vcc 3.15V min to 3.3V min, changed thermal resistance to match thermal scans, removed Max Tj; Added SR and SQ orderable callouts; Updated MAX NF to 0.52 dB
10/1/21	Rev D: Added back Max Tj.
3/8/22	Added Note about pin 6 not left floating

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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