

Description

The SX20N65MP is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

General Features

$V_{DS} = 650V$ $I_D = 20A$

$R_{DS(ON)} < 480m\Omega$ @ $V_{GS}=10V$

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)

**Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)**

Symbol	Parameter	Value	Unit
$VDSS$	Drain-Source Voltage ($V_{GS} = 0V$)	650	V
ID	Continuous Drain Current	20	A
IDM	Pulsed Drain Current (note1)	72	A
VGS	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	340	mJ
I_{AR}	Avalanche Current (note1)	18	A
E_{AR}	Repetitive Avalanche Energy note1)	48	mJ
P_D	Power Dissipation ($T_c = 25^\circ C$)	35	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55~+150	$^\circ C$
R_{thJC}	Thermal Resistance, Junction-to-Case	3.55	$^\circ C/W$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ C/W$

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$	650	690	--	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 25^\circ\text{C}$	--	--	1	μA
IGSS	Gate-Source Leakage	$V_{GS} = \pm 30\text{V}$	--	--	± 100	nA
VGS(th)	Gate-Source Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2.0	3.0	4.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	$V_{GS} = 10\text{V}$, $I_D = 9\text{A}$	--	380	480	$\text{m}\Omega$
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$	--	2150	--	pF
C_{oss}	Output Capacitance		--	265	--	
C_{rss}	Reverse Transfer Capacitance		--	6.2	--	
Q_g	Total Gate Charge	VDS=335V, ID=18A, VGS =10V	--	38	--	nC
Q_{gs}	Gate-Source Charge		--	12	--	
Q_{gd}	Gate-Drain Charge		--	13	--	
td(on)	Turn-on Delay Time	VDD=335V, ID=18A, RG = 25 Ω	--	36	--	ns
t_r	Turn-on Rise Time		--	51	--	
td(off)	Turn-off Delay Time		--	80	--	
t_f	Turn-off Fall Time		--	44	--	
I_S	Continuous Body Diode Current	$T_C = 25^\circ\text{C}$	--	--	18	A
ISM	Pulsed Diode Forward Current		--	--	72	
V_{SD}	Body Diode Voltage	$T_J = 25^\circ\text{C}$, $I_{SD} = 18\text{A}$, $V_{GS} = 0\text{V}$	--	--	1.4	V
trr	Reverse Recovery Time	$V_{GS} = 0\text{V}$, $I_S = 18\text{A}$, $dI/dt = 100\text{A}/\mu\text{s}$	--	456	--	ns
Q_{rr}	Reverse Recovery Charge		--	5.9	--	μC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The EAS data shows Max. rating . L=4.1Mh IAS=18A, VDD=50V, RG=25Ω, Starting TJ = 25 °C
- 3、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

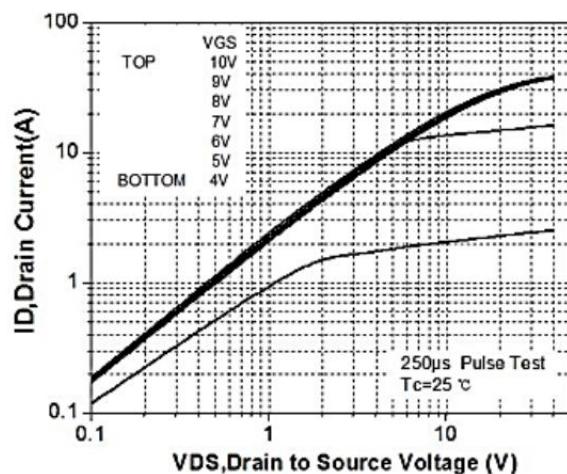


Figure 1. On-Region Characteristics

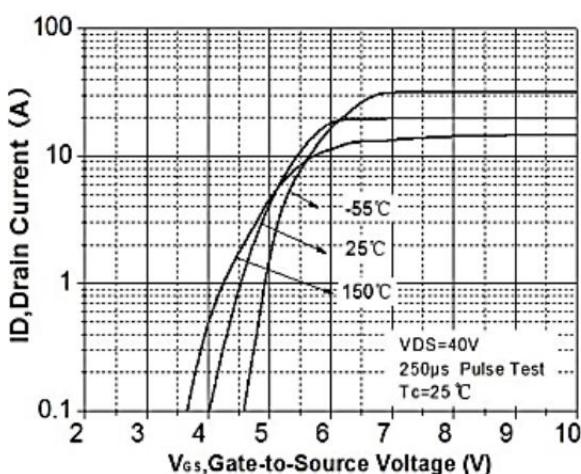


Figure 2. Transfer Characteristics

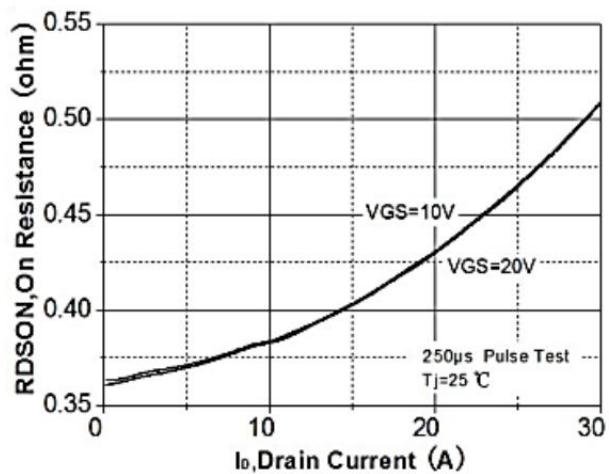


Figure 3. On-Resistance Variation vs
Drain Current and Gate Voltage

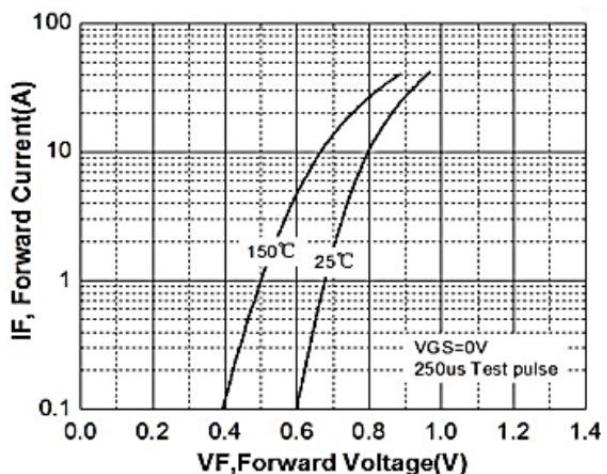


Figure 4. Body Diode Forward Voltage
Variation with Source Current
and Temperature

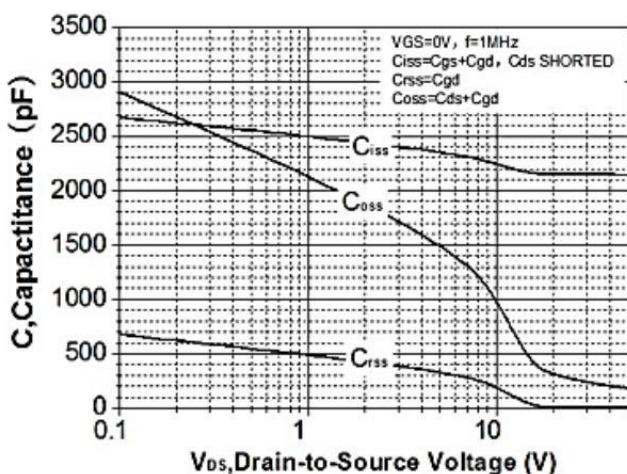


Figure 5. Capacitance Characteristics

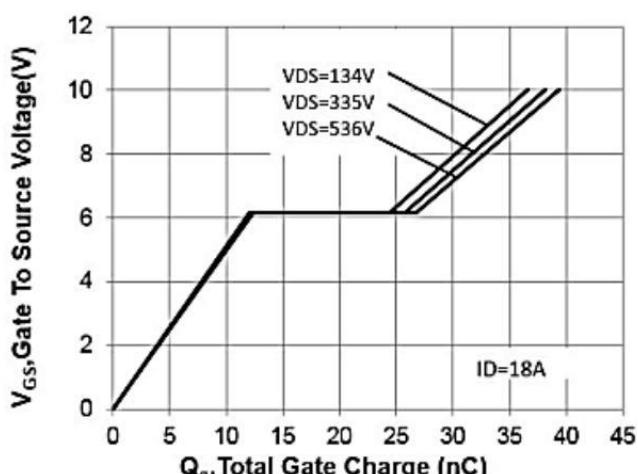
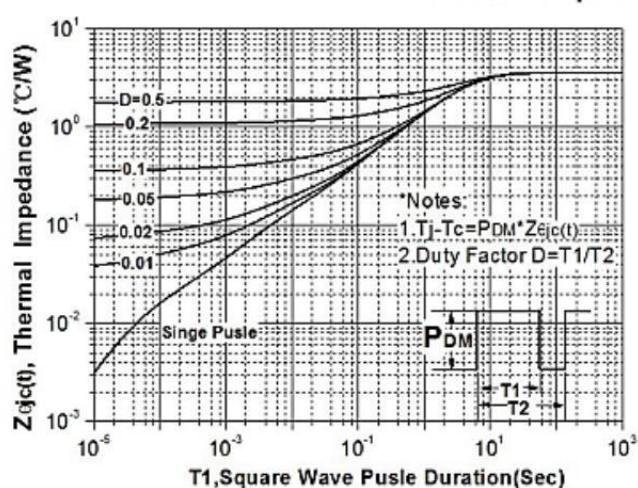
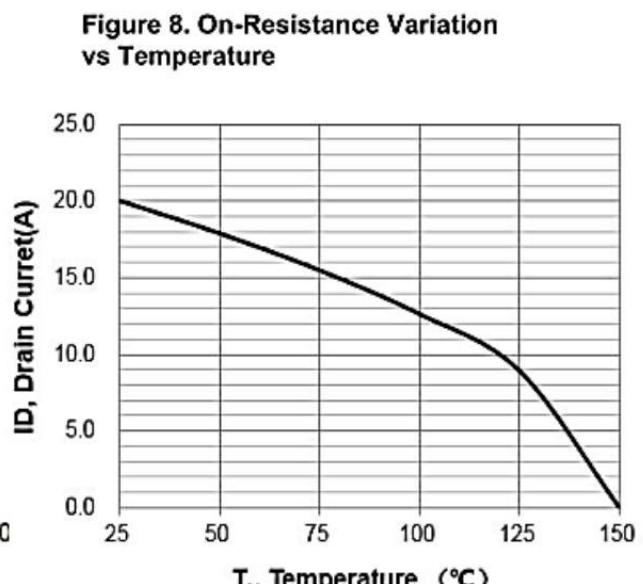
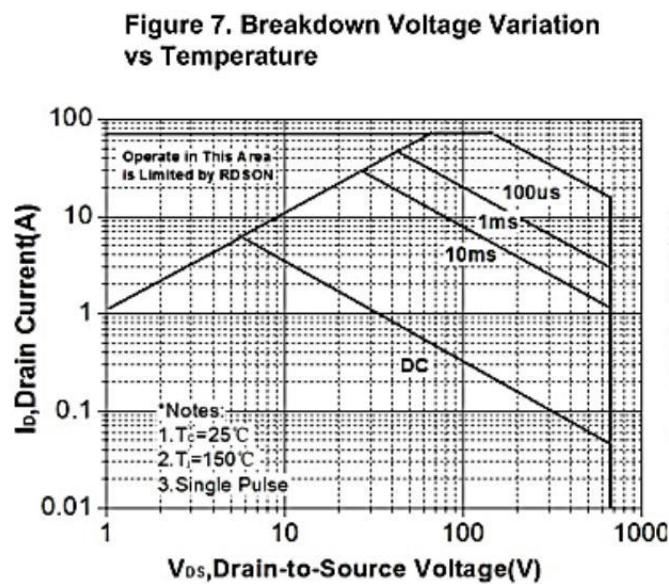
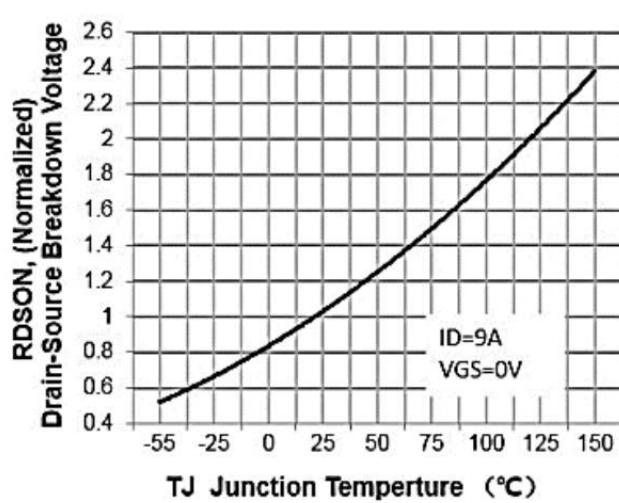
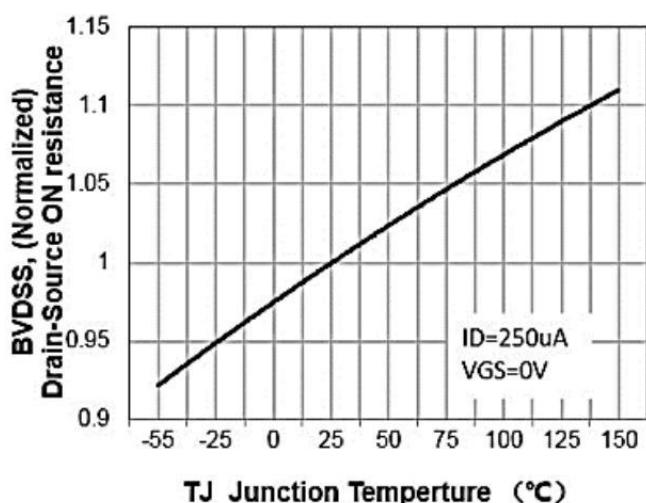
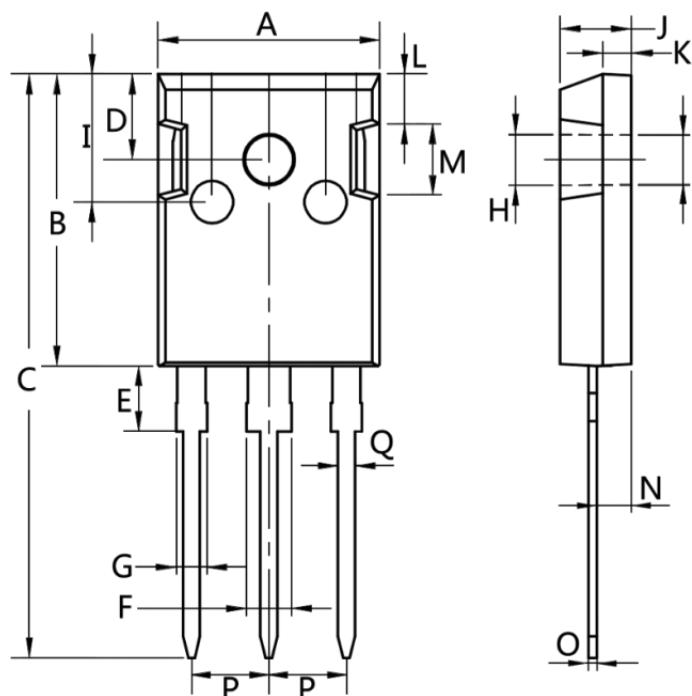


Figure 6. Gate Charge Characteristics

Typical Characteristics



Package Mechanical Data-TO-247-3L

Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	TO-247-3L		360