650V N-Channel Enhancement Mode MOSFET

Description

The SX2N65D is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

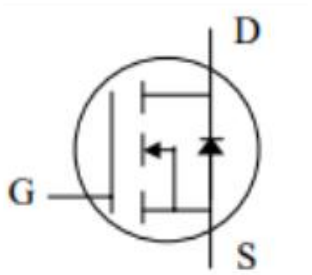
General Features

VDS =650V,ID =2A

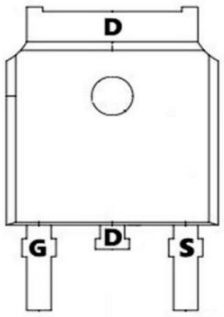
RDS(ON) <4.8Ω@ VGS=10V

Application

Uninterruptible Power Supply(UPS) Power Factor Correction (PFC)



TO-252-3L



Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage (V_{GS} = 0V)	V_{DSS}	650	V
Continuous Drain Current	I_D	2	A
Pulsed Drain Current	I_{DM}	6	A
Gate-Source Voltage	V_{GSS}	±30	V
Single Pulse Avalanche Energy	E_{AS}	57	mJ
Avalanche Current	I_{AR}	2.4	A
Repetitive Avalanche Energy	E_{AR}	6.4	mJ
Power Dissipation (T_C = 25ºC)	P_D	25	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+150	ºC
Thermal Resistance, Junction-to-Case	R_{thJC}	5	ºC/W
Thermal Resistance, Junction-to-Ambient	R_{thJA}	60	

Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	650	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0V, T_J = 25ºC	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±30V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	3.0	--	4.0	V
Drain-Source On-Resistance (Note3)	$R_{DS(on)}$	V_{GS} = 10V, I_D = 1.0A	--	4	4.8	Ω
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	--	310	--	pF
Output Capacitance	C_{oss}		--	39	--	
Reverse Transfer Capacitance	C_{rss}		--	6	--	
Total Gate Charge	Q_g	V_{DD} = 520V, I_D = 2.0A, V_{GS} = 10V	--	8.0	--	nC
Gate-Source Charge	Q_{gs}		--	1.2	--	
Gate-Drain Charge	Q_{gd}		--	5	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 300V, I_D = 2.0A, R_G = 25 Ω	--	7.8	--	ns
Turn-on Rise Time	t_r		--	33	--	
Turn-off Delay Time	$t_{d(off)}$		--	23	--	
Turn-off Fall Time	t_f		--	59	--	
Continuous Body Diode Current	I_S	T_C = 25 ºC	--	--	2	A
Pulsed Diode Forward Current	I_{SM}		--	--	8	
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = 2.0A, V_{GS} = 0V	--	--	1.4	V
Reverse Recovery Time	t_{rr}	V_{GS} = 0V,I_S = 2.0A, di_F/dt =100A /μs	--	80	--	ns
Reverse Recovery Charge	Q_{rr}		--	1.8	--	μC

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS} = 2.4A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25 ºC
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Characteristics

Figure 1. Output Characteristics (T_J = 25ºC)

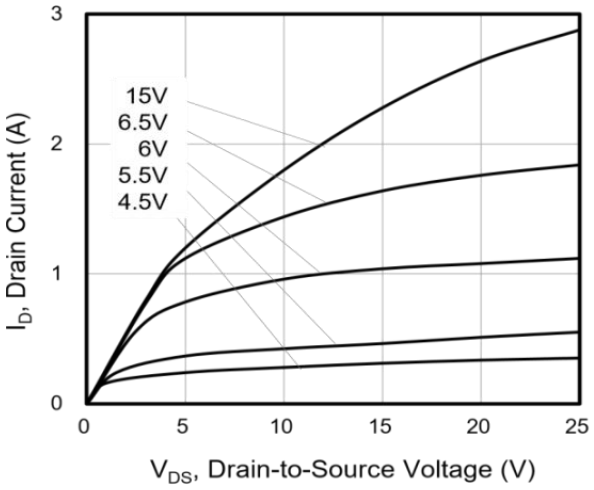


Figure 2. Body Diode Forward Voltage

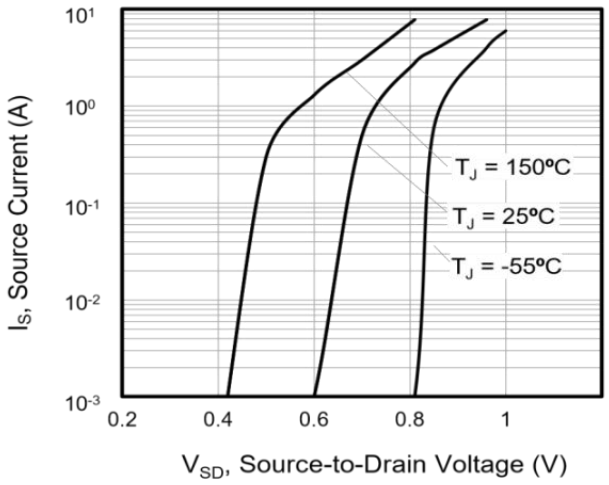


Figure 3. Drain Current vs. Temperature

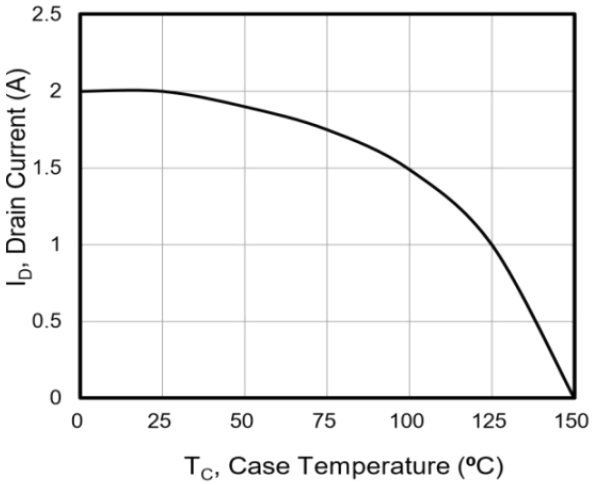


Figure 4. Power Dissipation vs. Temperature TO-251,TO-252

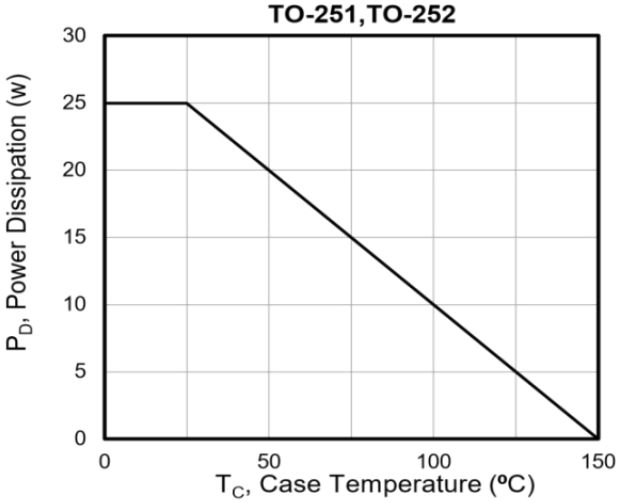


Figure 5. Transfer Characteristics

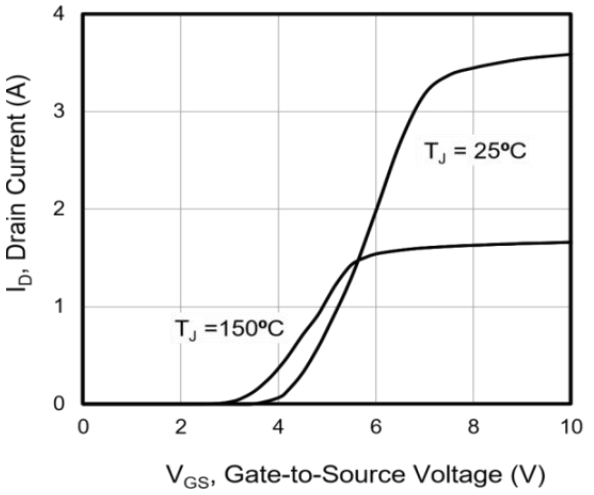
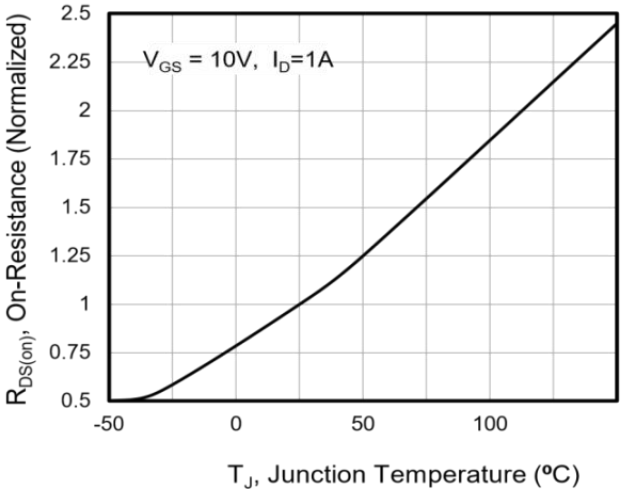


Figure 6. On-Resistance vs. Temperature



Typical Characteristics

Figure 7. Capacitance

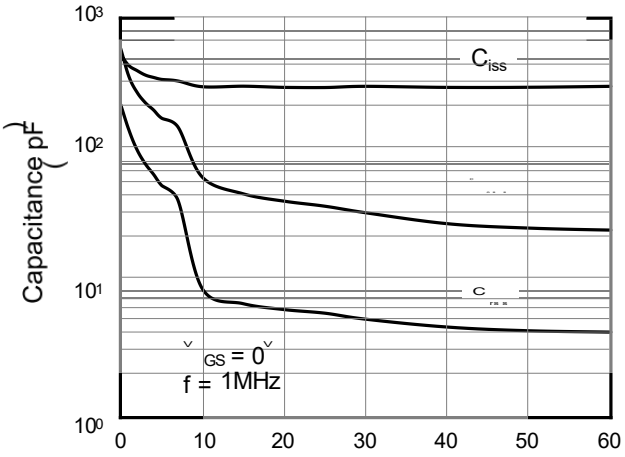


Figure 8. Gate Charge

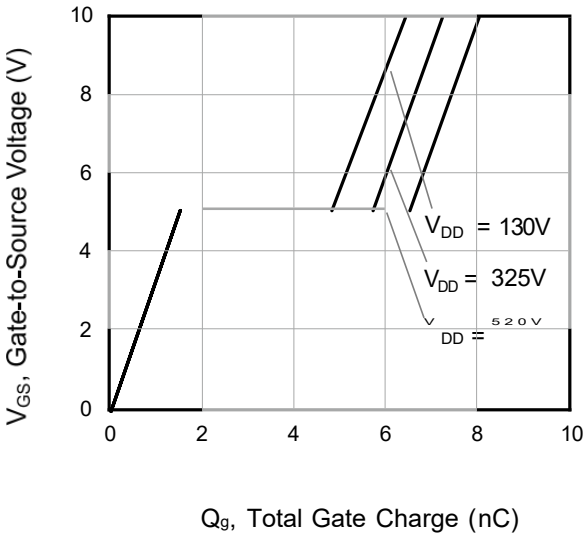
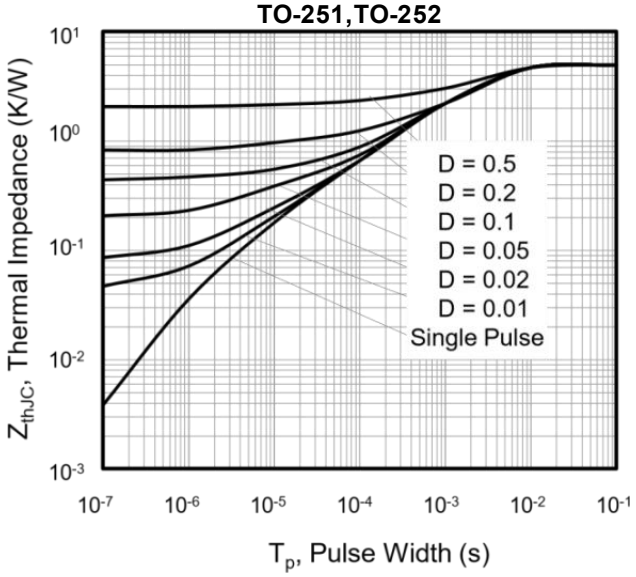


Figure 9. Transient Thermal Impedance TO-251,TO-252



Typical Characteristics

Figure A：Gate Charge Test Circuit and Waveform

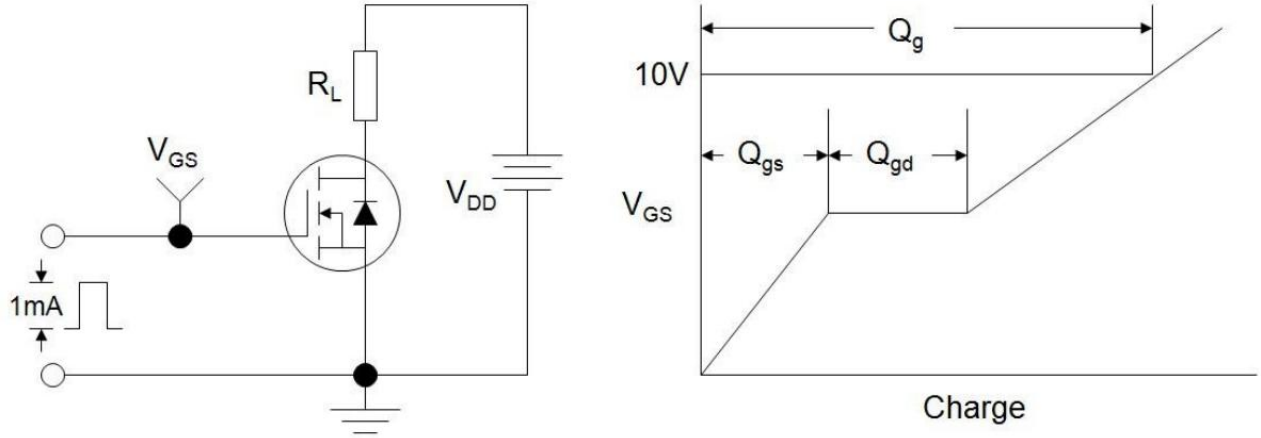


Figure B：Resistive Switching Test Circuit and Waveform

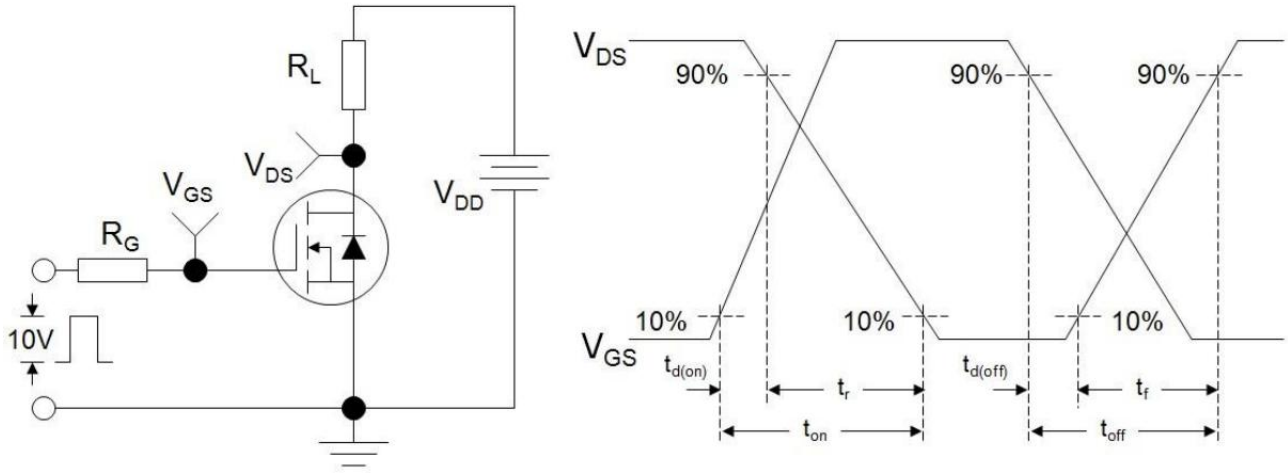
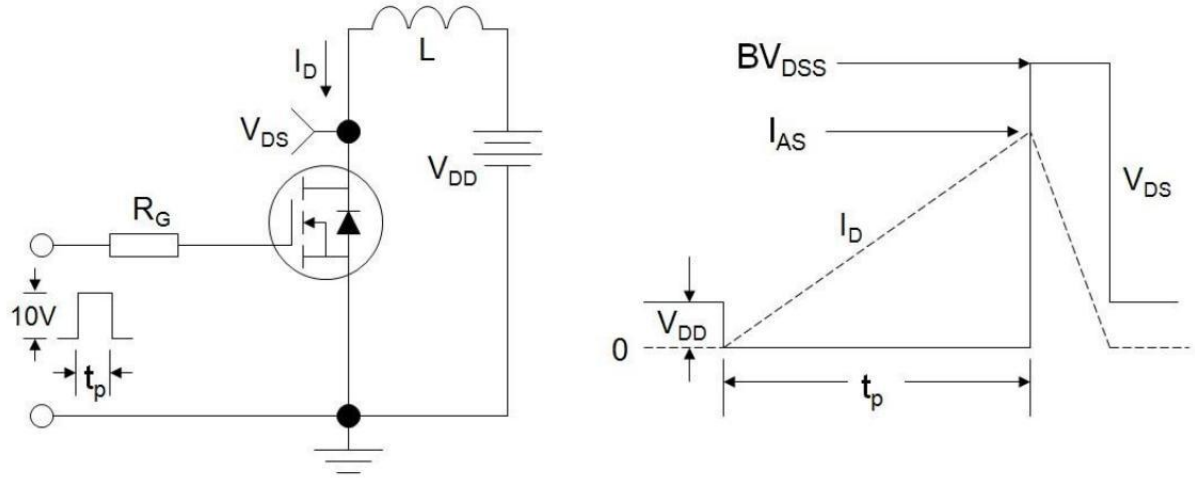
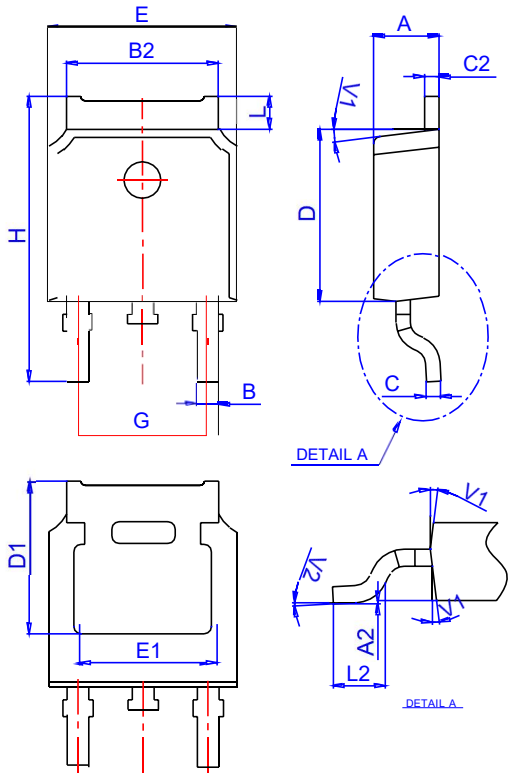


Figure C：Unclamped Inductive Switching Test Circuit and Waveform



Package Mechanical Data: TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	TO-252-3L		2500