

74LVC573A

Octal D-type transparent latch
with 5 V tolerant inputs/outputs; 3-state

Rev. 6 — 26 September 2018

Product data sheet

1. General description

The 74LVC573A consists of eight D-type transparent latches, featuring separate D-type inputs for each latch and 3-state true outputs for bus-oriented applications. A Latch Enable (LE) input and an Output Enable ($\overline{OE}$) input are common to all internal latches.

When LE is HIGH, data at the Dn inputs enters the latches. In this condition, the latches are transparent, that is, a latch output changes each time its corresponding D-input changes. When LE is LOW, the latches store the information that was present at the D-inputs one set-up time preceding the HIGH-to-LOW transition of LE.

When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices as translators in mixed 3.3 V or 5 V applications.

The 74LVC573A is functionally identical to the 74LVC373A, but has a different pin arrangement.

2. Features and benefits

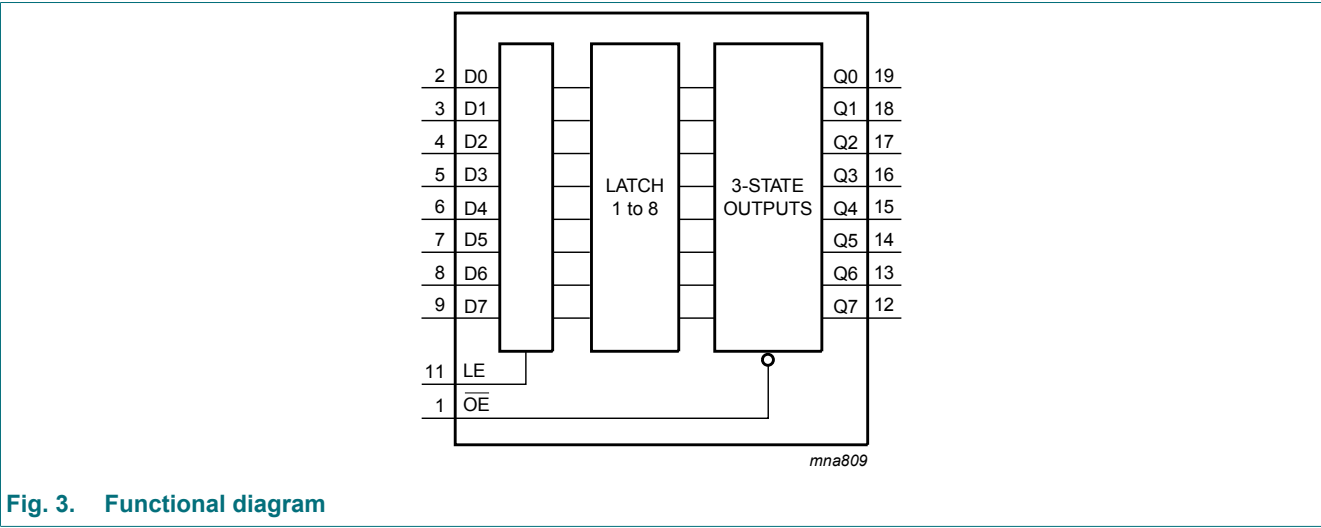
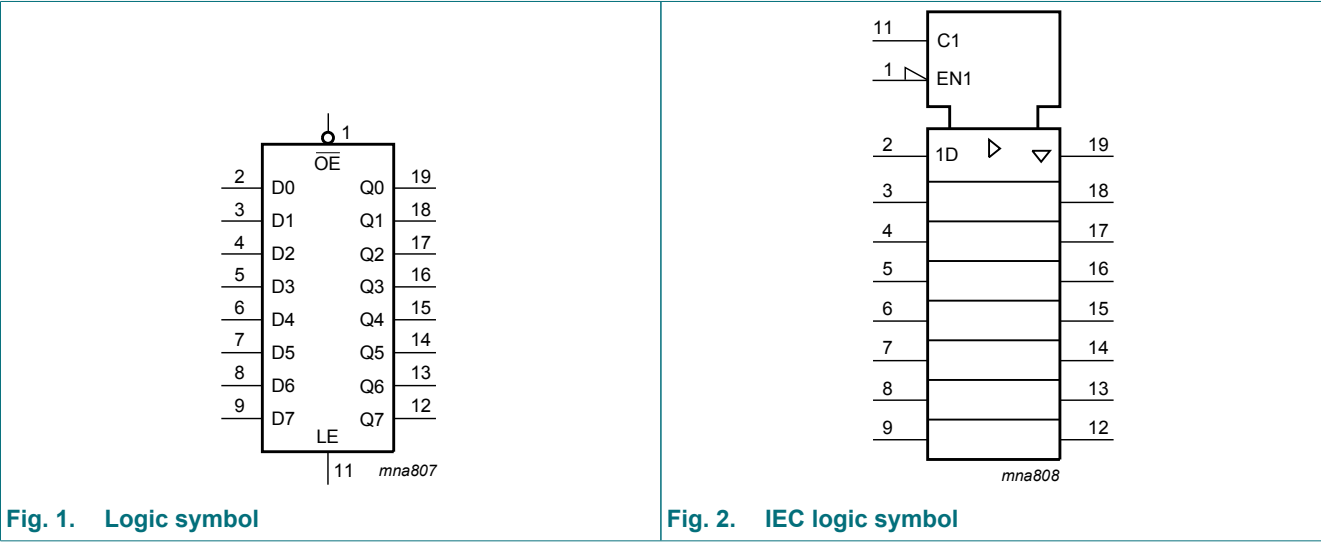
- 5 V tolerant inputs/outputs, for interfacing with 5 V logic
- Supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- High-impedance when $V_{CC} = 0$ V
- Flow-through pinout architecture
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-B exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC573AD	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC573ADB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVC573APW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVC573ABQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram



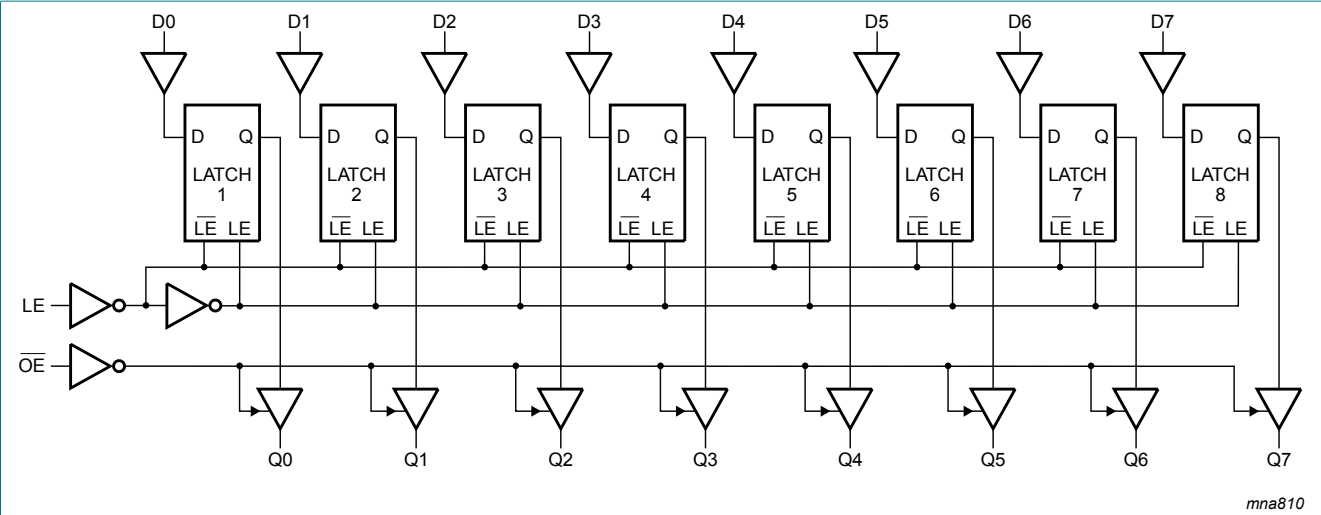
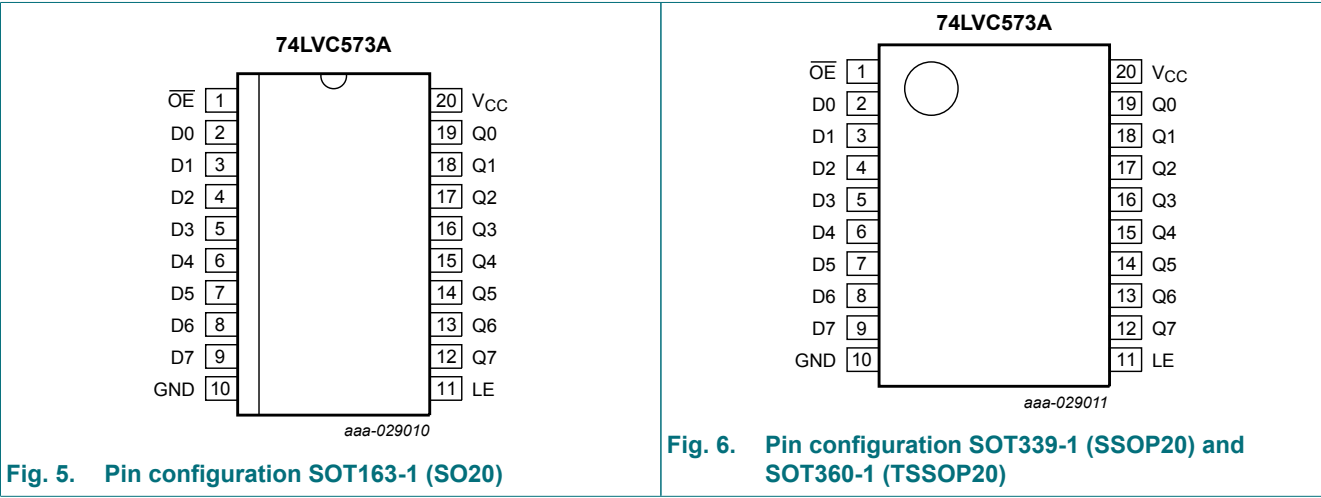


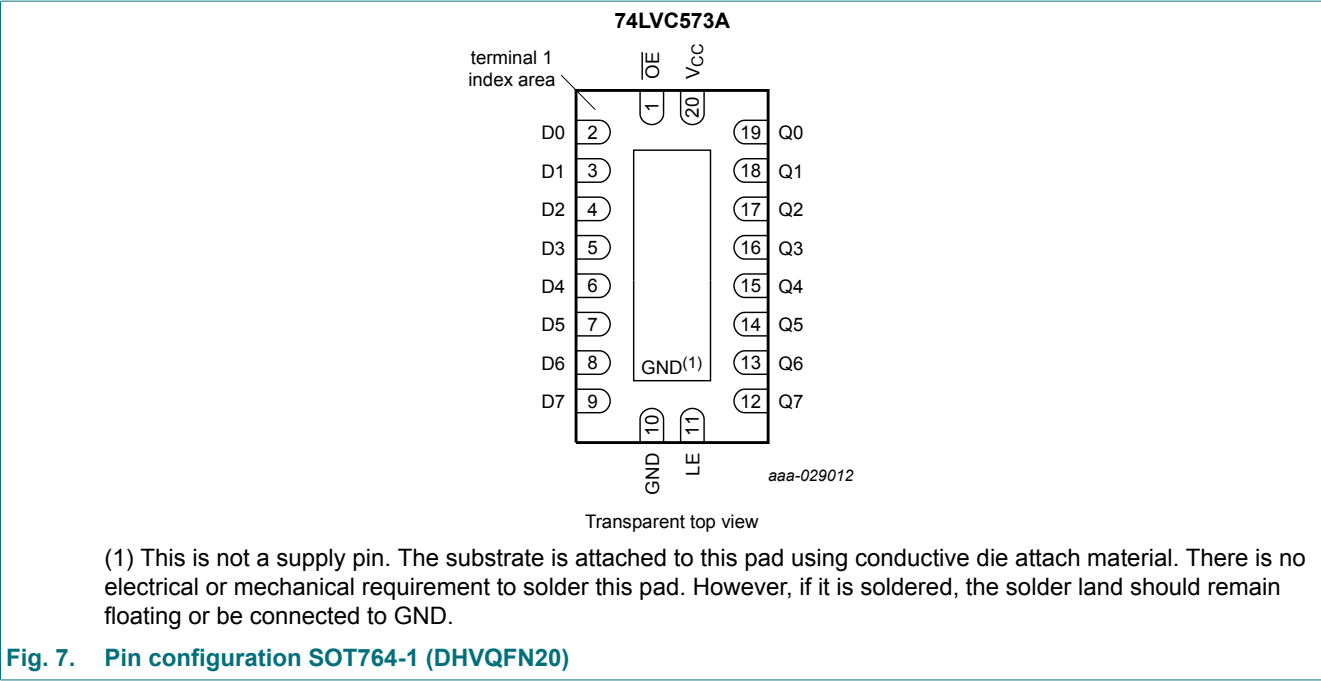
Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	output enable input (active LOW)
LE	11	latch enable input (active HIGH)
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data input
Q0, Q1, Q2,Q3, Q4, Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	data output
GND	10	ground (0 V)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Functional table

H = HIGH voltage level ; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high-impedance OFF-state

Operating modes	Input			Internal latch	Output
	$\overline{OE}$	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$	-50	-	mA
V_I	input voltage	[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
V_O	output voltage	[2]	-0.5	$V_{CC} + 0.5$	V
I_O	output current	$V_O = 0\text{ V to }V_{CC}$	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$ [3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO20 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.

For SSOP20 and TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

For DHVQFN20 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH- or LOW-state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 µA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND	-	0.1	±5	-	±20	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	0.1	±10	-	±20	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Fig. 12](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	Dn to Qn; see Fig. 8 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	16.0	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.1	7.8	16.3	2.1	18.8	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	4.1	8.0	1.5	9.2	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	4.1	7.2	1.5	9.0	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	3.4	6.2	1.5	8.0	ns
		LE to Qn; see Fig. 9 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	16.0	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.0	7.7	16.0	2.0	18.4	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	4.1	7.8	1.5	9.1	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	3.7	7.5	1.5	9.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	3.4	6.5	1.5	8.5	ns
t_{en}	enable time	OE to Qn; see Fig. 10 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	18.0	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.7	7.5	17.5	1.7	20.2	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	4.2	9.2	1.5	10.6	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	4.2	8.5	1.5	11.0	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	3.4	7.5	1.5	9.5	ns
t_{dis}	disable time	OE to Qn; see Fig. 10 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	8.0	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	3.3	10.1	1.0	11.6	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.3	1.8	5.7	0.3	6.6	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	3.0	6.5	1.5	8.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	2.5	6.0	1.5	7.5	ns
t_W	pulse width	LE HIGH; see Fig. 9						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	5.0	-	-	5.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	4.0	-	-	4.0	-	ns
		$V_{CC} = 2.7 \text{ V}$	3.2	-	-	3.2	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.2	1.6	-	3.2	-	ns
t_{su}	set-up time	Dn to LE; see Fig. 11						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	4.0	-	-	4.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.5	-	-	2.5	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.7	-	-	1.7	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.7	-	-	1.7	-	ns
t_h	hold time	Dn to LE; see Fig. 11						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	3.0	-	-	3.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.9	-	-	1.9	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	-	-	1.5	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.4	-	-	1.4	-	ns

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$t_{sk(0)}$	output skew time	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per latch; $V_I = \text{GND to } V_{CC}$ [4]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	7.1	-	-	-	pF
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	10.3	-	-	-	pF
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	13.2	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and $V_{CC} = 1.2\text{ V}, 1.8\text{ V}, 2.5\text{ V}, 2.7\text{ V}$ and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

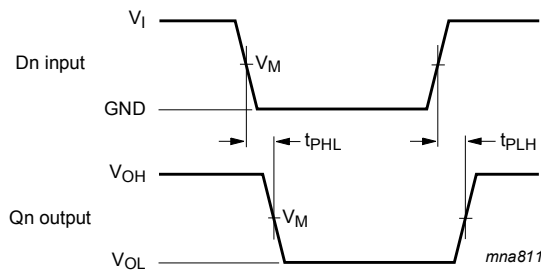
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

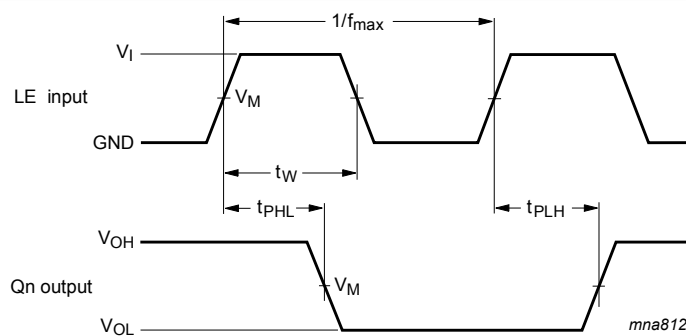
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Input (Dn) to output (Qn) propagation delays



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 9. Latch Enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

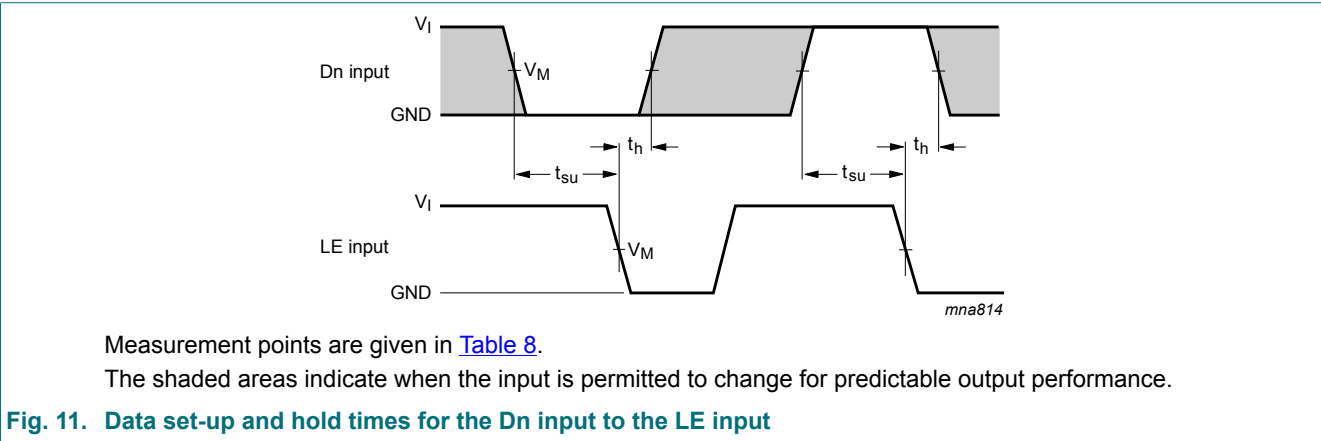
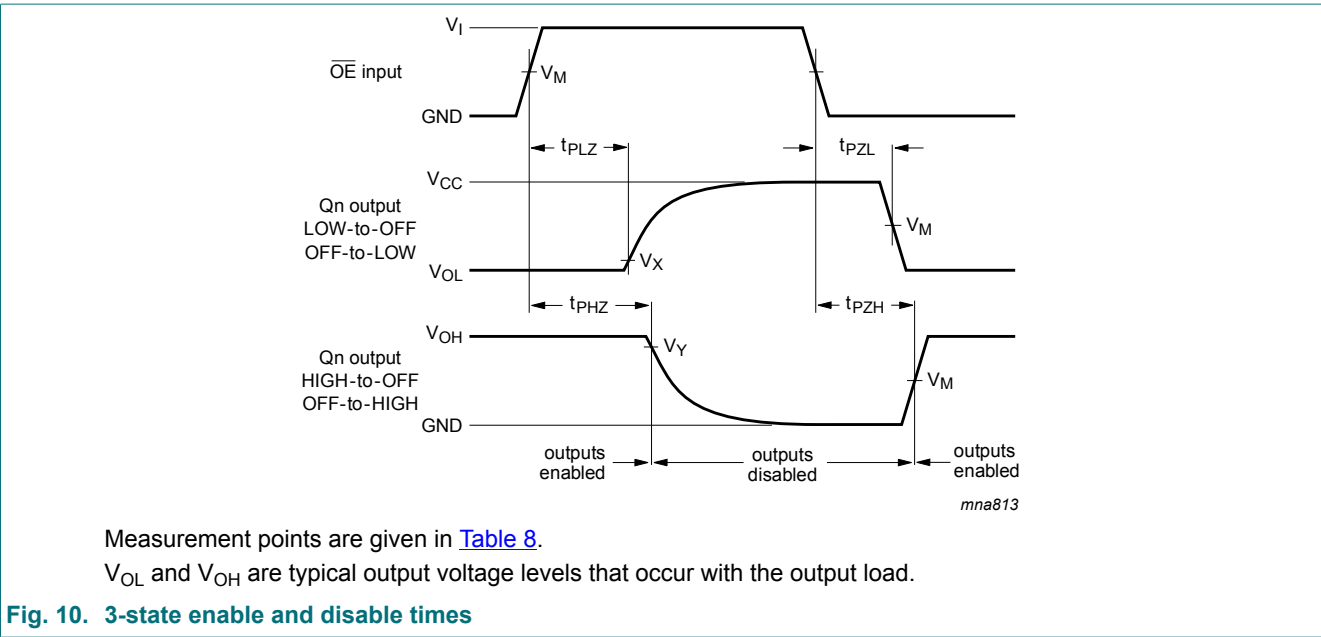


Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

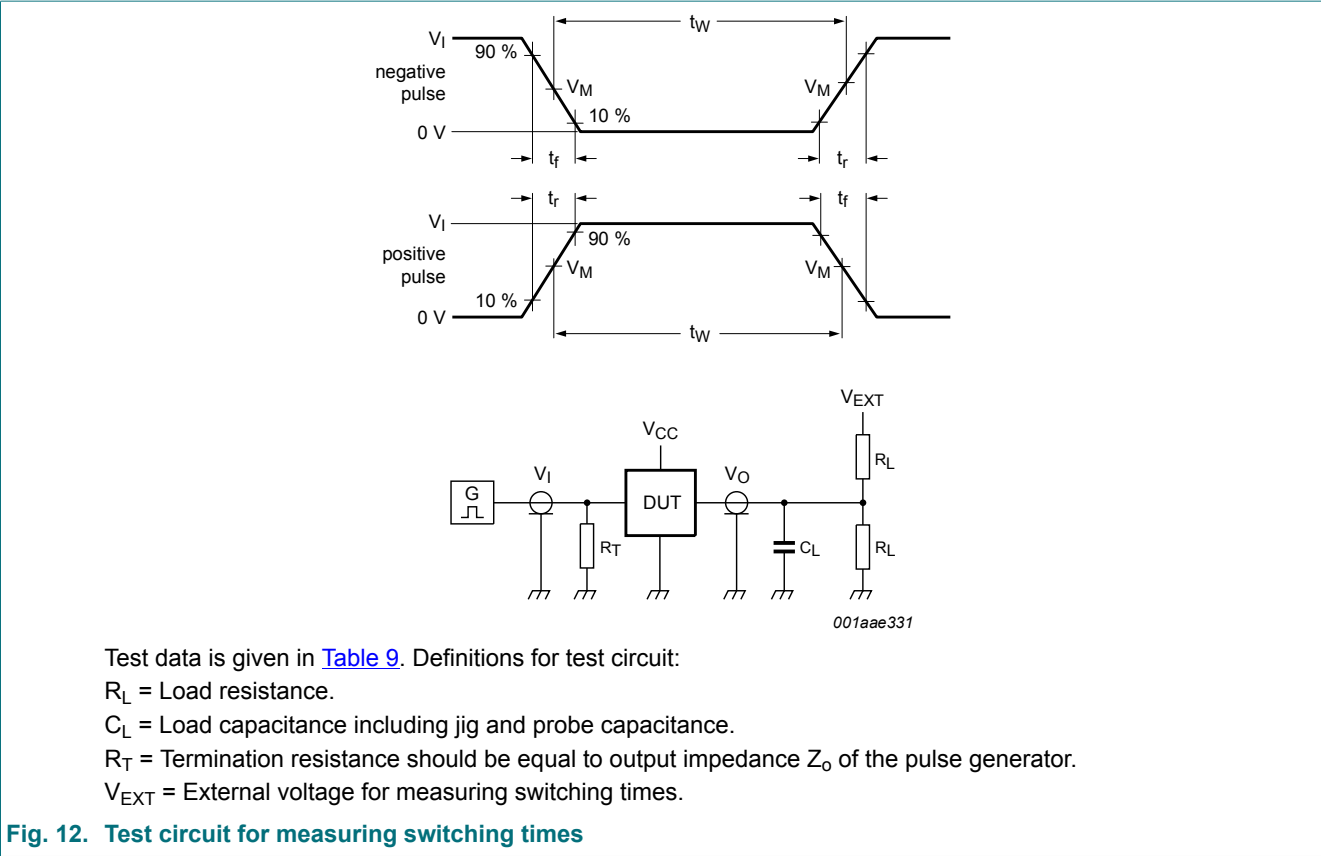


Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

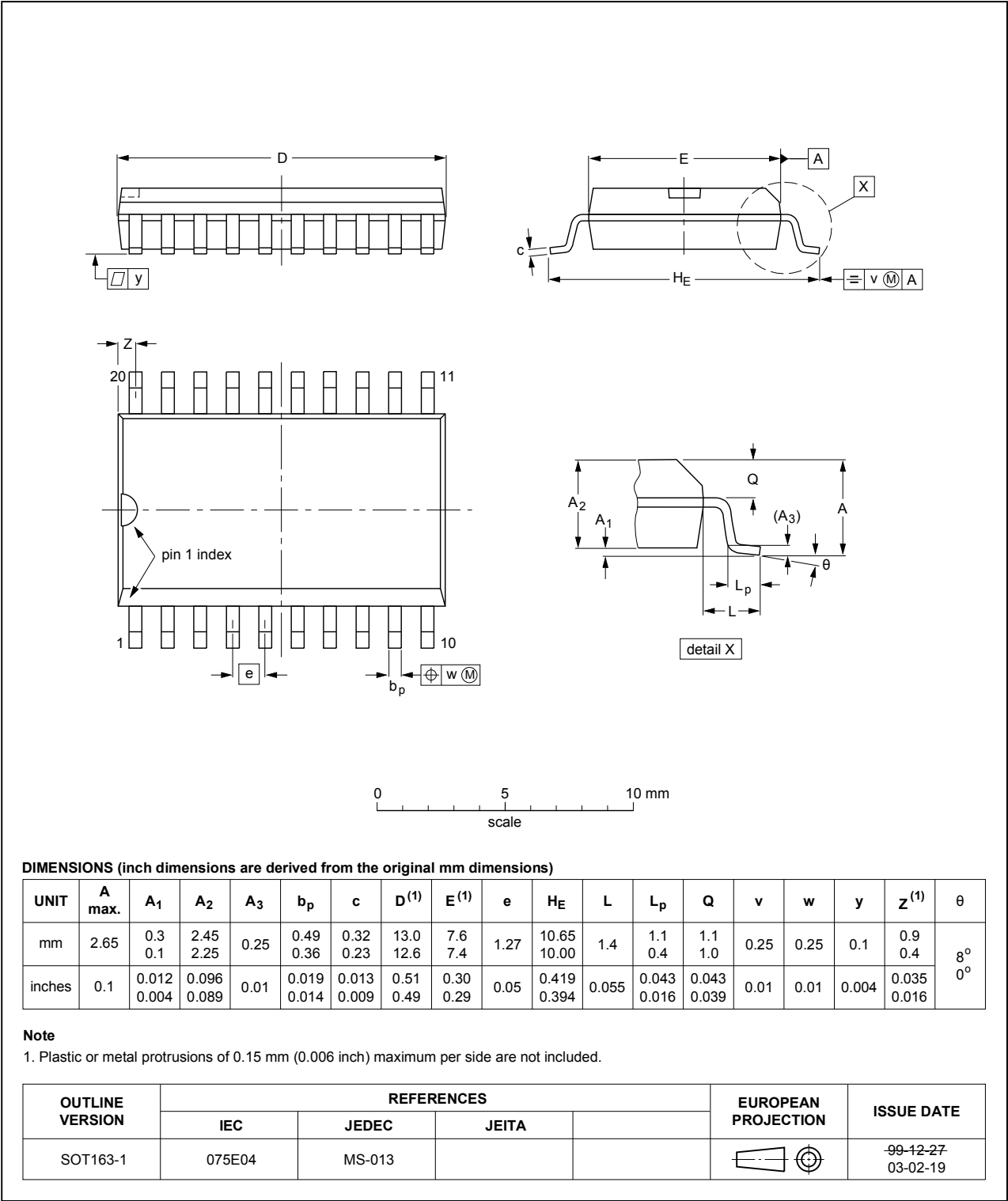


Fig. 13. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

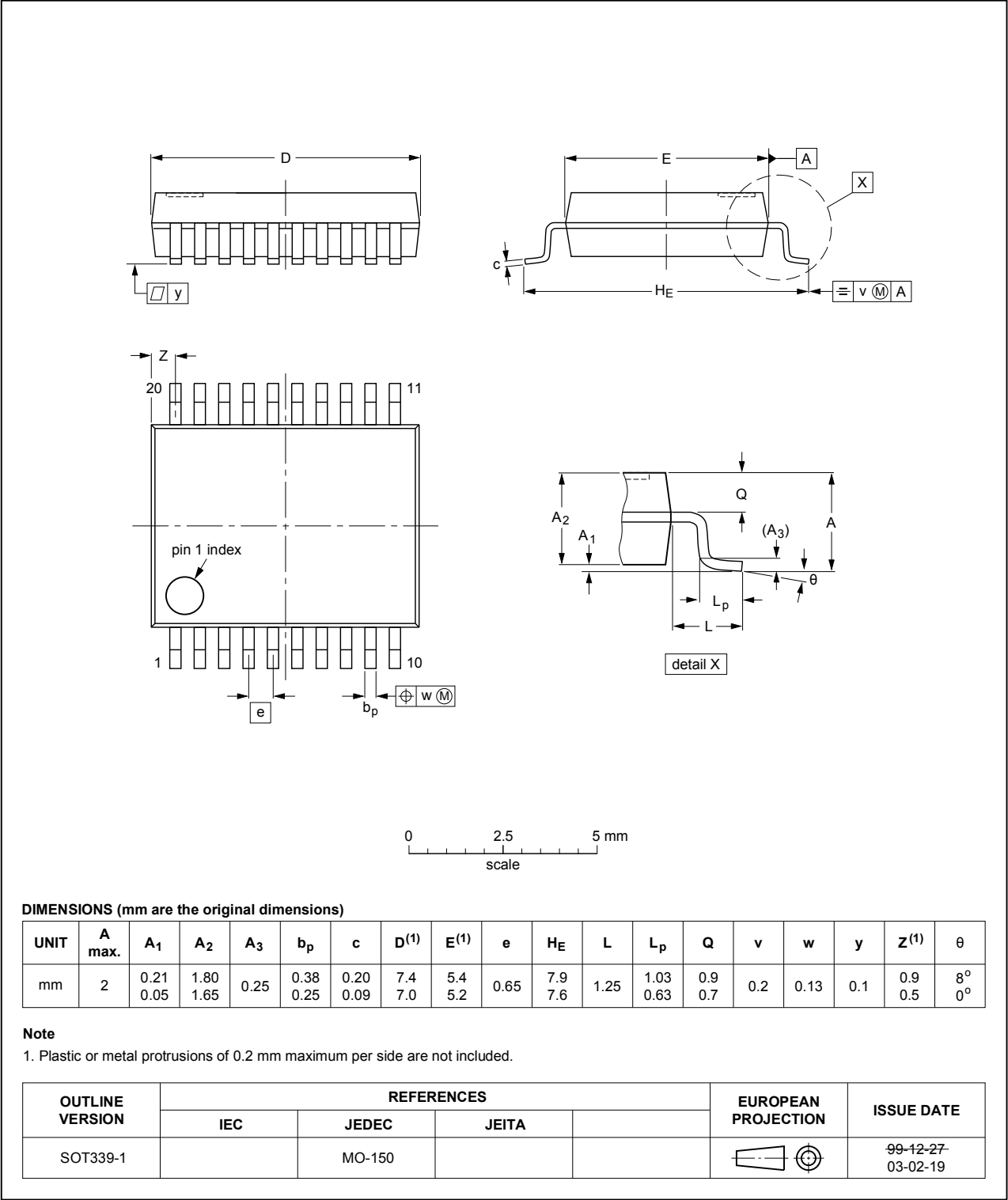


Fig. 14. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

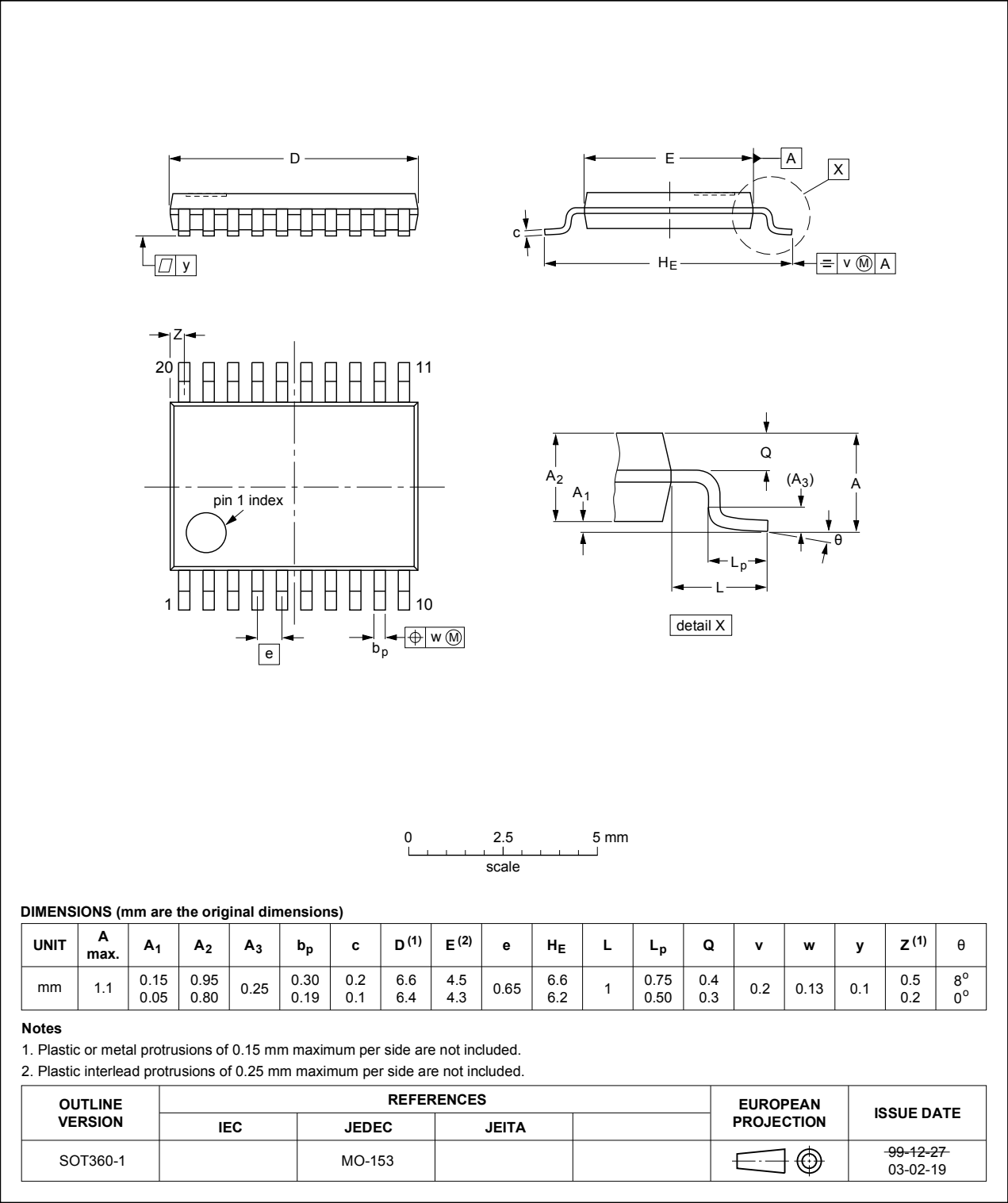


Fig. 15. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

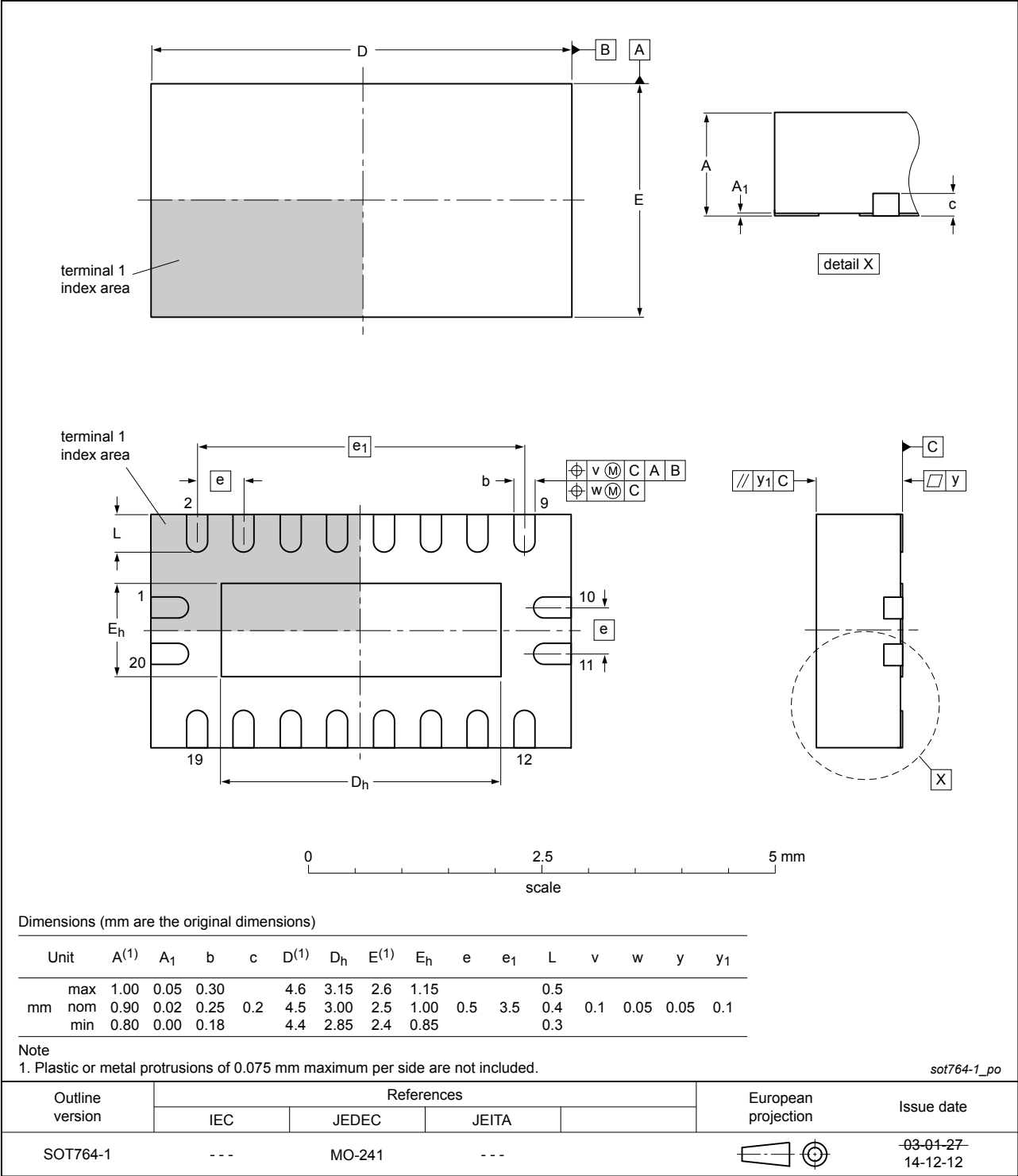


Fig. 16. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC573A v.6	20180926	Product data sheet	-	74LVC573A v.5
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type number 74LVC573ABX (SOT1045-2) removed. - Package outline drawing SOT764-1 updated			
74LVC573A v.5	20130219	Product data sheet	-	74LVC573A v.4
Modifications:	74LVC573ABX added.			
74LVC573A v.4	20121129	Product data sheet	-	74LVC573A v.3
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Table 4, Table 5, Table 6, Table 7, Table 8 and Table 9: values added for lower voltage ranges.			
74LVC573A v.3	20031003	Product specification	-	74LVC573A v.2
74LVC573A v.2	20030526	Product specification	-	74LVC573A v.1
74LVC573A v.1	19980729	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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