MP28167-B

2.8V to 22V V_{IN}, 3A I_{OUT}, Four-Switch, High-Frequency, Integrated Buck-Boost Converter with PG Indication

DESCRIPTION

The MP28167-B is a synchronous, four-switch, integrated buck-boost converter regulates the output voltage (V_{OUT}) across a wide 2.8V to 22V input voltage (V_{IN}) range with high efficiency. Integrated V_{OUT} scaling and the adjustable output current limit (I_{OUT_LIMIT}) meet USB power delivery (PD) requirements.

The MP28167-B uses constant-on-time (COT) control in buck mode and constant-off-time control in boost mode to provide fast load transient response and smooth buck-boost mode transient. The MP28167-B provides automatic pulse-frequency modulation (PFM)/pulse-width modulation (PWM) mode and forced PWM modes. It also provides a configurable output constant current (CC) limit, which supports flexible design for different applications.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), configurable soft start (SS), and thermal shutdown.

The MP28167-B is available in a QFN-16 (3mmx3mm) package.

FEATURES

- Configurable V_{OUT} via the FB Pin
- Wide 2.8V to 22V Operating V_{IN} Range
- 0.08V to 1.637V Reference Voltage (V_{REF}) Range with 0.8mV Resolution via the I^2C (1) (Default 0.54V V_{REF})
- 3A Output Current (I_{OUT}) and 4A Input Current (I_{IN})
- Four Low On Resistance ($R_{DS(ON)}$) Internal Buck Power MOSFETs
- Adjustable, Accurate CC I_{OUT_LIMIT} with Internal Sensing MOSFET via the I^2C
- 500kHz, 750kHz, 1MHz, or 1.25MHz Selectable Switching Frequency (f_{SW}) (Default 1.25MHz f_{SW})
- Output OVP with Hiccup Mode
- Output Short-Circuit Protection (SCP) with Hiccup Mode
- Over-Temperature Warning and Shutdown
- Power Good (PG) Indication
- One-Time Programmable (OTP) Non-Volatile Memory (NVM)
- I^2C-Configurable Line Drop Compensation, PFM/PWM Mode, SS, OCP, and OVP
- Configurable Enable (EN) Shutdown Discharge
- Available in a QFN-16 (3mmx3mm) Package

MPL Optimized Performance with MPS Inductor MPL-AL6050 Series

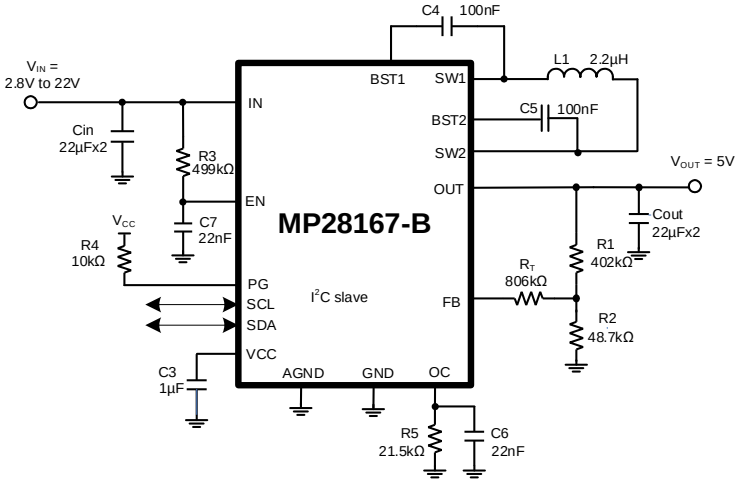
APPLICATIONS

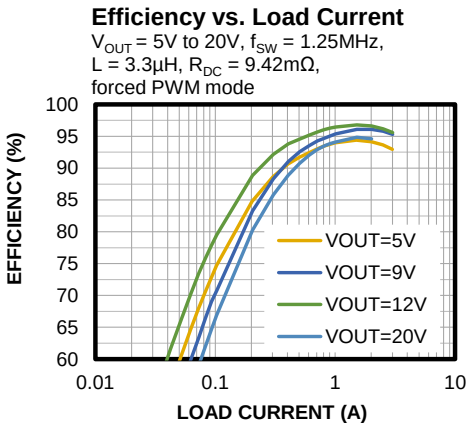
- USB Power Delivery (PD) Sourcing Ports
- Wireless Charging Transmitter
- Buck-Boost Bus Supplies

Note:

1) For applications where V_{OUT} is below 3V, f_{SW} decreases.

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP28167GQ-B	QFN-16 (3mmx3mm)	*See below*	1
EVKT-MP28167-B	Evaluation kit		

* For Tape & Reel, add suffix -Z (e.g. MP28167GQ-B-Z).

TOP MARKING

CAXY
LLLL

CAX: Product code of MP28167GQ-B
Y: Year code
LLLL: Lot number

EVALUATION KIT EVKT-MP28167-B

EVKT-MP28167-B kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVL28167-B-Q-00A	MP28167-B evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I^2C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

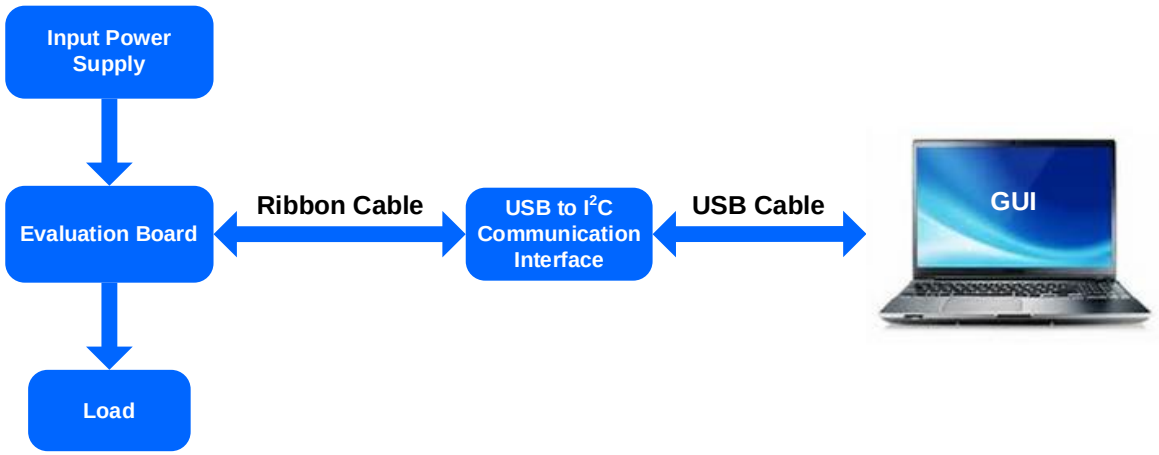
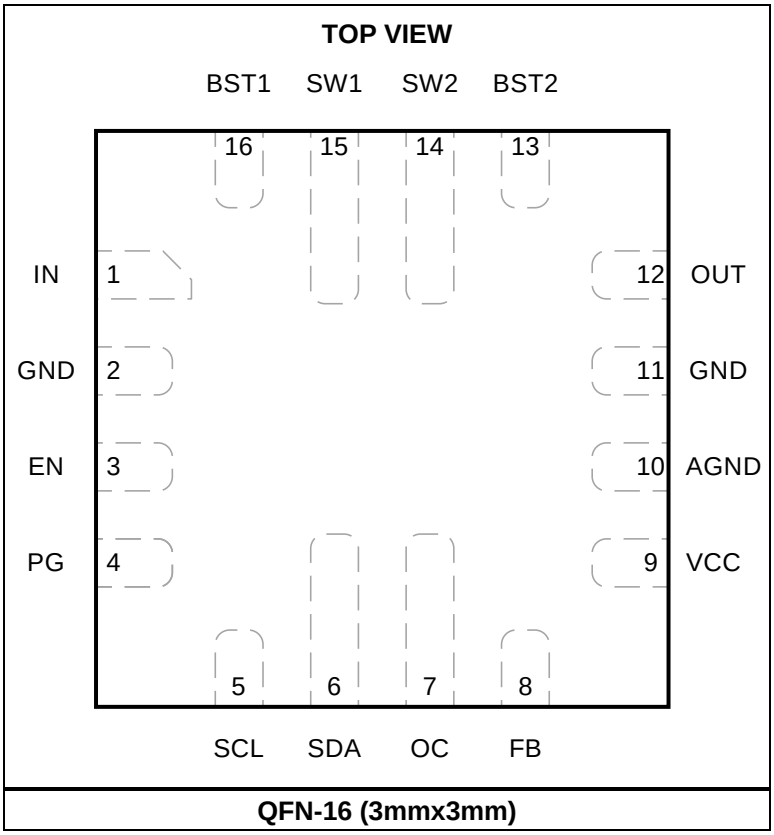


Figure 1: EVKT-MP28167-B Evaluation Kit

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	IN	**Input voltage.** The IN pin is the drain of the internal power device, and provides power to the entire chip. The MP28167-B operates from a 2.8V to 22V input voltage (V_{IN}). A capacitor (C_{IN}) is required to prevent large voltage spikes from appearing at the input. Place C_{IN} as close to the IC as possible.
2, 11	GND	**Power ground.** GND is the reference ground of the regulated output voltage (V_{OUT}). GND requires extra consideration during PCB layout. Connect GND with copper traces and vias.
3	EN	**On/off control for entire chip.** Pull EN high to turn the device on; pull EN low or float EN to turn it off. EN has an internal, 2MΩ pull-down resistor connected to ground.
4	PG	**Power good output.** The PG pin indicates the V_{OUT} status.
5	SCL	**I^2C interface clock pin.** The SCL pin can support an I^2C clock up to 3.4MHz. If not used, SCL should be pulled up to VCC.
6	SDA	**Data pin of the I^2C interface.** If not used, SDA should be pulled up to VCC.
7	OC	**Output constant current (CC) limit setting.**
8	FB	**Feedback.** The FB pin sets V_{OUT} when connected to the tap of an external resistor divider that is connected between the output and GND.
9	VCC	**Internal 3.65V LDO regulator output.** Decouple VCC using a 1µF capacitor.
10	AGND	**Analog ground.** Connect AGND to GND using a single point.
12	OUT	**Output power pin.** Place the output capacitor (C_{OUT}) close to the OUT and GND pins.
13	BST2	**Bootstrap.** Connect a 0.1µF capacitor between the SW2 and BST2 pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
14	SW2	**Second half-bridge switching node.** Connect one end of the inductor to SW2 for the current to run through the bridge.
15	SW1	**First half-bridge switching node.** Connect one end of the inductor to SW1 for the current to run through the bridge.
16	BST1	**Bootstrap.** Connect a 0.1µF capacitor between the SW1 and BST1 pins to form a floating supply across the HS-FET driver.

ABSOLUTE MAXIMUM RATINGS (2)

Input voltage (V_{IN}) 26V
V_{OUT} 24V
V_{SWx} (DC) .....-0.3V to +24.3V
V_{SWx} (10ns) .....-7V to +26V
V_{BSTx} ..... V_{SWx} + 4V
V_{EN} .....-0.3V to +26V
V_{PG} .....-0.3V to +5.5V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (3) (6) 4.8W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings (4)

Human body model (HBM) (all pins)..... ±2kV
Charged device model (CDM) (all pins).....±2kV

Recommended Operating Conditions (5)

Operating input voltage (V_{IN}) range……
……2.8V to 22V
Output voltage (V_{OUT}) range.....1V to 20.47V
Output current (I_{OUT}).....
…3A continuous current or 4A input current (I_{IN})
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-16 (3mmx3mm)		
EVL28167-B-Q-00A (6)	26	3 °C/W
JESD51-7 (7)	50	12 °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Human body model (HBM) is per JEDEC specification JESD22-A114. Charged device model (CDM) is per JEDEC specification JESD22-C101. JEDEC document JEP155 states that a 500V HBM allows for safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that a 250V CDM allows for safe manufacturing with a standard ESD control process.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on the EVL28167-B-Q-00A, 4-layer PCB, 64mmx64mm.
7) Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 specifications and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (8), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{IN}	V_{EN} = 0V		2	5	μA
Quiescent supply current	I_Q	Not switching, I^2C sets pulse-frequency modulation (PFM) mode		1		mA
Enable (EN) rising threshold	V_{EN_RISING}		1.0	1.1	1.2	V
EN hysteresis	V_{EN_HYS}			110		mV
EN to ground resistance	R_{EN}	V_{EN} = 2V		2		MΩ
EN on to V_{OUT} > 90% delay	t_{DELAY}	See Figure 10 on page 19		2.3		ms
VCC regulator voltage	V_{CC}		3.3	3.65	4	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 10mA		1		%
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		2.5	2.65	2.8	V
V_{IN} UVLO hysteresis	V_{UVLO_HYS}			160		mV
Power Converter						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	Switch A (SWA) and switch D (SWD)		25	40	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	Switch B (SWB) and switch C (SWC)		21	35	mΩ
Feedback (FB) voltage	V_{FB}	T_J = 25°C	-1%	540	+1%	mV
		T_J = -40°C to +125°C	-1.5%	540	+1.5%	mV
FB current	I_{FB}	V_{FB} = 1.05V		10		nA
Output discharge resistance	R_{DIS}			60	100	Ω
Switch leakage current	I_{SW_LKG}	V_{EN} = 0V, V_{SWx} = 22V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SWx} = 22V, T_J = -40°C to +125°C			5	μA
Switching frequency	f_{SW}	Default f_{SW}, T_J = 25°C	-25%	1.25	+25%	MHz
Minimum on time (9)	t_{ON_MIN1}	Switch A, switch B, switch C, and switch D		160		ns
Maximum duty cycle	D_{MAX}	Buck mode, FREQ = 00 (500kHz)		85		%
Minimum duty cycle (9)	D_{MIN}	Boost mode, FREQ = 00 (500kHz)		15		%
Soft-start time	t_{SS}	Can be changed via the I^2C, V_{REF} = 0V to 1V, default t_{SS}		2.2		ms
Protection						
Output over-voltage protection (OVP) rising threshold	V_{OVP_RISING}		150	160	170	% of V_{REF}
Output OVP falling threshold	$V_{OVP\_FALLING}$		130	140	150	% of V_{REF}
LS-FET B valley current limit	I_{LIMIT2}	SWB	6	8	10	A
LS-FET C peak current limit	I_{LIMIT3}	SWC		10		A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C [8], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output average current [9]	I_{OUT_LIM1}	V_{OUT} = 5V, across 0°C to 125°C temperature range	0.85	1	1.15	A
	I_{OUT_LIM2}	V_{OUT} = 5V, across 0°C to 125°C temperature range	-5%	3.5	+5%	A
Output under-voltage protection (UVP) threshold	V_{UVP}	20µs deglitch, UV falling	45	50	55	% of V_{REF}
Power good (PG) rising threshold	V_{PG_RISING}	V_{OUT} from low to high	85	90	95	% of V_{REF}
PG falling threshold	$V_{PG\_FALLING}$	V_{OUT} from high to low	75	80	85	% of V_{REF}
PG sink current capability	V_{PG_LOW}	Sink 4mA			0.4	V
PG leakage current	I_{PG_LKG}	V_{PULL} = 5V			5	µA
Thermal shutdown rising threshold [9]	T_{SD}			150		°C
Thermal hysteresis [9]	T_{SD_HYS}			20		°C
I^2C Specifications [9]						
Input logic high voltage	V_{IH}	Pull VDD up between 1.8V and 3.3V	1.4			V
Input logic low voltage	V_{IL}				0.4	V
Output voltage (V_{OUT}) logic low	V_{OUT_LOW}				0.4	V
SCL clock frequency	f_{SCL}			400	3400	kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DATA}		10			ns
Data hold time	t_{HD_DATA}		0	60		ns
Set-up time for (repeated) start condition	t_{SU_START}		160			ns
Hold time for (repeated) start condition	t_{HD_START}		160			ns
Bus free time between a start and a stop condition	t_{BUF}		160			ns
Set-up time for a stop condition	t_{SU_STOP}		160			ns
SCL and SDA rising time	t_{RISE}		10		300	ns
SCL and SDA falling time	t_{FALL}		10		300	ns
Suppressed spike pulse-width	t_{SP}		0		50	ns
Capacitance for each bus line	C_{BUS}				400	pF

Notes:

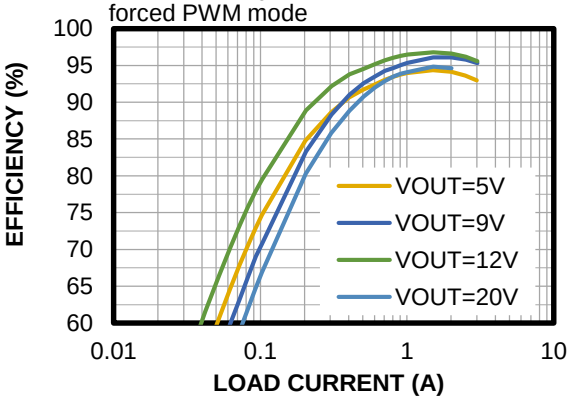
8) All minimum and maximum parameters are tested at T_J = 25°C. Over-temperature limits are guaranteed by design, characterization, and correlation.
9) Guaranteed by engineering sample characterization.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V to 20V, f_{SW} = 1.25MHz, T_A = 25°C, unless otherwise noted.

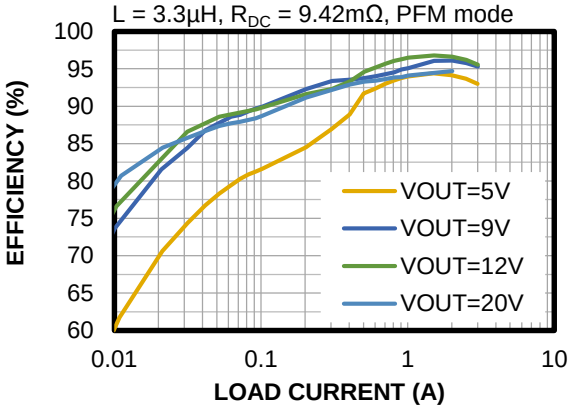
Efficiency vs. Load Current

V_{OUT} = 5V to 20V, f_{SW} = 1.25MHz,
L = 3.3µH, R_{DC} = 9.42mΩ,
forced PWM mode



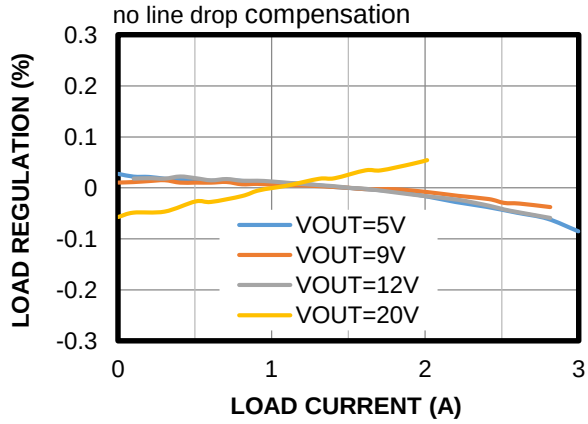
Efficiency vs. Load Current

V_{OUT} = 5V to 20V, f_{SW} = 1.25MHz,
L = 3.3µH, R_{DC} = 9.42mΩ, PFM mode



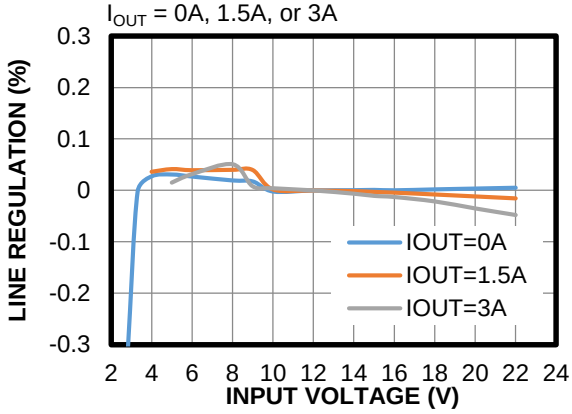
Load Regulation

V_{IN} = 12V; V_{OUT} = 5V, 9V, 12V, or 20V;
L = 3.3µH; I_{OUT} = 0A to 3A;
no line drop compensation



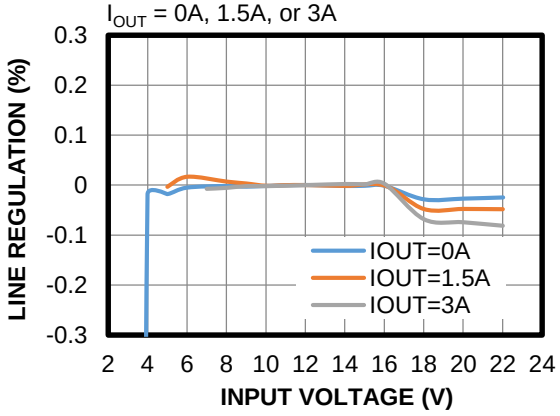
Line Regulation

V_{OUT} = 5V; L = 3.3µH;
I_{OUT} = 0A, 1.5A, or 3A



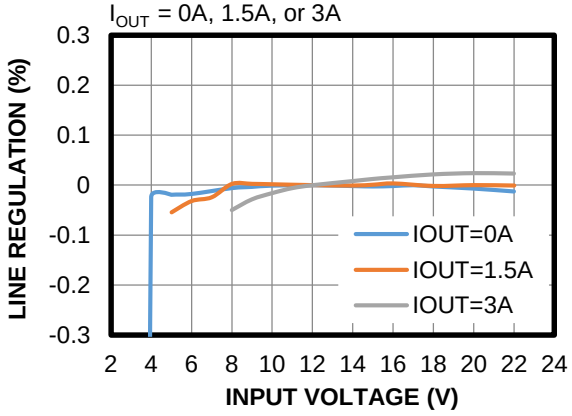
Line Regulation

V_{OUT} = 9V; L = 3.3µH;
I_{OUT} = 0A, 1.5A, or 3A



Line Regulation

V_{OUT} = 12V; L = 3.3µH;
I_{OUT} = 0A, 1.5A, or 3A



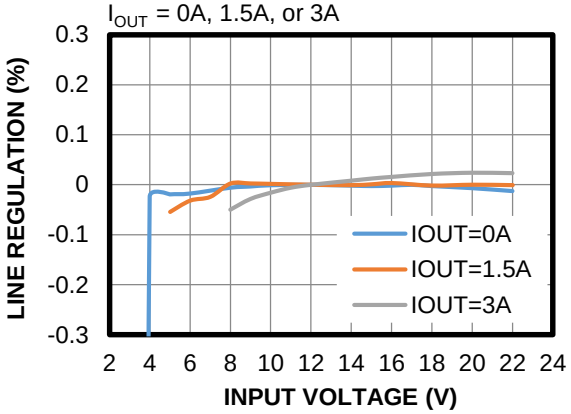
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V to 20V, f_{SW} = 1.25MHz, T_A = 25°C, unless otherwise noted.

Line Regulation

V_{OUT} = 12V; L = 3.3µH;

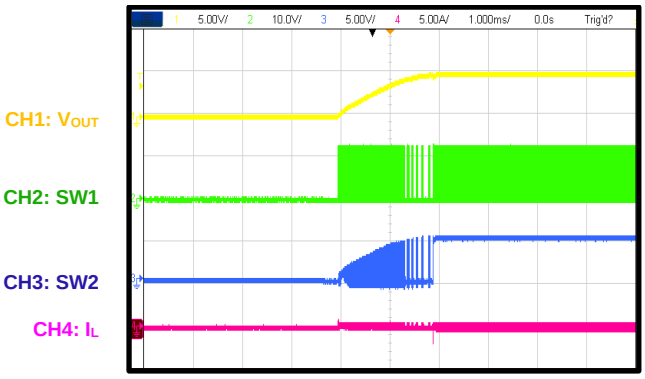
I_{OUT} = 0A, 1.5A, or 3A



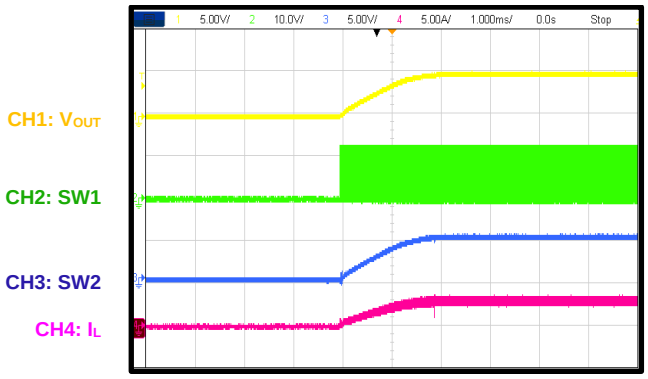
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH, f_{SW} = 1.25MHz, T_A = 25°C, the test waveforms are based on Figure 17 on page 30, unless otherwise noted.

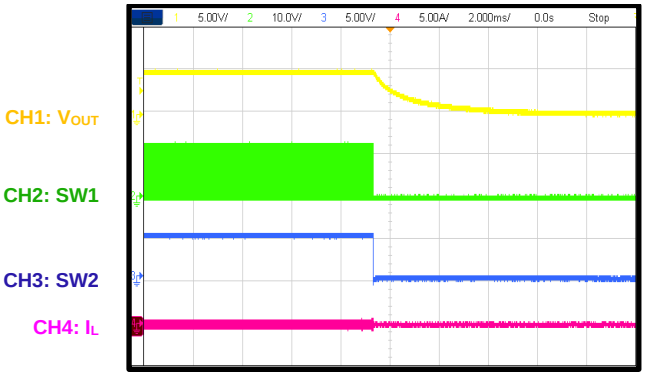
EN Bit Enabled through the I²C
I_{OUT} = 0A



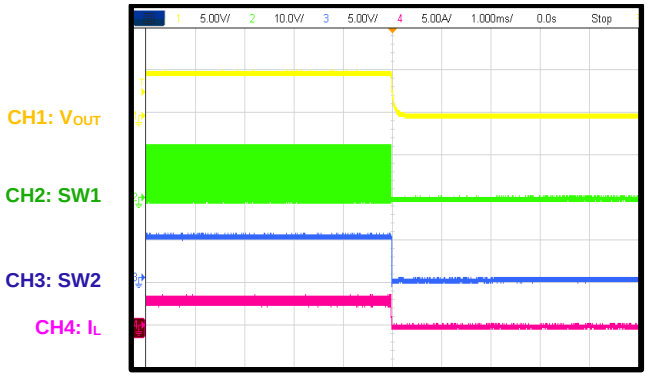
EN Bit Enabled through the I²C
I_{OUT} = 3A



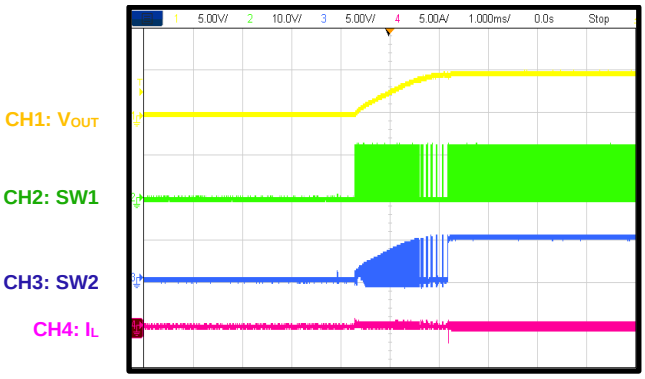
EN Bit Shutdown through the I²C
I_{OUT} = 0A



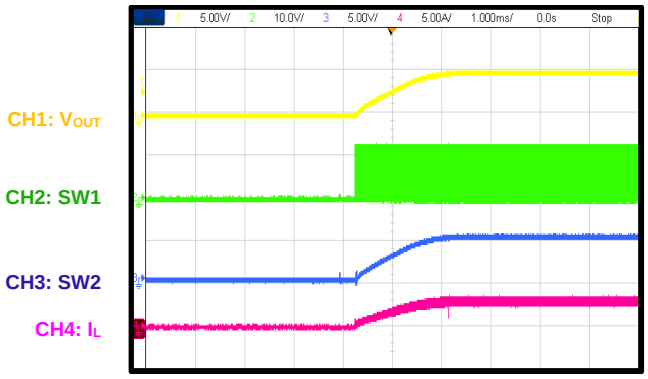
EN Bit Shutdown through the I²C
I_{OUT} = 3A



Start-Up through EN
I_{OUT} = 0A



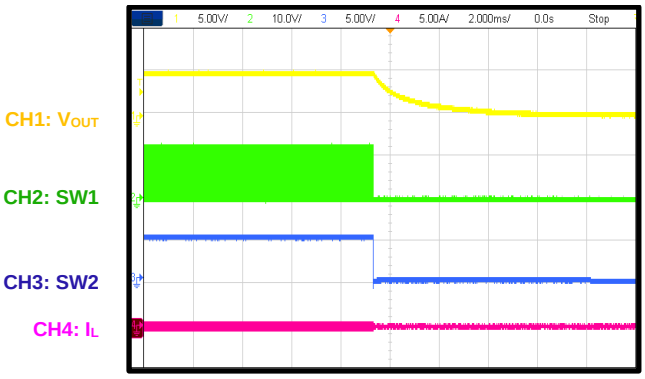
Start-Up through EN
I_{OUT} = 3A



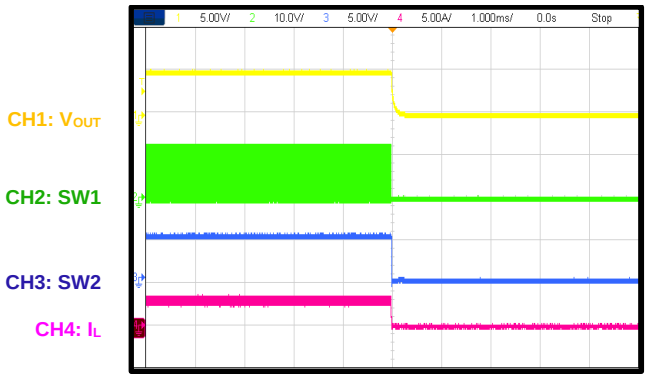
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH, f_{SW} = 1.25MHz, T_A = 25°C, the test waveforms are based on Figure 17 on page 30, unless otherwise noted.

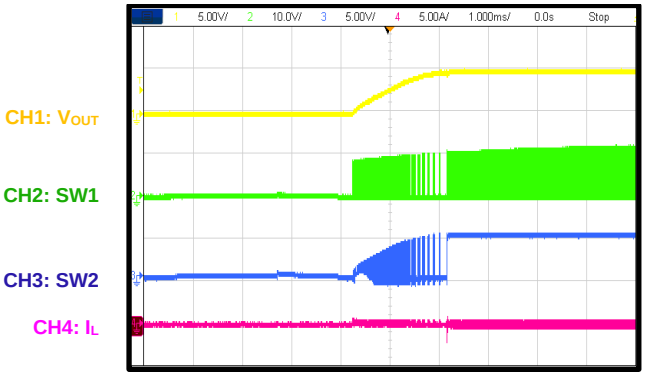
Shutdown through EN
I_{OUT} = 0A



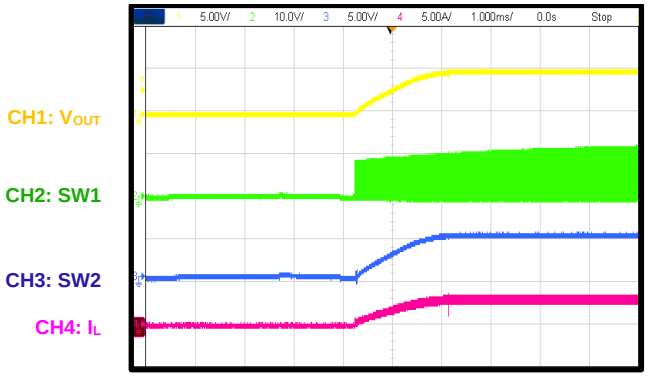
Shutdown through EN
I_{OUT} = 3A



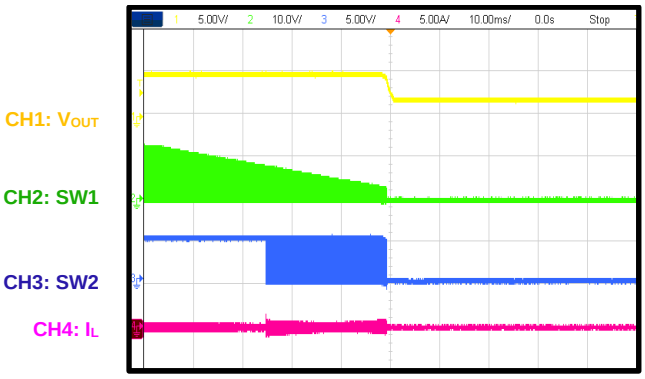
Start-Up through VIN
I_{OUT} = 0A



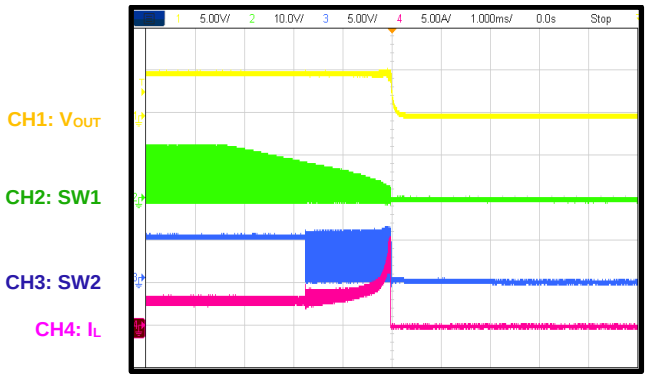
Start-Up through VIN
I_{OUT} = 3A



Shutdown through VIN
I_{OUT} = 0A



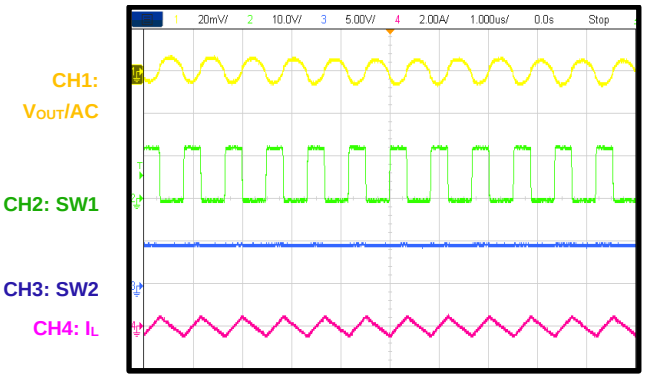
Shutdown through VIN
I_{OUT} = 3A



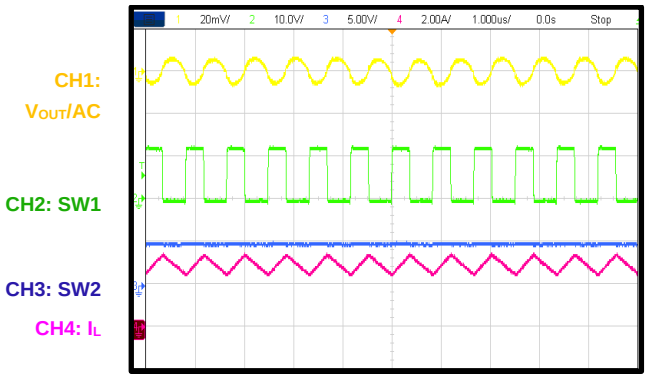
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH, f_{SW} = 1.25MHz, T_A = 25°C, the test waveforms are based on Figure 17 on page 30, unless otherwise noted.

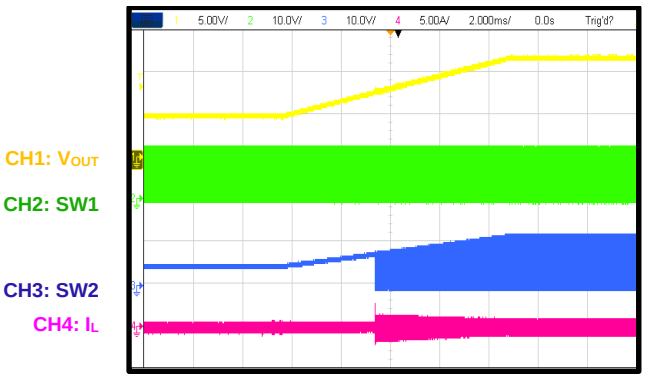
Steady State
I_{OUT} = 0A



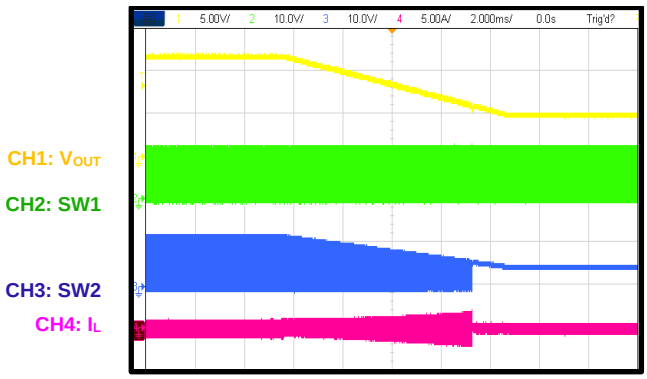
Steady State
I_{OUT} = 3A



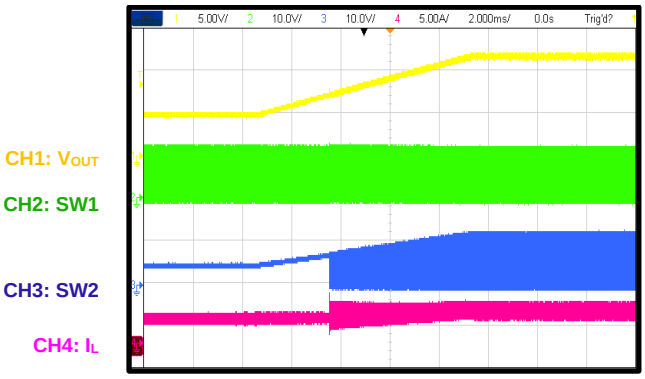
I²C VID
V_{OUT} = 5V to 12V, I_{OUT} = 0A



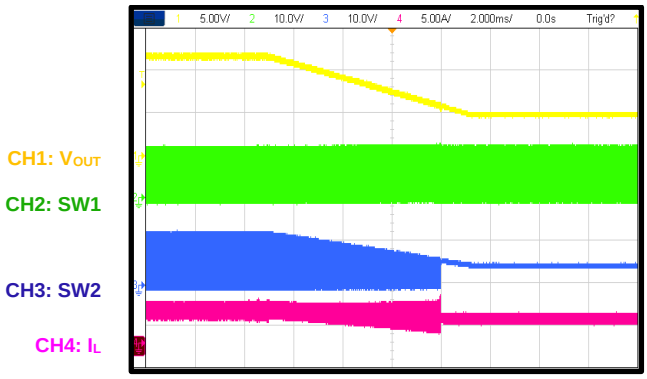
I²C VID
V_{OUT} = 12V to 5V, I_{OUT} = 0A



I²C VID
V_{OUT} = 5V to 12V, I_{OUT} = 3A



I²C VID
V_{OUT} = 12V to 5V, I_{OUT} = 3A

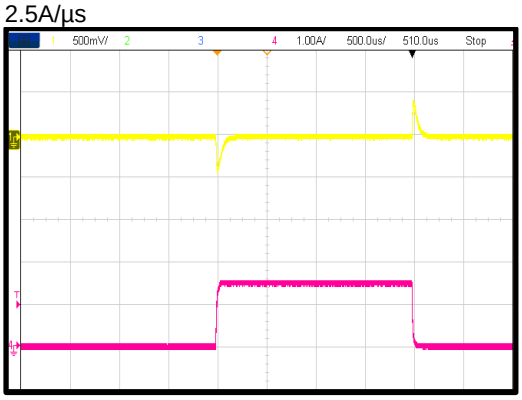


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH, f_{SW} = 1.25MHz, T_A = 25°C, the test waveforms are based on Figure 17 on page 30, unless otherwise noted.

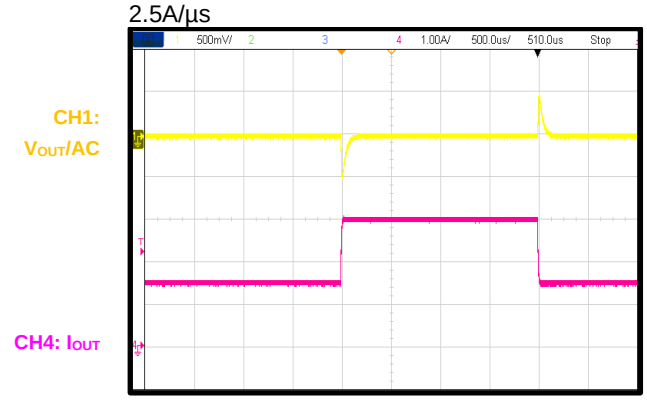
Load Transient

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A to 1.5A, E-load 2.5A/µs

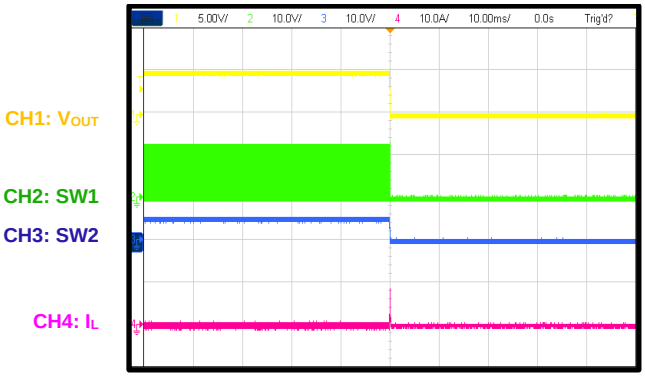


Load Transient

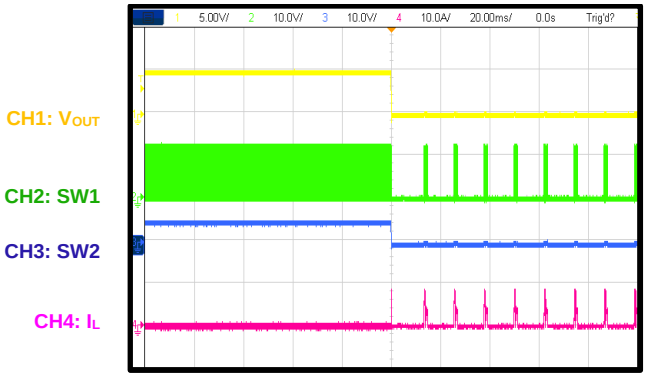
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.5A to 3A, E-load 2.5A/µs



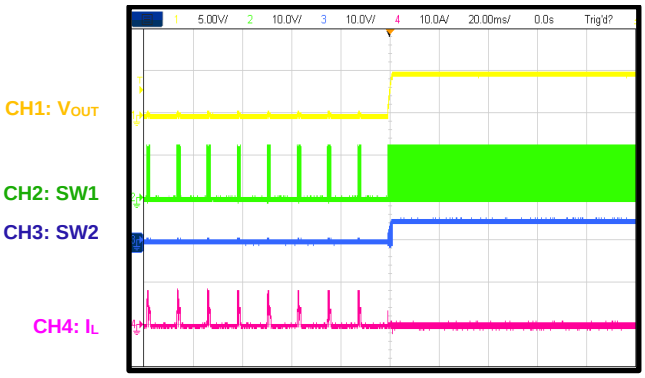
Short-Circuit Protection Entry with Latch-Off Mode



Short-Circuit Protection Entry with Hiccup Mode

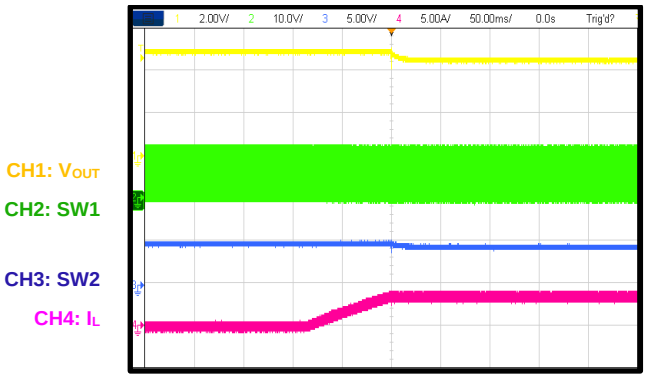


Short-Circuit Protection Recovery with Hiccup Mode



CC Current Limit Entry

E-load CV mode

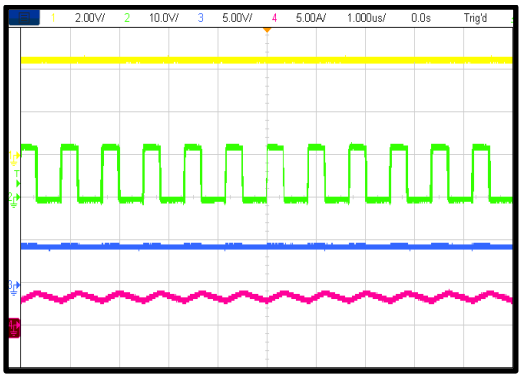


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

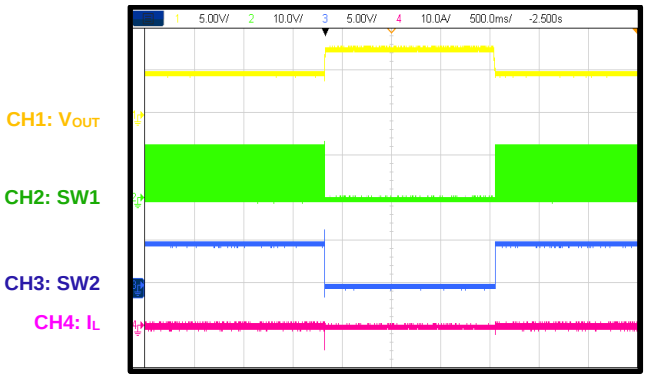
V_{IN} = 12V, V_{OUT} = 5V, L = 2.2µH, f_{SW} = 1.25MHz, T_A = 25°C, the test waveforms are based on Figure 17 on page 30, unless otherwise noted.

CC Current Limit Steady State

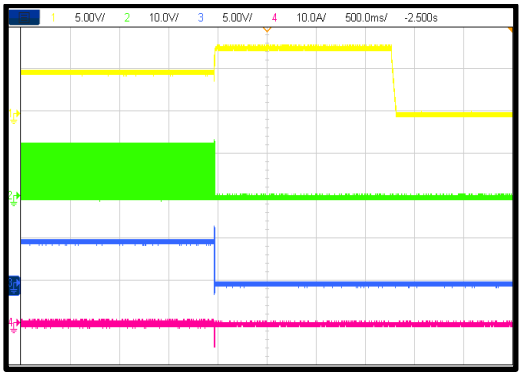
E-load CV mode



V_{OUT} OVP with Hiccup Mode



V_{OUT} OVP with Latch-Off Mode



FUNCTIONAL BLOCK DIAGRAM

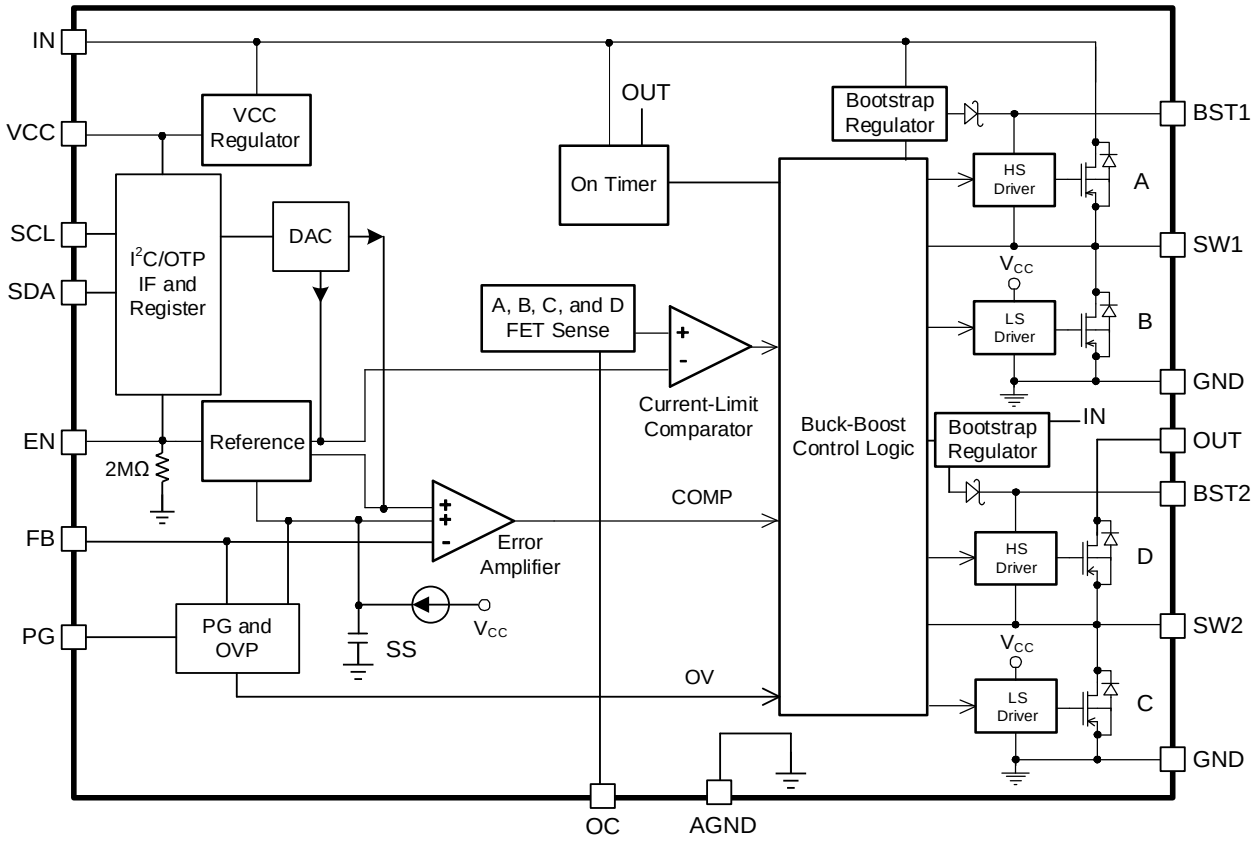


Figure 2: Functional Block Diagram

OPERATION

The MP28167-B is a four-switch, integrated buck-boost converter that can operate in constant-on-time (COT) control mode with a fixed frequency. This provides fast transient response for buck, boost, and buck-boost mode. A special buck-boost control strategy provides high efficiency across the entire input voltage (V_{IN}) range and smooth transient between different modes.

Buck-Boost Operation

The MP28167-B can regulate the output voltage (V_{OUT}) to be above, equal to, or below V_{IN}. Figure 3 shows a power structure with one inductor and the four switches.

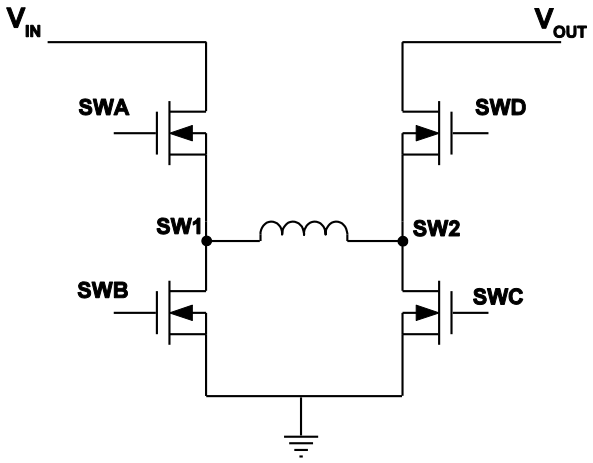


Figure 3: Buck-Boost Topology

The MP28167-B can operate in buck mode, boost mode, or buck-boost mode with different inputs (see Figure 4).

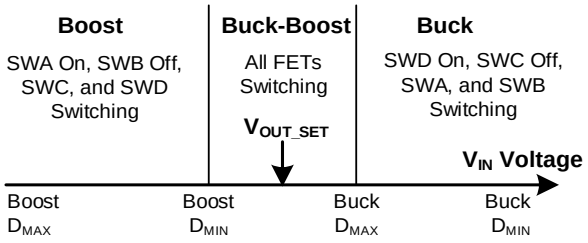


Figure 4: Buck-Boost Operating Range

Buck Mode

When V_{IN} is significantly higher than V_{OUT}, the MP28167-B works in buck mode. In buck mode, switch A (SWA) and switch B (SWB) switch for buck regulation. Switch C (SWC) is off, and switch D (SWD) remains on to conduct the inductor current (I_L).

SWA works with COT control, and SWB turns on as a complement of SWA. In each cycle, SWB turns on to conduct I_L.

When I_L drops to the COMP voltage (V_{COMP}), SWB turns off and SWA turns on. SWA turns on for a fixed on time before turning off. Then SWB turns on again, and the operation repeats. The COMP signal is the error amplifier (EA) output from the output feedback voltage (V_{FB}) and the internal reference voltage (V_{REF}) (see Figure 5).

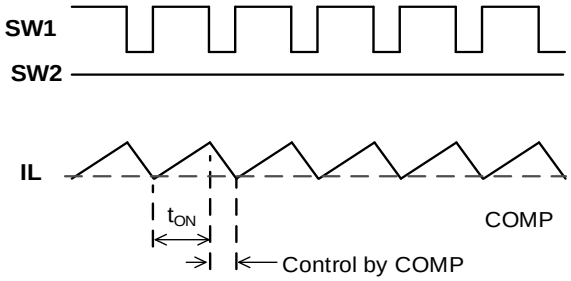


Figure 5: Buck Waveform

Boost Mode

When V_{IN} is significantly lower than V_{OUT}, the MP28167-B works in boost mode. In boost mode, SWC and SWD switch for boost regulation. SWB is off, and SWA remains on to conduct I_L.

During each period, SWC remains off with COT control, while SWD turns on as a complement of SWC to boost I_L to the output. In each cycle, SWC turns on to conduct I_L. When I_L rises and reaches V_{COMP}, SWC turns off and SWD turns on. SWC turns off with a fixed off time before turning on again. During this period, SWD turns on for the current freewheel (see Figure 6).

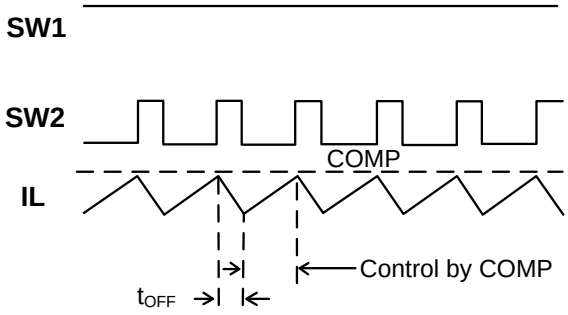


Figure 6: Boost Waveform

Buck-Boost Mode

When V_{IN} is almost equal to V_{OUT}, the MP28167-B cannot provide enough energy to operate in buck mode due to SWA's minimum off time, or it supplies too much power to V_{OUT} in boost mode due to SWC's minimum on time. The IC uses buck-boost control to regulate V_{OUT} in these conditions.

If V_{IN} drops and the SWA off period is close to the minimum buck off time in buck mode, buck-boost mode is engaged. When the next cycle starts after the SWA and SWD on time (the buck high-side MOSFET [HS-FET] on period), boost starts with SWA and SWC on (the boost low-side MOSFET [LS-FET] on period).

SWA and SWD turn on again for the remainder of boost mode (boost HS-FET on). After the boost period elapses, the buck period starts, and SWB and SWD remain on until I_L drops to V_{COMP}. Then SWA and SWD turn on until the next boost period begins. Buck and boost switching work with a one-interval period. This is called buck-boost mode.

If V_{IN} rises and the SWC on time is close to the boost minimum on time in boost mode, then buck-boost mode is enabled. After the boost constant-off-time period (SWA and SWD on), SWB and SWD remain on until I_L drops to V_{COMP}, similar to buck off-time control.

Once I_L triggers V_{COMP}, SWA and SWD turn on for the buck on time, which is followed by boost switching (SWA and SWC on). Buck and boost switching work with a one-interval period. Figure 7 shows the buck-boost waveform when V_{IN} exceeds V_{OUT}.

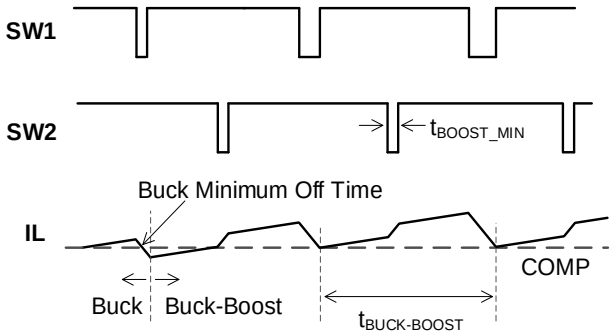


Figure 7: Buck to Buck-Boost Transient

Figure 8 shows the buck-boost waveform when V_{OUT} exceeds V_{IN}.

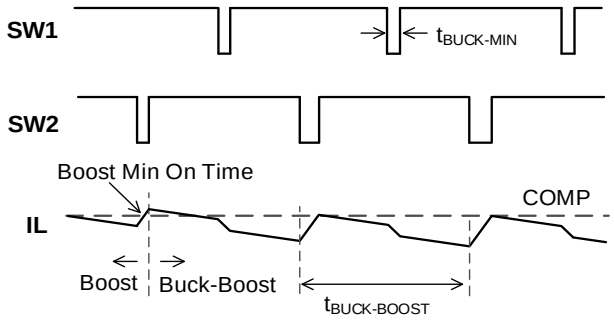


Figure 8: Buck-Boost Waveform

If V_{IN} exceeds 130% of V_{OUT} in buck-boost mode, the MP28167-B switches from buck-boost mode to buck mode. If V_{IN} drops below 20% of V_{OUT}, the MP28167-B switches from buck-boost mode to boost mode.

Operation Mode Selection

The MP28167-B operates with a fixed frequency under heavy-load conditions. When the load current decreases, the MP28167-B can work in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM) based on the MODE register setting.

Forced Continuous Conduction Mode (FCCM) (or Forced PWM)

In FCCM (also called forced pulse-width modulation [Forced PWM] mode), the buck on time and boost off time are determined by the internal circuit. This achieves a fixed frequency based on the V_{IN} / V_{OUT} ratio. As the load decreases, the average input current (I_{IN}) drops, and I_L may go negative from V_{OUT} to V_{IN} during the off time (SWD on). This forces I_L to work in continuous mode with a fixed frequency, producing a lower V_{OUT} ripple (ΔV_{OUT}) than in PSM.

Pulse-Skip Mode (PSM)

If I_L drops to 0A in PSM (also called automatic pulse-frequency modulation [PFM]/PWM mode), SWD turns off to prevent the current from flowing from V_{OUT} to V_{IN}, forcing I_L to work in discontinuous conduction mode (DCM). Meanwhile, the internal off time clock stretches once the MP28167-B enters DCM. The frequency drops when the I_L conduction period decreases, which helps save power and reduce ΔV_{OUT}.

If V_{COMP} drops to the PSM threshold (even if the IC stretches the frequency), the MP28167-B

stops switching to further decrease the switching power loss.

The MP28167-B recovers switching once V_{COMP} exceeds the PSM threshold. The switching pulse skips based on V_{COMP} under very light-load conditions. PSM has much higher efficiency at light loads than FCCM; however, ΔV_{OUT} may be higher due to the group switching pulse.

Internal VCC Regulator

The 3.65V internal regulator powers most of the internal circuitry. This regulator takes V_{IN} and operates across the entire V_{IN} range. When V_{IN} exceeds 3.65V, the regulator output is in full regulation. If V_{IN} drops below 3.65V, the output decreases with V_{IN}. Decouple VCC using an external 1µF ceramic capacitor.

Enable (EN) Control

The MP28167-B has an enable (EN) control pin. Pull EN high to enable the IC. Pull EN low or float EN to disable the IC.

If EN is pulled down when the output discharge function is enabled, the MP28167-B shuts down after 55ms. The MP28167-B's I^2C register value is reset to default only after the MP28167-B experiences this type of shutdown. If EN is pulled high within 55ms, the I^2C register is not reset, and the MP28167-B enables the output with the previous register setting.

If the output discharge function is disabled, the MP28167-B shuts down once EN is pulled down for more than 100µs, and the MP28167-B I^2C register is reset after a 100µs delay.

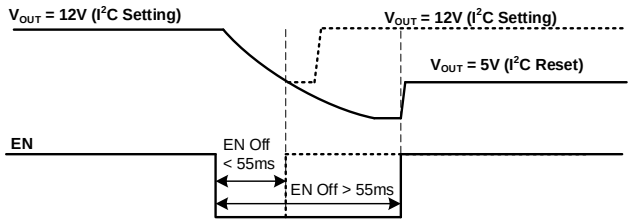


Figure 9: EN On/Off Logic for I^2C Register Reset

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors V_{IN} and enables or disables the entire IC.

Internal Soft Start (SS)

Soft start (SS) prevents the converter's V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 3.65V. If V_{SS} is below V_{REF}, the EA uses V_{SS} as the reference. If V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference.

If the MP28167-B's output is pre-biased to a certain voltage during start-up, the IC disables both HS-FET and LS-FET switching until V_{SS} exceeds the internal feedback voltage (V_{FB}) (see Figure 10).

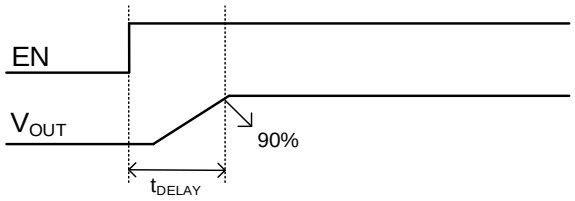


Figure 10: EN On to V_{OUT} > 90% Delay

Power Good (PG)

The MP28167-B uses a power good (PG) output to indicate whether V_{OUT} is ready. PG is an open-drain output. Connect PG to VCC or another voltage source below 5.5V using a pull-up resistor (e.g. 100kΩ). When V_{IN} is applied, PG is pulled down to GND before the internal SS is ready. When V_{OUT} is above 90% of V_{REF}, PG is pulled high once.

During normal operation, PG is pulled low when V_{OUT} drops below 80% of V_{REF} or V_{OUT} is exceeds 160% of V_{REF}.

During UVLO, if EN is low or over-temperature protection is triggered, PG is pulled low immediately. During an over-current (OC) condition, PG is pulled low when V_{OUT} drops below 80% of V_{REF}. During an over-voltage (OV) condition, PG is pulled low when V_{OUT} exceeds 160% of V_{REF}.

Over-Current Protection (OCP)

The MP28167-B has a constant-current limit control loop to limit the average output current (I_{OUT}). The current information is sensed from SWA, SWB, SWC, and SWD. Then an average algorithm calculates I_{OUT}.

When I_{OUT} exceeds the current-limit threshold, V_{OUT} starts to drop.

There are two conditions that can cause this:

1. When V_{OUT} exceeds 3V, V_{FB} drops below 50% of V_{REF}, and V_{OUT} drops below 3V, then the MP28167-B enters hiccup mode or latch-off mode according to the I^2C setting.
2. When V_{OUT} is below or equal to 3V, and V_{OUT} drops below the under-voltage protection (UVP) threshold (typically 50% below V_{REF}), then the MP28167-B enters hiccup mode or latch-off mode according to the I^2C setting.

In hiccup mode, the MP28167-B stops switching and recovers automatically with 12.5% duty cycles. In latch-off mode, the MP28167-B stops switching until the IC restarts. Restart the part by cycling the power on VIN or EN, or toggling the EN bit.

Over-Voltage Protection (OVP)

The MP28167-B monitors a resistor-divided V_{FB} to detect output over-voltage (OV) conditions. When V_{FB} exceeds 160% of the target voltage, the over-voltage protection (OVP) comparator output goes high, and the output-to-ground discharge resistor turns on.

The OUT pin has an absolute OVP function. Once V_{OUT} exceeds the absolute OVP threshold (23V), the MP28167-B stops switching and turns on the output-to-ground discharge resistor.

Start-Up and Shutdown

If both V_{IN} and the EN voltage (V_{EN}) exceed their respective thresholds, the chip is enabled. The reference block starts up first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitry.

Three events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Output Discharge

The MP28167-B has an output discharge function that provides a resistive discharge path for the external output capacitor (C_{OUT}). The function is active when the part is disabled (V_{IN} is below the UVLO threshold or EN is off). The discharge path turns off when V_{OUT} is below 50mV or 50ms (the maximum timer) has elapsed. This function can also be disabled via the I^2C.

Thermal Warning and Thermal Shutdown

Thermal warning and thermal shutdown prevent the part from operating at exceedingly high temperatures. When the silicon die temperature exceeds 120°C, the MP28167-B sets the OTW bit [D5] to 1. When the temperature falls below its lower threshold (typically 100°C), the OTW bit [D5] is set to 0.

When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled. This is a non-latch protection.

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage (V_{BUS}) externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence.

The MP28167-B interface is an I²C slave that supports fast mode (400kHz) and high-speed mode (3.4MHz). The I²C interface adds flexibility to the power supply solution. The output voltage (V_{OUT}), transition slew rate, and other parameters can be controlled instantaneously via the I²C interface.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by a 0 to indicate a write operation, or a 1 to indicate a read operation.

Start and Stop Conditions

The start and stop conditions are signaled by the master device, which signifies the beginning and end of an I²C transfer. The start (S) condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop (P) condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 11).

The master then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit on the SDA line.

Data Transfer

Data is transferred in 8-bit bytes by the SDA line. Each byte of data should be followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MP28167-B requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. The MP28167-B acknowledges that it has received each byte by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP28167-B. The MP28167-B performs an update on the falling edge of the least significant bit (LSB) byte. See Figure 12, Figure 13, and Figure 14 for examples of the I²C write and read sequences.

I²C Start-Up Timing

I²C functionality is enabled once EN is active and the input voltage (V_{IN}) exceeds the under-voltage lockout (UVLO) threshold. The I²C works during over-current protection (OCP), over-voltage protection (OVP), and thermal shutdown.

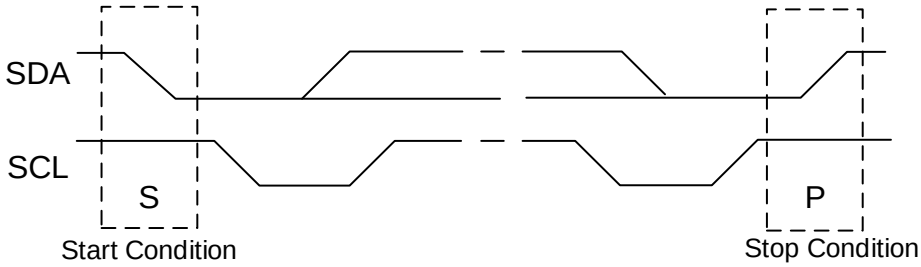


Figure 11: Start and Stop Conditions

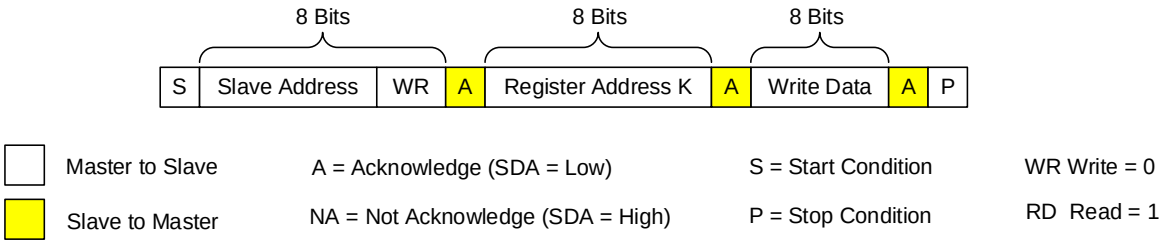


Figure 12: I²C Write Example (Single-Register Write)

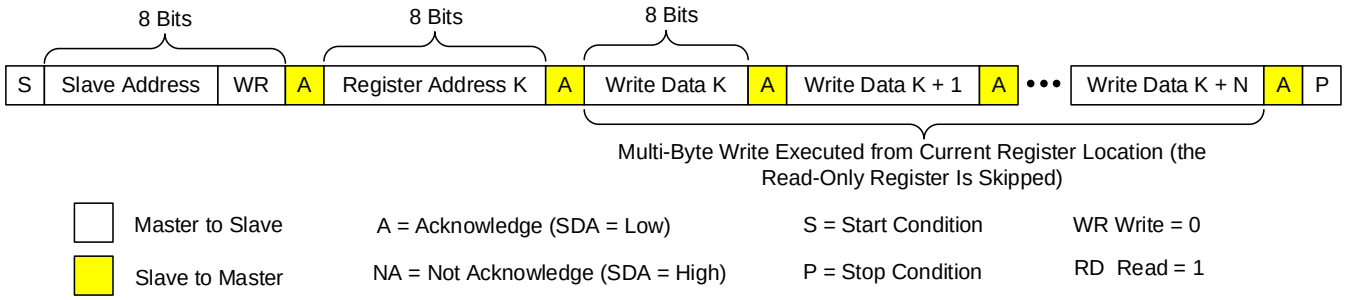


Figure 13: I²C Write Example (Multi-Register Write)

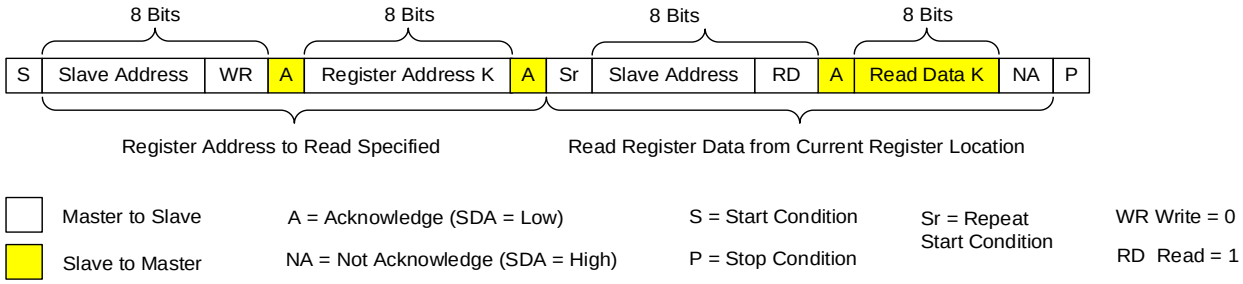


Figure 14: I²C Read Example (Single-Register Read)

I²C REGISTER MAP

Add (Hex)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VREF_L	R/W	RESERVED					VREF DATA BIT LOW [2:0] (10)		
01	VREF_H	R/W	VREF DATA BIT HIGH [10:3] (10)							
02	VREF_GO	R/W	RESERVED						PG_DELAY_EN (10)	GO_BIT
03	IOUT_LIM	R/W	RESERVED	Output current limit threshold (0A to 6.35A/50mA step for 21.5kΩ OC resistor) (10)						
04	CTL1	R/W	EN (10)	HICCUP OCP_OVP (10)	DISCHG_EN (10)	MODE (10)	FREQ (10)		RESERVED	
05	CTL2	R/W	LINE DROP COMP (10)		SS (10)		RESERVED			
06	RESERVED	R	RESERVED, ALL “0”						RESERVED	
07	RESERVED	R	RESERVED							
08	RESERVED	R	RESERVED							
09	STATUS	R	PG	OTP	OTW	CC_CV	RESERVED			
0A	INTERRUPT	W1C (11)	OTEMPP_ENTER	OT WARNING_ENTER	OC_ENTER	OC_RECOVER	UVP_FALLING	OTEMPP_EXIT	OT WARNING_EXIT	PG_RISING
0B	MASK	R/W	RESERVED			OTPMSK (10)	OTWMSK (10)	OC_MSK (10)	UVP_MSK (10)	PG_MSK (10)
0C	ID1	R	OTP configuration code. “0x00” means the standard MP28167-B							
27	MFR_ID	R	Manufacturer ID: b ‘0000 1001’							
28	DEV_ID	R	Device ID: b ‘0101 1000’							
29	IC_REV	R	IC revision: b ‘0000 0001’							

Notes:

10) These items have a one-time programmable (OTP) non-volatile memory. The OTP is reloaded to the I²C register when V_{IN} exceeds the under-voltage lockout (UVLO) threshold, or during EN shutdown.

11) Write “0xFF” to this register to reset the interrupt.

REGISTER DESCRIPTION

I²C Bus Slave Address

The MP28167-B I²C slave address is fixed at 60h.

Output Reference Voltage (V_{REF}) Setting (00h~01h)

The VREF_L (00h) and VREF_H (01h) registers set the 11-bit reference voltage (V_{REF}) in direct format. VREF_H [7:0] sets VREF[10:3], and VREF_L [2:0] sets VREF[2:0].

VREF_L (00h)

Bit	Bit Name	Default	Description
D[2:0]	VREF_L	011	Sets VREF[2:0].

VREF_H (01h)

Bit	Bit Name	Default	Description
D[7:0]	VREF_H	0101 0100	Sets VREF[10:3].

V_{REF} can be calculated with Equation (1):

$$V_{REF}\ (mV) = V \times 0.8 \quad (1)$$

Where V is an 11-bit unsigned binary integer of VREF[10:0] between 0 and 2047.

The V_{REF} resolution is 0.8mV/LSB. The V_{REF} changing slew rate is fixed at 1mV/µs. See the VREF_GO Register (02h) section below to change V_{REF}. If V is set at its default value (675), then the default V_{REF} is 540mV (calculated with Equation 1).

VREF_GO (02h)

The VREF_GO register sets the power good (PG) rising delay time. It also sets when the output reference change starts.

Bits	Bit Name	Default	Description
D[1]	PG_DELAY_EN	0	Sets the power good (PG) rising delay time. 0: No delay 1: 100µs rising delay
D[0]	GO_BIT	0	Sets when the output reference change starts. 0: V_{REF} does not change 1: The output reference change starts according to the VREF register, and automatically resets to 0 when the change is complete

The MP28167-B can be controlled when V_{REF} begins to change. Set GO_BIT to 1 to start the output reference change according to the VREF register. When the V_{REF} change is complete (the internal V_{REF} reaches its target value), GO_BIT automatically resets to 0. This prevents a false operation of V_{REF} scaling.

Write V_{REF} (registers 00h and 01h) first, and then write GO_BIT = 1. V_{REF} changes according to the new register setting. GO_BIT resets to 0 when V_{REF} reaches a new value. The host can read GO_BIT to determine whether V_{REF} scaling is complete.

The V_{OUT}-to-ground discharge function is enabled when GO_BIT = 1. This ramps V_{OUT} from high to low under light-load conditions.

When GO_BIT = 0, V_{REF} does not change. When GO_BIT = 1, V_{REF} changes according to the V_{REF} register setting. After V_{REF} scaling finishes, GO_BIT is automatically reset to 0.

When PG_DELAY_EN = 0, there is no PG delay. When PG_DELAY_EN = 1, PG has a 100µs rising delay. The default value is 0.

IOUT_LIM (03h)

The IOUT_LIM register sets the output current limit (I_{OUT_LIMIT}).

Bits	Bit Name	Default	Description
D[6:0]	IOUT_LIM	100 0110	Sets the output current limit (I_{OUT_LIMIT}).

IOUT_OC can be calculated with Equation (2):

$$IOUT\_OC\ (A) = IOUT\_LIM \times 0.05 \quad (2)$$

Where IOUT_LIM is a 7-bit unsigned binary integer of IOUT_LIM D[6:0], and the IOUT_OC resolution is 50mA/LSB (6.35A maximum).

There are two methods to change I_{OUT_LIMIT}. The first method is to use a 21.5kΩ resistor connected from the OC pin to ground to adjust I_{OUT_LIMIT} via the IOUT_LIM register. Then I_{OUT_LIMIT} can be calculated with Equation 2. The default value is 3.5A. A 22nF filter capacitor on the OC pin is required to keep the constant current (CC) loop stable. The MP28167-B allows IOUT_LIM to be directly changed using the I^2C. If the CC threshold must be changed after the MP28167-B has already entered the CC limit operating state, it is recommended to change the CC threshold step by step (e.g. 50mA/step) instead of changing the current value to the final value.

The second method is to change the resistor connected from the OC pin to ground to set the over-current (OC) limit between 1A and 6.5A, while maintaining the default IOUT_LIM value. A filter capacitor on the OC pin is required to keep the CC loop stable. Table 1 shows the OC resistance (R_{OC}) and OC capacitance (C_{OC}) combinations for different current limit settings.

Table 1: Resistor and Capacitor Selection for Different Output Current Limit Settings

R_{OC} (kΩ)	75	64.9	54.9	44.2	37.4	30	21.5	15
C_{OC} (nF)	6.8	6.8	8.2	10	12	15	22	33
I_{OUT_LIMIT} (A)	1	1.16	1.37	1.7	2	2.5	3.5	5

CTL1 (04h)

The CTL1 register sets the enable bit (EN), the over-current protection (OCP) mode, over-voltage protection (OVP) mode, output discharge enable bit (DISCHG_EN), pulse-frequency modulation (PFM)/pulse-width modulation (PWM) mode, and switching frequency (f_{SW}).

Bits	Bit Name	Default	Description
D[7]	EN	1	I^2C-controlled bit that turns the part on and off. When the external EN pin is low, the converter is off, and the I^2C shuts down. When EN is high, the EN bit takes over. 0: Disabled 1: Enabled
D[6]	HICCUP_OCP_OVP	1	Selects the over-current protection (OCP) and over-voltage protection (OVP) mode. 0: Latch-off mode 1: Hiccup mode
D[5]	DISCHG_EN	1	Enables output discharge. 0: No output discharge occurs during shutdown 1: Output discharge occurs during EN or VIN shutdown
D[4]	MODE	1	Enables pulse-frequency modulation (PFM)/pulse-width modulation (PWM) mode. The default is PWM mode under light-load conditions. 0: Enables auto-PFM/PWM mode 1: Enables forced PWM mode

D[3:2]	FREQ	11	Sets the switching frequency (f_{SW}). 00: 500kHz 01: 750kHz 10: 1MHz 11: 1.25MHz

CTL2 (05h)

The CTL2 register sets the output voltage (V_{OUT}) compensation and soft-start time (t_{SS}).

Bits	Bit Name	Default	Description
D[7:6]	LINE_DROP_COMP	00	Sets the output voltage (V_{OUT}) compensation (V_{LINE} vs. the load feature). 00: No compensation 01: V_{OUT} compensates 60mV when I_{OUT} = 3A 10: V_{OUT} compensates 120mV when I_{OUT} = 3A 11: V_{OUT} compensates 200mV when I_{OUT} = 3A V_{OUT} compensation is based on R1 and R2. The compensated voltage (V_{LINE}) can be calculated with the following equation: $V_{LINE} = (1 + R1 / R2) \times V_{REF\_LINE}$ Where V_{REF_LINE} = 0mV, 12mV, 24mV, or 40mV when the D[7:6] bits = 00, 01, 10, or 11, respectively.
D[5:4]	SS	10	Sets the output start-up soft-start time (t_{SS}) (from 0% to 100%). If V_{REF} = 1V, then: 00: 1.1ms 01: 2.2ms 10: 3.5ms 11: 4.4ms The soft-start slew rate is constant; however, t_{SS} changes with different V_{REF}. For example, t_{SS} = 3.5ms when V_{REF} = 1V, and t_{SS} = 5.25ms when V_{REF} = 1.5V.

STATUS (09h)

The STATUS register indicates the instantaneous status of PG, over-temperature protection, over-temperature warning (OTW), and constant-current (CC) or constant-voltage (CV) mode. These status bits indicate the instantaneous values.

Bit	Bit Name	Default	Description
D[7]	PG	N/A	Indicates the output PG status. 0: Output power is not good 1: Output power is good
D[6]	OTP	N/A	Indicates the over-temperature protection status. 0: Over-temperature protection has not occurred 1: Over-temperature protection has occurred
D[5]	OTW	N/A	Indicates the over-temperature warning (OTW) status. 0: OTW has not occurred 1: OTW has occurred
D[4]	CC_CV	N/A	Enables constant-current (CC) or constant-voltage (CV) output mode. 0: CV mode 1: CC mode

INTERRUPT (0Ah)

The INTERRUPT register indicates the chip's status. When any status occurs, the relevant bit latches. The interrupt can be cleared by writing "0xFF" to this register.

Bits	Bit Name	Description
D[7]	OTEMPP_ENTER	Indicates an over-temperature protection entry. When this bit is high, the IC enters thermal shutdown. This bit is not masked, even if OTPMSK = 1.
D[6]	OTWARNING_ENTER	Indicates a die temperature early warning entry. When this bit is high, the die temperature exceeds 120°C. This bit is not masked, even if OTWMSK = 1.
D[5]	OC_ENTER	Indicates an over-current (OC) or CC limit mode entry.
D[4]	OC_RECOVER	Indicates from CC limit mode recovery.
D[3]	UVP_FALLING	Indicates that the internal feedback voltage (V_{FB}) is below the under-voltage protection (UVP) threshold.
D[2]	OTEMPP_EXIT	Indicates that over-temperature protection (OTP) has ended.
D[1]	OTWARNING_EXIT	Indicates a die temperature early warning exit. When the die temperature is below 100°C, this bit is set to 1. This bit is not masked, even if OTWMSK = 1.
D[0]	PG_RISING	Indicates an output PG rising edge.

MSK (0Bh)

The MSK register masks over-temperature protection, OTW, OCP, UVP, and PG indication.

Bit	Bit Name	Default	Description
D[4]	OTPMSK	1	Set OTPMSK to 1 to mask over-temperature protection.
D[3]	OTWMSK	1	Masks the over-temperature warning.
D[2]	OC_MSK	1	Masks OCP and CC entry and recovery.
D[1]	UVP_MSK	1	Masks the output UVP interrupt.
D[0]	PG_MSK	1	Masks PG indication. 1: The PG pin does not indicate a PG event 0: The PG indicates a PG rising event

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (V_{OUT}). R1 can be calculated with Equation (1):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (1)$$

Figure 15 shows the feedback (FB) circuit.

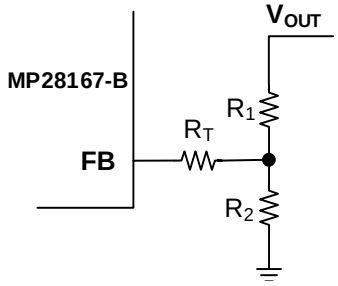


Figure 15: Feedback Network

Table 2 lists the recommended resistors and inductance for common V_{OUT}. If the I^2C is not used to set V_{OUT}, the voltage can also be set using the resistors below.

Table 2: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	L (µH)
5	402	48.7	806	2.2
12	402	18.7	806	3.3
15	402	15	402	3.3
20	402	11	402	3.3

Selecting the Inductor

MPL Optimized Performance with MPS Inductor MPL-AL6050 Series

The inductor should be chosen according to the operation mode. The inductance in buck mode (L_{BUCK}) can be estimated with Equation (2):

$$L_{BUCK} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (2)$$

Where ΔI_L is the peak-to-peak inductor ripple current (between 30% and 50% of the maximum load current).

In boost mode, the inductor should be chosen to limit the peak-to-peak current ripple (ΔI_L) between 30% and 50% of the maximum input current (I_{IN}).

The target inductance in boost mode can be estimated with Equation (3):

$$L_{BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (3)$$

A larger-value inductor reduces the ripple current; however, it also has a larger physical size. A larger-value inductor also reduces the converter's bandwidth by moving the right half-plane zero to lower frequencies. This tradeoff should be determined based on the application requirements.

In addition to the inductance, the inductor must support the peak current to avoid saturation.

The peak current in buck mode (I_{PEAK_BUCK}) can be calculated with Equation (4):

$$I_{PEAK\_BUCK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{2 \times V_{IN\_MAX} \times f_{SW} \times L} \quad (4)$$

The peak current in boost mode (I_{PEAK_BOOST}) can be calculated with Equation (5):

$$I_{PEAK\_BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN\_MIN}} + \frac{V_{IN\_MIN} \times (V_{OUT} - V_{IN\_MIN})}{2 \times V_{OUT} \times f_{SW} \times L} \quad (5)$$

Where η is the MP28167-B's estimated efficiency.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 3 lists recommended power inductors.

Table 3: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
Select family series (MPL-AL)	2.2µH to 4.7µH	MPS
MPL-AL6050-4R7	4.7µH	MPS
MPL-AL6050-3R3	3.3µH	MPS
MPL-AL5030-2R2	2.2µH	MPS

Visit MonolithicPower.com for more information.

Selecting the Input and Output Capacitors

It is recommended to use ceramic capacitors with an electrolytic capacitor at the input to filter the input ripple current and achieve stable operation.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires sufficient capacitance. For most applications, a 100µF electrolytic capacitor and a 22µF ceramic capacitor are sufficient.

The output capacitor (C_{OUT}) stabilizes the DC V_{OUT}. Choose a sufficient capacitance to limit the V_{OUT} ripple (ΔV_{OUT}). The minimum ceramic C_{OUT} should be 22µF x 5.

The input and output ceramic capacitors should be placed as close to the device as possible.

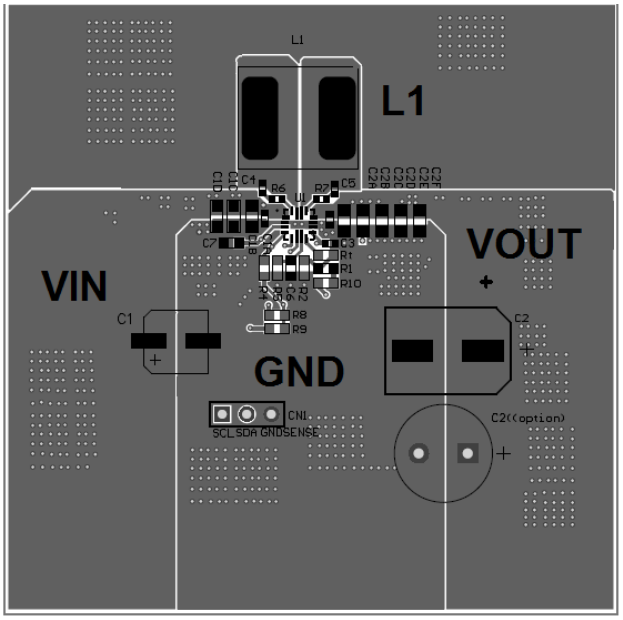
PCB Layout Guidelines (12)

Efficient PCB layout is critical for stable operation and thermal dissipation. For the best results, refer to Figure 16 and follow the guidelines below:

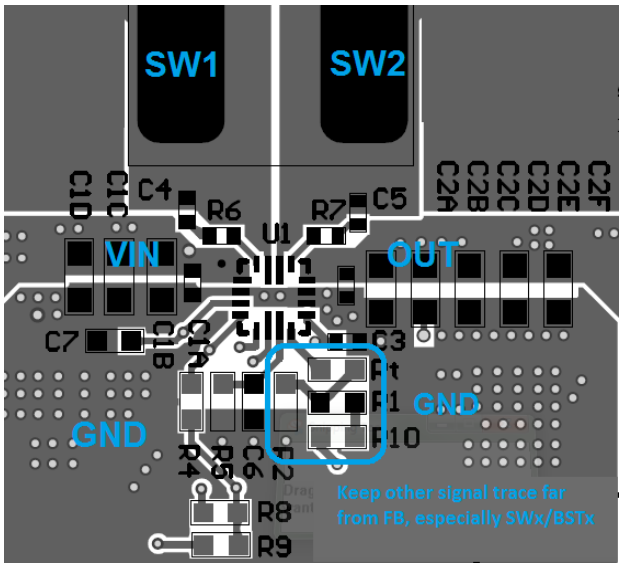
1. Place the ceramic C_{IN} and C_{OUT} close to the IC's VIN-to-GND and OUT-to-GND pins, respectively.
2. Use a large copper plane for PGND.
3. Add multiple vias to improve thermal dissipation.
4. Connect AGND to PGND.
5. Connect OUT using short, direct, and wide traces.
6. Add vias under the IC and route the OUT trace on both PCB layers (highly recommended).
7. Use a large copper plane for SW1 and SW2.
8. Place the VCC decoupling capacitor as close to the VCC pin as possible.
9. The FB trace requires special consideration. Use a GND copper to cover this trace.
10. Route other signal traces far away from FB, such as SWx and BSTx.

Note:

12) The recommended PCB layout is based on Figure 17 on page 30.



Top Layer



Close-Up of Layout

Figure 16: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

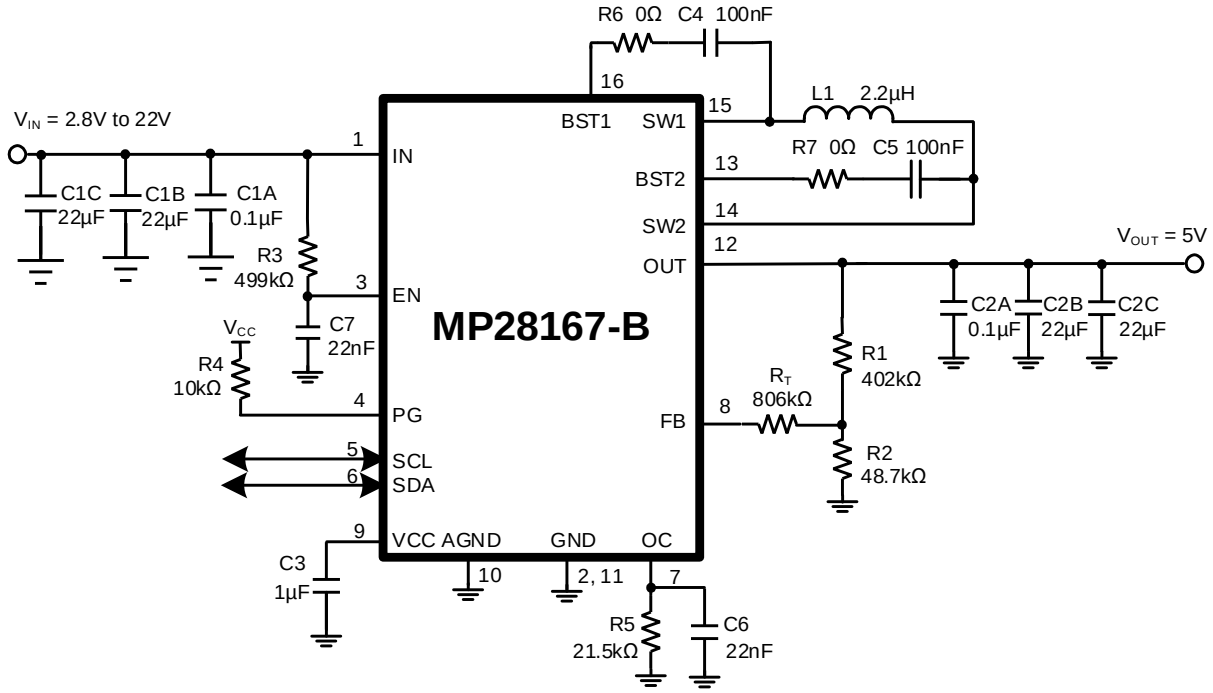


Figure 17: Typical Application Circuit (V_{OUT} = 5V)

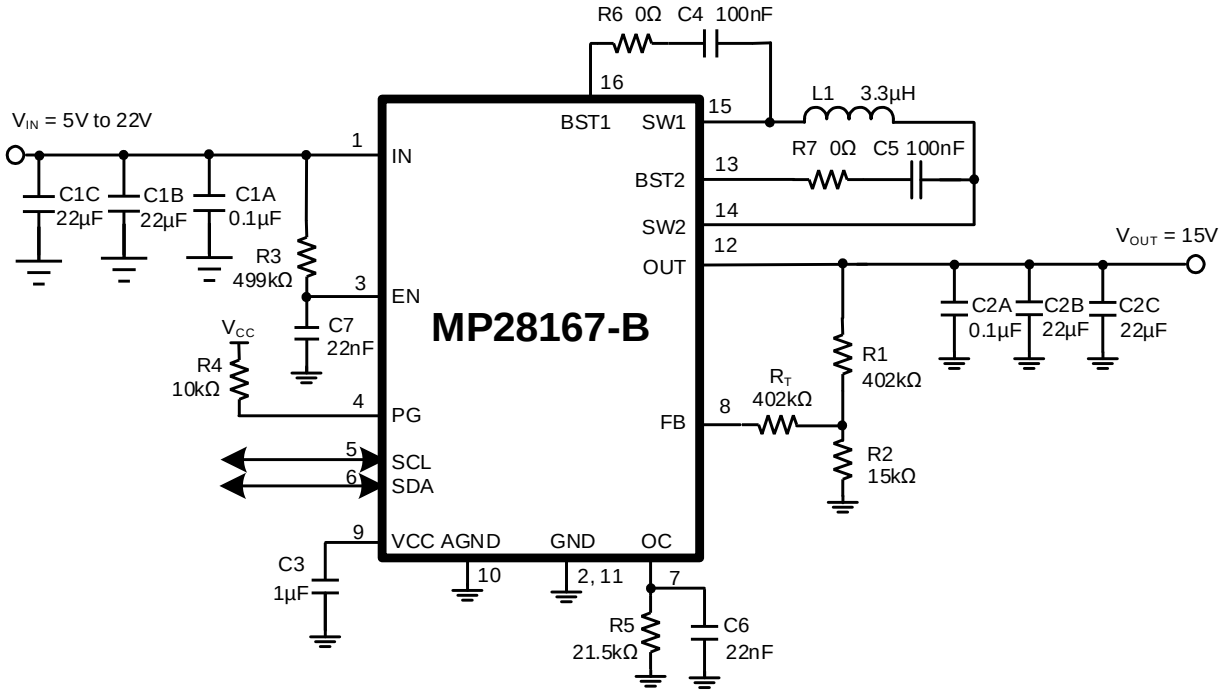
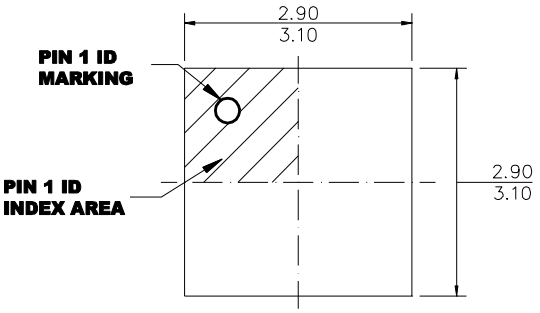


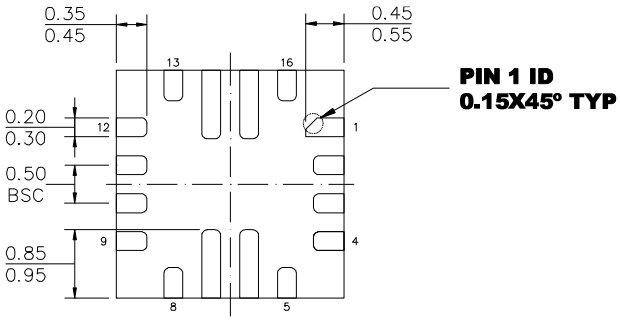
Figure 18: Typical Application Circuit (V_{OUT} = 15V)

PACKAGE INFORMATION

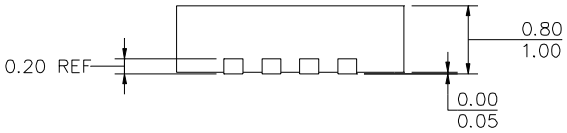
QFN-16 (3mmx3mm)



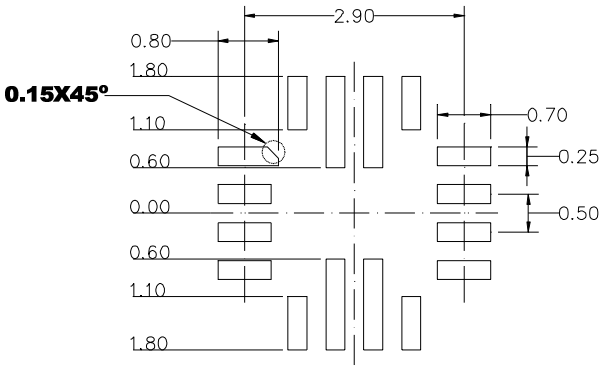
TOP VIEW



BOTTOM VIEW



SIDE VIEW

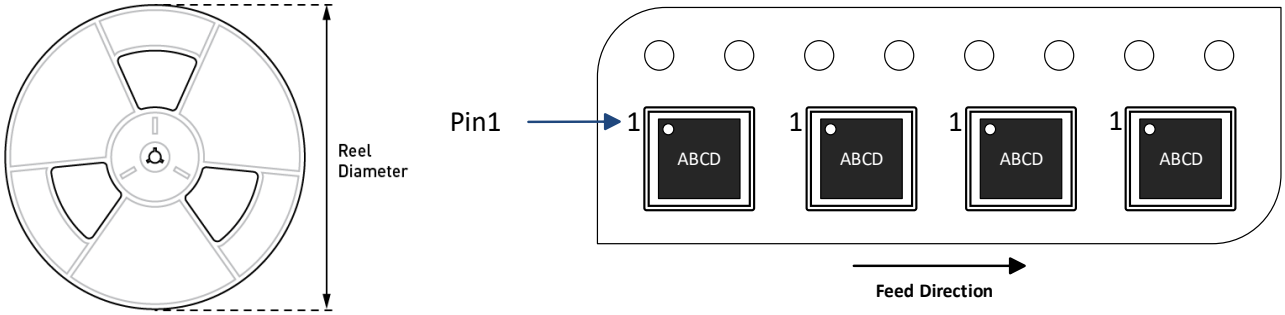


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP28167GQ-B-Z	QFN-16 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/8/2024	Initial Release	-