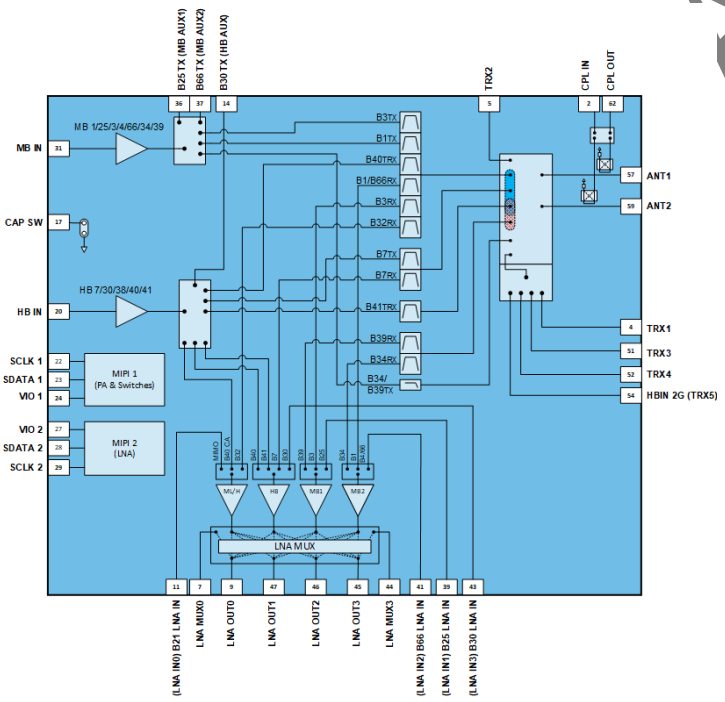
QM77048/B/D/E
Integrated MHB L-PAMiD

Product Overview

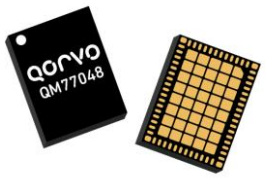
The Qorvo® QM77048 is a multi-mode, high efficiency Mid Band and High Band L-PAMiD (LNA plus Power Amplifier Module with integrated Duplexers) module designed for use as the integrated RF front-end in multi-mode NR / LTE / UMTS / CDMA mobile cellular equipment. The high efficiency L-PAMiD contains power amplifier paths and LNA bank for 3G/4G/5G Mid and High Band frequencies along with distribution switches, multiplex filters, and antenna switches for multi-band coverage of both transmit and receive functions. QM77048 band select, LNA gain and operating parameters are programmed through the Mobile Industry Processor Interface (MIPI) bus(es). The QM77048 transmit-receive module supports Average Power Tracking (APT) and Envelope Tracking (ET) for application versatility combined with higher system efficiency across a wide range of power levels.

The QM77048 is packaged in a RoHS-compliant, compact 62-pin, 6.5 x 8.6 x 0.8 (max) mm surface-mount leadless package.

Functional Block Diagram



Functional Block Diagram



62 Pin 6.5x8.6 mm leadless SMT Package

Key Features

- Integrated MB and HB LNAs
- Multi-Mode and Multi Band Capabilities
- NR, FDD-LTE/TDD-LTE, WCDMA, CDMA2000
- Integrated Band 1, 3, 4, 7[3], 32[1,2,3], 34, 39, 40 and 41(38) Filters for Transmit and Receive
- Additional Bands Through External AUX Paths
- MIPI RFFE Digital Control Interface
- Intra-Band Uplink and Downlink Carrier Aggregation (CA): B1, B3, B7, B39, B40, B41
- Inter-band Downlink Carrier Aggregation (DL CA) functionality: B39+B41, B34+B39, B1+B3+41, B1+B3+B40[3], B1+B3+B7[3]+B32[1,2,3]
- Designed and Optimized for Use with DC-DC Converter
- Support of Average Power Tracking (APT) and Envelope Tracking (ET) for High System Efficiency and Versatility
- Supports Power Class 2 (PC2) within B41.
- Supports 5NR bands n1, n3, n4, n7, n40, n41(38), n66.
- Programmable with MIPI RFFE V3.0 Interfaces

1 – Not included in QM77048B
2 – Not included in QM77048D
3 – Not included in QM77048E

Applications

- 2G/3G/4G/5G Multi-Mode Modems, Handsets, Data Cards or Wearable Devices
- High Performance Communication Systems

Ordering Information

PART NUMBER	DESCRIPTION
QM77048x TR7	7” Reel with 750 pieces
QM77048x TR13	13” Reel with 5000 pieces
QM77048x PCK	Evaluation board and 5 pc sample
QM77048x SB	Sample Bag with 5 pc sample
QM77048x DK	Design Kit includes EVB with module, RD2000 Communication Bd and harness.

Note: x = B, D,or E Version

Absolute Maximum Ratings

PARAMETER	CONDITIONS	Rating
Storage Temperature		−55 to +150 °C
Operating Temperature		−30 to +85 °C
Supply Voltage, VCC	Standby Mode	+6.0 V
	Idle Mode	+6.0 V
	Operating Mode	+5.5 V
Supply Voltage, VBATT		-1.2V to +6.0 V
Supply Voltage, VDD_LNA		+1.32V
Digital control signals (VIO, SLCK, SDATA)		+2 V
RF Input Power	CW, 50 Ω, T = 25˚C	+10 dBm
Output Load VSWR (Ruggedness) Ant and MB_HB Tx Aux Ports	Ruggedness is guaranteed with closed loop condition with fixed Forward Pout=Prated. VBATT = 4.8V, VCC = 4.8V. Temp = -30 to +85°C.	10:1

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of the Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Recommended Operating Conditions

PARAMETER	MIN.	TYP.	MAX.	UNITS
Operating Frequency Range	1452	-	2690	MHz
Operating Ambient Temperature	-20	+25	+85	°C
Supply Voltage, VBATT	+3.0	3.8	+4.8	V
Supply Voltage, APT, VCC1, VCC2	+0.5(1)	3.8	+4.8	V
Supply Voltage, ET, VCC1, VCC2	+1	-	+5.1	V
Supply Voltage, VDD_LNA	+1.15	+1.2	+1.3	V
Supply Voltage, VIO	+1.65	+1.8	+1.95	V
VIO Rise Time	-	-	400	µs
RF Input Power	-	-	+6	dBm
SCLK, SDATA Logic Low	0	-	0.3*VIO	V
SCLK, SDATA Logic HIGH	0.7*VIO	-	VIO	V
SCLK, SDATA Input, Current	-	-	50	µA
SCLK Write Speed	-	38.4	52	MHz
SCLK Read Speed	-	-	26	MHz
Total Leakage Current (ICC+IBAT)	-	-	20	µA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Notes:

1. VCC down to 0.5V may be used for backed-off power when using DC-DC converter to reduce low power current drain. Refer to Look-up Table (LUT) for recommended VCC settings for each output power level.

5G NR Waveforms

Waveform Name format is "NRccMmm" where: cc is Channel BW (MHz); mm is MPR *10 to avoid showing the decimal point.
NR Bands are tested with Highest Channel BW and Lowest SCS unless otherwise specified

5G Waveform	Duplex Mode	Channel BW	SCS	Modulation	RB allocation	RB Allocated	RB start	MPR
NR20M00	FDD	20	15	DFT-s-OFDM QPSK	Inner_Full	50	25	0
NR20M30	FDD	20	15	CP-OFDM QPSK	Outer_Full	106	0	3
NR20M65	FDD	20	15	CP-OFDM 256QAM	Outer_Full	106	0	6.5
NR30M00	FDD	30	15	DFT-s-OFDM QPSK	Inner_Full	80	40	0
NR30M30	FDD	30	15	CP-OFDM QPSK	Outer_Full	160	0	3
NR30M65	FDD	30	15	CP-OFDM 256QAM	Outer_Full	160	0	6.5
NR80M00	TDD	80	30	DFT-s-OFDM QPSK	Inner_Full	108	54	0
NR80M30	TDD	80	30	CP-OFDM QPSK	Outer_Full	217	0	3
NR80M65	TDD	80	30	CP-OFDM 256QAM	Outer_Full	217	0	6.5
NR100M00	TDD	100	30	DFT-s-OFDM QPSK	Inner_Full	135	67	0
NR100M30	TDD	100	30	CP-OFDM QPSK	Outer_Full	273	0	3
NR100M65	TDD	100	30	CP-OFDM 256QAM	Outer_Full	273	0	6.5

Band 1 4G LTE and 5G NR Common Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 1	1920		1980	MHz
Noise at LNA Out (LNA_Out0 ~ LNA_Out3, LNA on, G1)					
Non CA RX Band Noise	2110 – 2170MHz, 20MHz QPSK 100RB		-156		dBm/Hz
B3 RX Band Noise (1805 – 1880MHz)	Tx=1930MHz, 20MHz QPSK 25RB		-150		
	Tx=1950MHz, 20MHz QPSK 25RB		-154		
B40 Rx Band Noise, DL CA	2300 – 2400MHz, 20MHz QPSK 100RB		-155		
B41 Rx Band Noise, DL CA	2496 – 2690MHz, 20MHz QPSK 100RB		-156		
B7 Rx Band Noise, DL CA	2620 – 2690MHz, 20MHz QPSK 100RB		-156		
Co-existence Noise at ANT (ANT1 or ANT2)					
LB RX Band Noise	699 – 960MHz, 40MHz QPSK 200RB		-170		dBm/Hz
GPS Band Noise	1574 – 1577MHz, 40MHz QPSK 200RB		-164		
ISM 2.4G Noise	2402 – 2484MHz, 40MHz QPSK 200RB		-164		
n77 RX Band Noise	3300 – 4200MHz, 40MHz QPSK 200RB		-160		
ISM 5G Noise (except harmonics)	5150 – 5850MHz, 40MHz QPSK 200RB		-184		
Harmonics at ANT ports (10MHz QPSK 12RB)	2f0		-60		dBm
	3f0		-70		
	≥4f0		-55		
Stability, spurious output level	Output Load VSWR 6:1, all phases angles, Pout = Prated Closed Loop, CW Modulation, VCC=3.4V to 4.6V, Temp = -20°C to +85°C			-70	dBc

Band 1 5G NR Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

Parameter	Conditions		Min.	Typ.	Max.	Units
Operational Frequency Range	NR Band n1		1920		1980	MHz
Maximum Linear Output Power	HPM, VCC = 3.8V	NR20M00	25			dBm
Gain	HPM, VCC = 3.8V	NR20M00		29		dB
	HPM, VCC = 3.8V, VBAT=3.8V, Temp = -20°C to +85°C	NR20M00		27		
	LPM, VCC =1.3V, Pout=12dBm	NR20M00		27		
	LPM, VCC = 0.7V, Pout=2dBm	NR20M00		24		
PAE	HPM, VCC = 3.8V, Pout = Pmax	NR20M00		15		%
Current Consumption	HPM, VCC = 3.8V, Pout = Pmax	NR20M00		530		mA
	LPM, VCC = 0.7V, Pout = 2dBm	NR20M00		65		
NR ACLR	HPM, VCC = 3.8V, Pout ≤ Pmax	NR20M30		-42	-33	dBc
UTRA - ACLR1	HPM, VCC = 3.8V, Pout ≤ Pmax	NR20M30		-43	-36	
UTRA - ACLR2	HPM, VCC = 3.8V, Pout ≤ Pmax	NR20M30		-62	-39	
EVM	HPM, VCC = 3.8V, Pout ≤ Pmax	NR20M65		2		%

Band 1 4G LTE Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, QPSK, 10MHz, 12 Resource Blocks with MPR=0. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 1	1920		1980	MHz
Maximum Linear Output Power	ET, VCC ≤ 5.1V	26			dBm
	HPM, VCC = 3.8V	25			
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C	24			
Gain	HPM, VCC = 3.8V		29		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		27		
	LPM, VCC =1.3V, Pout=12dBm		27		
	LPM, VCC =0.70V, Pout=2dBm		24		
EUTRA - ACLR	HPM, VCC = 3.8V, Pout ≤ Pmax		-43	-33	dBc
UTRA - ACLR1	HPM, VCC = 3.8V, Pout ≤ Pmax			-36	
UTRA - ACLR2	HPM, VCC = 3.8V, Pout ≤ Pmax			-39	
EVM	All modulations		1.25		%
Gain transient time	Gain transient time between PA modes		--	10	µs
PAE	HPM, VCC = 3.8V, Pout = Pmax		15		%
Quiescent Current	HPM, VCC = 3.8V, No RF		150		mA
Current Consumption	HPM, VCC = 3.8V, Pout = Pmax		510		mA
	LPM, VCC = 0.70V, Pout=2dBm		65		

Band 1 3G WCDMA Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, R99. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 1	1920		1980	MHz
Maximum Output Power	HPM, VCC = 3.8V	26			dBm
	HPM, VCC = 3.8V, VBATT= 3.8V, Temp = -20°C to +85°C	25			
Gain	HPM, VCC = 3.8V		29		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		28		
UMTS ACLR1 (±5MHz)	Pout ≤ Pmax		-45	-36	dBc
UMTS ACLR2 (±10MHz)	Pout ≤ Pmax		-58	-46	
EVM	All Condition		1.0		%
PAE	HPM, Pout = Pmax		16		%
Current Consumption	HPM, Pout = Pmax		730		mA
Phase discontinuity variation			--	10	Degree
Noise at LNA Out (LNA_Out0 ~ LNA_Out3, LNA on, G1)					
RX Band Noise	Pout ≤ Pmax		-166		dBm/Hz
Co-existence Noise at ANT (ANT1 or ANT2)					
ISM 2.4G Noise	2400 to 2483 MHz		-187		dBm/Hz
ISM 5G Noise (except harmonics)	5150 to 5850 MHz		-187		
GPS Band Noise	1574 to 1577 MHz		-181		
Harmonics at ANT ports	2f0		-68		dBm
	3f0		-60		

Band 1/4/66 Rx Characteristics

Test conditions unless otherwise stated: VDD_LNA=1.2V, Temp = 25°C, VBATT = 3.8V, PA disabled, Gain state G1. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 1	2110		2170	MHz
	Band 4	2110		2155	
	Band 66 (70 MHz)	2110		2180	
RF Gain	Gain state 0 (G0)		15.8		dB
	Gain state 1 (G1)		15		
	Gain state 2 (G2)		12.7		
	Gain state 3 (G3)		9.8		
	Gain state 4 (G4)		7.1		
	Gain state 5 (G5)		3.1		
	Gain state 6 (G6)		0		
	Gain state 7 (G7)		-7.6		
	Gain state 8 (G8)		TBD 11		
	Gain state 9 (G9)		-9		
	Gain state 10 (G10)		-14.7		
Drain Current	Gain state 0 (G0)		9		mA
	Gain state 1 (G1)		8		
	Gain state 2 (G2)		7		
	Gain state 3 (G3)		6		
	Gain state 4 (G4)		5.4		
	Gain state 5 (G5)		5.4		
	Gain state 6 (G6)		5		
	Gain state 7 (G7)		3.3		
	Gain state 8 (G8)		TBD 1.5		
	Gain state 9 (G9)		0.1		
	Gain state 10 (G10)		0.1		
Noise Figure	Gain state 0 (G0)		4		dB
	Gain state 1 (G1)		4		
	Gain state 2 (G2)		4.5		
	Gain state 3 (G3)		5		
	Gain state 4 (G4)		5.5		
	Gain state 5 (G5)		6		
	Gain state 6 (G6)		9.5		
	Gain state 7 (G7)		14		
	Gain state 8 (G8)		TBD		
	Gain state 9 (G9)		10		
	Gain state 10 (G10)		15		
Input Return Loss	Rx On, Gain state 1 (G1)		12		dB
Output Return Loss	Rx On, Gain state 1 (G1)		5		
Tx Leakage Power	Gain state 1 (G1), PA enabled, Tx Pout ≤ Pmax, 5MHz QPSK 25RB		-17		dBm/5MHz
Reverse Isolation	Rx out to ANT, Active Gain state only		32		dB
Timing, LPM to Active	Gain settling within 0.2dB of final		3.6		µs

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Timing, LNA Enable	value when LNA is turned on (after Bus Park)		3.5		
Timing, Gain State Change	Switching between any two gain modes		0.5		

Band 3/4/66 4G LTE and 5G NR Common Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 3	1710		1785	MHz
	Band 4	1710		1755	
	Band 66	1710		1780	
Noise at LNA Out (LNA_Out0 ~ LNA_Out3, LNA on, G1)					
RX Band Noise	1805 – 1880MHz, 20MHz QPSK 50RB		-157		dBm/Hz
B1 RX Band Noise (2110 – 2170MHz)	Tx=1920MHz, 20MHz QPSK 50RB		-161		
B40 Rx Band Noise, DL CA	2300 – 2400MHz, 20MHz QPSK 100RB		-153		
B41 Rx Band Noise, DL CA	2496 – 2690MHz, 20MHz QPSK 100RB		-156		
B7 Rx Band Noise, DL CA	2620 – 2690MHz, 20MHz QPSK 100RB		-165		
Co-existence Noise at ANT (ANT1 or ANT2)					
LB RX Band Noise	699 – 960MHz, 40MHz QPSK 200RB		-170		dBm/Hz
GPS Band Noise	1574 – 1577MHz, 40MHz QPSK 200RB		-154		
ISM 2.4G Noise	2402 – 2484MHz, 40MHz QPSK 200RB		-169		
n77 RX Band Noise	3300 – 4200MHz, 40MHz QPSK 200RB		-157		
ISM 5G Noise (except harmonics)	5150 – 5850MHz, 40MHz QPSK 200RB		-187		
Harmonics at ANT ports (10MHz QPSK 12RB)	2f0		-62		dBm
	3f0		-72		
	≥4f0		-40		
Stability, spurious output level	Output Load VSWR 6:1, all phases angles, Pout = Prated Closed Loop, CW Modulation, VCC=3.4V to 4.6V, Temp = -30°C to +85°C			-70	dBc

Band 3/4/66 5G NR Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

Parameter	Conditions		Min.	Typ.	Max.	Units
Operational Frequency Range	NR Band n3		1710		1785	MHz
	NR Band n4		1710		1755	
	NR Band n66		1710		1780	
Maximum Linear Output Power	HPM, VCC = 3.8V,	NR30M00	25			dBm
Gain	HPM, VCC = 3.8V	NR30M00		29		dB
	HPM, VCC = 3.8V, VBAT=3.8V, Temp = -20°C to +85°C	NR30M00		28		
	LPM, VCC = 1.3V, Pout=12dBm	NR30M00		26		
	LPM, VCC = 0.7V, Pout=2dBm	NR30M00		23		
PAE	HPM, VCC = 3.8V, Pout = Pmax	NR30M00		16		%
Current Consumption	HPM, VCC = 3.8V, Pout = Pmax	NR30M00		525		mA
	LPM, VCC = 0.7V, Pout=2dBm	NR30M00		65		
NR ACLR	n3, HPM, VCC = 3.8V, Pout ≤ Pmax	NR30M30		-38	-33	dBc
UTRA - ACLR1	n3, HPM, VCC = 3.8V, Pout ≤ Pmax	NR30M30		-40	-36	
UTRA - ACLR2	n3, HPM, VCC = 3.8V, Pout ≤ Pmax	NR30M30		-50	-39	
EVM	n3, HPM, VCC = 3.8V, Pout ≤ Pmax	NR30M65		1.6		%
EUTRA ACLR	n4, n66, HPM, VCC = 3.8V, Pout ≤ Pmax	NR20M30		-38	-33	dBc
EVM	n4, n66, HPM, VCC = 3.8V, Pout ≤ Pmax	NR20M65		2.1		%

Band 3/4/66 4G LTE Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, QPSK, 10MHz, 12 Resource Blocks with MPR=0. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 3	1710		1785	MHz
	Band 4	1710		1755	
	Band 66	1710		1780	
Maximum Linear Output Power	ET, VCC ≤ 5.1V	26			dBm
	HPM, VCC = 3.8V	25			
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C	24			
Gain	HPM, VCC = 3.8V		28.5		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		27.5		
	LPM, VCC =1.3V, Pout=12dBm		26		
	LPM, VCC = 0.7V, Pout=2dBm		22		
EUTRA - ACLR	HPM, VCC = 3.8V, Pout ≤ Pmax		-48	-33	dBc
UTRA - ACLR1	HPM, VCC = 3.8V, Pout ≤ Pmax		-50	-36	
UTRA - ACLR2	HPM, VCC = 3.8V, Pout ≤ Pmax		-58	-39	
EVM	All modulations		1.5		%
Gain transient time	Gain transient time between PA modes		--	10	µs
PAE	HPM, VCC = 3.8V, Pout = Pmax		16		%
Quiescent Current	HPM, VCC = 3.8V, No RF		150		mA
Current Consumption	HPM, VCC = 3.8V, Pout = Pmax		515		mA
	LPM, VCC = 0.7V, Pout=2dBm		55		

Band 3 Rx Characteristics

Test conditions unless otherwise stated: VDD_LNA=1.2V, Temp = 25°C, VBATT = 3.8V, PA disabled, Gain state G1. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 3	1805		1880	MHz
RF Gain	Gain state 0 (G0)		17		dB
	Gain state 1 (G1)		15		
	Gain state 2 (G2)		12		
	Gain state 3 (G3)		9.5		
	Gain state 4 (G4)		6		
	Gain state 5 (G5)		2.7		
	Gain state 6 (G6)		0		
	Gain state 7 (G7)		-4.3		
	Gain state 8 (G8)		TBD 14		
	Gain state 9 (G9)		-8.5		
	Gain state 10 (G10)		-13.8		
Drain Current	Gain state 0 (G0)		9		mA
	Gain state 1 (G1)		8		
	Gain state 2 (G2)		7		
	Gain state 3 (G3)		6		
	Gain state 4 (G4)		5.4		
	Gain state 5 (G5)		5.4		
	Gain state 6 (G6)		5		
	Gain state 7 (G7)		3.3		
	Gain state 8 (G8)		TBD 1.5		
	Gain state 9 (G9)		0.1		
	Gain state 10 (G10)		0.1		
Noise Figure	Gain state 0 (G0)		3.5		dB
	Gain state 1 (G1)		3.5		
	Gain state 2 (G2)		3.7		
	Gain state 3 (G3)		4		
	Gain state 4 (G4)		4.6		
	Gain state 5 (G5)		5.2		
	Gain state 6 (G6)		8.4		
	Gain state 7 (G7)		10		
	Gain state 8 (G8)		TBD 3.9		
	Gain state 9 (G9)		8		
	Gain state 10 (G10)		13.5		
Input Return Loss	Rx On, Gain state 1 (G1)		16		dB
Output Return Loss	Rx On, Gain state 1 (G1)		7		
Tx Leakage Power	Gain state 1 (G1), PA enabled, Tx Pout ≤ Pmax, 5MHz QPSK 25RB		TBD -11		dBm/5MHz
Reverse Isolation	Rx out to ANT, Active Gain state only		30		dB
Timing, LPM to Active	Gain settling within 0.2dB of final value when LNA is turned on (after Bus Park)		1.7		µs
Timing, LNA Enable			1.6		
Timing, Gain State Change	Switching between any two gain modes		0.5		

Band 32 Rx Characteristics (Not available in B/D/E part numbers)

Test conditions unless otherwise stated: VDD_LNA=1.2V, Temp = 25°C, VBATT = 3.8V, PA disabled, Gain state G1. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 32	1452		1496	MHz
RF Gain	Gain state 0 (G0)		15.8		dB
	Gain state 1 (G1)		15.6		
	Gain state 2 (G2)		12.5		
	Gain state 3 (G3)		9.8		
	Gain state 4 (G4)		6.5		
	Gain state 5 (G5)		3.2		
	Gain state 6 (G6)		-3.5		
	Gain state 7 (G7)		-8.3		
	Gain state 8 (G8)		TBE 9.4		
	Gain state 9 (G9)		-10.7		
	Gain state 10 (G10)		-17.2		
Drain Current	Gain state 0 (G0)		9		mA
	Gain state 1 (G1)		8		
	Gain state 2 (G2)		7		
	Gain state 3 (G3)		6		
	Gain state 4 (G4)		5.4		
	Gain state 5 (G5)		5.4		
	Gain state 6 (G6)		5		
	Gain state 7 (G7)		3.3		
	Gain state 8 (G8)		TBD 1.5		
	Gain state 9 (G9)		0.1		
	Gain state 10 (G10)		0.1		
Noise Figure	Gain state 0 (G0)		4.4		dB
	Gain state 1 (G1)		4.4		
	Gain state 2 (G2)		4.6		
	Gain state 3 (G3)		4.9		
	Gain state 4 (G4)		5.3		
	Gain state 5 (G5)		6.1		
	Gain state 6 (G6)		11		
	Gain state 7 (G7)		13.5		
	Gain state 8 (G8)		TBD 3.6		
	Gain state 9 (G9)		10.8		
	Gain state 10 (G10)		17.4		
Input Return Loss	Rx On, Gain state 1 (G1)		9		dB
Output Return Loss	Rx On, Gain state 1 (G1)		16		
Reverse Isolation	Rx out to ANT, Active Gain state only		40		dB
Timing, LPM to Active	Gain settling within 0.2dB of final value when LNA is turned on (after Bus Park)		2.7		µs
Timing, LNA Enable			2.6		
Timing, Gain State Change	Switching between any two gain modes		0.7		

Band 34 4G LTE Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, QPSK, 10MHz, 12 Resource Blocks with MPR=0. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 34	2010		2025	MHz
Maximum Linear Output Power	ET, VCC ≤ 5.1V	26			dBm
	HPM, VCC = 3.8V	25			
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C	24			
Gain	HPM, VCC = 3.8V		28.5		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		29		
	LPM, VCC =1.3V, Pout=12dBm		27		
	LPM, VCC =0.7V, Pout=2dBm		24		
EUTRA - ACLR	HPM, VCC = 3.8V, Pout ≤ Pmax		-43	-33	dBc
UTRA - ACLR1	HPM, VCC = 3.8V, Pout ≤ Pmax		-45	-36	
UTRA - ACLR2	HPM, VCC = 3.8V, Pout ≤ Pmax		-60	-39	
EVM	All modulations		1.2		%
Gain transient time	Gain transient time between PA modes		--	10	µs
PAE	HPM, VCC = 3.8V, Pout = Pmax		17		%
Quiescent Current	HPM, VCC = 3.8V, No RF		150		mA
Current Consumption	HPM, VCC = 3.8V, Pout = Pmax		470		mA
	LPM, VCC = 0.7V, Pout=2dBm		60		
LB RX Band Noise at ANT ports	699 – 960MHz, 15MHz QPSK 75RB		-145		dBm/Hz
GPS Band Noise at ANT ports	1574 – 1577MHz, 15MHz QPSK 75RB		-135		
ISM 2.4G Noise at ANT ports	2402 – 2484MHz, 15MHz QPSK 75RB		-155		
n77 RX Band Noise at ANT ports	3300 – 4200MHz, 15MHz QPSK 75RB		-187		
ISM 5G Noise at ANT ports	5150 – 5850MHz, 15MHz QPSK 75RB		-186		
Harmonics	2f0		-51		dBm
	3f0		-41		
	4f0		-33		
	≥5f0		-	-40	
Stability, spurious output level	Output Load VSWR 6:1, all phases angles, Pout = Prated Closed Loop, CW Modulation, VCC=3.4V to 4.6V, Temp = -30°C to +85°C			-70	dBc

Band 34 3G TDS-CDMA Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, TDS-CDMA modulation. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 34	2010		2025	MHz
Maximum Output Power	HPM, VCC = 3.8V	26			dBm
	HPM, VCC = 3.8V, VBATT = 3.8V, Temp = -20°C to +85°C	25			
Gain	HPM, VCC = 3.8V		30		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		29		
UMTS ACLR1 (±1.6MHz)	Pout ≤ Pmax		-50	-36	dBc
UMTS ACLR2 (±3.2MHz)	Pout ≤ Pmax		-67	-46	
EVM	All Condition		1		%
PAE	HPM, Pout = Pmax		19		%
Current Consumption	HPM, Pout = Pmax		625		mA
RX Band Noise at ANT ports	925 – 935MHz		-95		dBm/100kHz
	935 – 960MHz		-95		
	1805 – 1880MHz		-81		
ISM 2.4G Noise at ANT ports	2400 to 2483 MHz		-153		dBm/Hz
ISM 5G Noise at ANT ports	5150 to 5850 MHz		-188		
GPS Band Noise at ANT ports	1574 to 1577 MHz		-134		
Harmonics	2f0		-70		dBm
	3f0		-77		

Band 34 Rx Characteristics

Test conditions unless otherwise stated: VDD_LNA=1.2V, Temp = 25°C, VBATT = 3.8V, PA disabled, Gain state G1. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 34	2010		2025	MHz
RF Gain	Gain state 0 (G0)		15.3		dB
	Gain state 1 (G1)		14.6		
	Gain state 2 (G2)		11.6		
	Gain state 3 (G3)		8.3		
	Gain state 4 (G4)		5.4		
	Gain state 5 (G5)		1.4		
	Gain state 6 (G6)		-1.3		
	Gain state 7 (G7)		-8.2		
	Gain state 8 (G8)		TBD 8.6		
	Gain state 9 (G9)		-8.7		
	Gain state 10 (G10)		-14.6		
Drain Current	Gain state 0 (G0)		9		mA
	Gain state 1 (G1)		8		
	Gain state 2 (G2)		7		
	Gain state 3 (G3)		6		
	Gain state 4 (G4)		5.4		
	Gain state 5 (G5)		5.4		
	Gain state 6 (G6)		5		
	Gain state 7 (G7)		3.3		
	Gain state 8 (G8)		TBD 1.5		
	Gain state 9 (G9)		0.1		
	Gain state 10 (G10)		0.1		
Noise Figure	Gain state 0 (G0)		4.3		dB
	Gain state 1 (G1)		4.3		
	Gain state 2 (G2)		4.6		
	Gain state 3 (G3)		4.9		
	Gain state 4 (G4)		5.4		
	Gain state 5 (G5)		6.6		
	Gain state 6 (G6)		9.5		
	Gain state 7 (G7)		13.1		
	Gain state 8 (G8)		TBD 4.7		
	Gain state 9 (G9)		8.5		
	Gain state 10 (G10)		14.4		
Input Return Loss	Rx On, Gain state 1 (G1)		11		dB
Output Return Loss	Rx On, Gain state 1 (G1)		11		
Reverse Isolation	Rx out to ANT, Active Gain state only		28		dB
Timing, LPM to Active	Gain settling within 0.2dB of final value when LNA is turned on (after Bus Park)		2.5		µs
Timing, LNA Enable			2.4		
Timing, Gain State Change	Switching between any two gain modes		1.6		

Band 39 4G LTE Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, QPSK, 10MHz, 12 Resource Blocks with MPR=0. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 39	1880		1920	MHz
Maximum Linear Output Power	ET, VCC ≤ 5.1V	26			dBm
	HPM, VCC = 3.8V	25			
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C	24			
Gain	HPM, VCC = 3.8V		29.5		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		30		
	LPM, VCC =1.3V, Pout=12dBm		28		
	LPM, VCC =0.7V, Pout=2dBm		25		
EUTRA - ACLR	HPM, VCC = 3.8V, Pout ≤ Pmax		-48	-33	dBc
UTRA - ACLR1	HPM, VCC = 3.8V, Pout ≤ Pmax		-50	-36	
UTRA - ACLR2	HPM, VCC = 3.8V, Pout ≤ Pmax		-57	-39	
EVM	All modulations		1.5		%
Gain transient time	Gain transient time between PA modes		--	10	µs
PAE	HPM, VCC = 3.8V, Pout = Pmax		17		%
Quiescent Current	HPM, VCC = 3.8V, No RF		150		mA
Current Consumption	HPM, VCC = 3.8V, Pout = Pmax		450		mA
	LPM, VCC = 0.7V, Pout=2dBm		90		
LB RX Band Noise at ANT ports	699 – 960MHz, 20MHz QPSK 100RB		-146		dBm/Hz
GPS Band Noise at ANT ports	1574 – 1577MHz, 20MHz QPSK 100RB		-130		
ISM 2.4G Noise at ANT ports	2402 – 2484MHz, 20MHz QPSK 100RB		-156		
n77 RX Band Noise at ANT ports	3300 – 4200MHz, 20MHz QPSK 100RB		-169		
ISM 5G Noise at ANT ports (except harmonics)	5150 – 5850MHz, 20MHz QPSK 100RB		-186		
Harmonics	2f0		-50		dBm
	3f0		-48		
	4f0		-40		
	≥5f0		-	-40	
Stability, spurious output level	Output Load VSWR 6:1, all phases angles, Pout = Prated Closed Loop, CW Modulation, VCC=3.4V to 4.6V, Temp = -30°C to +85°C			-70	dBc

Band 39 3G TDS-CDMA Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, TDS-CDMA modulation. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 39	1880		1920	MHz
Maximum Output Power	HPM, VCC = 3.8V	26			dBm
	HPM, VCC = 3.8V, VBATT = 3.8V, Temp = -20°C to +85°C	25			
Gain	HPM, VCC = 3.8V		31.5		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		30.5		
UMTS ACLR1 (±1.6MHz)	Pout ≤ Pmax		-51	-36	dBc
UMTS ACLR2 (±3.2MHz)	Pout ≤ Pmax		-66	-46	
EVM	All Condition		1.0		%
PAE	HPM, Pout = Pmax		19		%
Current Consumption	HPM, Pout = Pmax		635		mA
RX Band Noise at ANT ports	925 – 935MHz		-95		dBm/100kHz
	935 – 960MHz		-96		
	1805 – 1880MHz		-64		
ISM 2.4G Noise at ANT ports	2400 to 2483 MHz		-155		dBm/Hz
ISM 5G Noise (except harmonics) at ANT ports	5150 to 5850 MHz		-187		
GPS Band Noise at ANT ports	1574 to 1577 MHz		-128		
Harmonics	2f0		-50		dBm
	3f0		-48		

Band 39 Rx Characteristics

Test conditions unless otherwise stated: VDD_LNA=1.2V, Temp = 25°C, VBATT = 3.8V, PA disabled, Gain state G1. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 39	1880		1920	MHz
RF Gain	Gain state 0 (G0)		16.9		dB
	Gain state 1 (G1)		15.5		
	Gain state 2 (G2)		12.4		
	Gain state 3 (G3)		9.5		
	Gain state 4 (G4)		6		
	Gain state 5 (G5)		2.8		
	Gain state 6 (G6)		-0.5		
	Gain state 7 (G7)		-4.1		
	Gain state 8 (G8)		TBD 14		
	Gain state 9 (G9)		-9		
	Gain state 10 (G10)		-14		
Drain Current	Gain state 0 (G0)		9		mA
	Gain state 1 (G1)		8		
	Gain state 2 (G2)		7		
	Gain state 3 (G3)		6		
	Gain state 4 (G4)		5.4		
	Gain state 5 (G5)		5.4		
	Gain state 6 (G6)		5		
	Gain state 7 (G7)		3.3		
	Gain state 8 (G8)		TBD 1.5		
	Gain state 9 (G9)		0.1		
	Gain state 10 (G10)		0.1		
Noise Figure	Gain state 0 (G0)		3.6		dB
	Gain state 1 (G1)		3.6		
	Gain state 2 (G2)		3.7		
	Gain state 3 (G3)		4.2		
	Gain state 4 (G4)		4.6		
	Gain state 5 (G5)		5.3		
	Gain state 6 (G6)		8.4		
	Gain state 7 (G7)		10		
	Gain state 8 (G8)		TBD 3.9		
	Gain state 9 (G9)		8.8		
	Gain state 10 (G10)		13.9		
Input Return Loss	Rx On, Gain state 1 (G1)		15		dB
Output Return Loss	Rx On, Gain state 1 (G1)		15		
Reverse Isolation	Rx out to ANT, Active Gain state only		28		dB
Timing, LPM to Active	Gain settling within 0.2dB of final value when LNA is turned on (after Bus Park)		1.5		µs
Timing, LNA Enable			1.4		
Timing, Gain State Change	Switching between any two gain modes		1.0		

MB_AUX 4G LTE and 5G NR Common Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location, including both B25_TX (MB_AUX1) and B66_TX (MB_AUX2).

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Mid Band	1710		2025	MHz
Co-existence Noise at ANT (ANT1 or ANT2)					
LB RX Band Noise	699 – 960MHz, 20MHz QPSK 100RB		-150		dBm/Hz
B2 Rx In Band Noise	1930 – 1990MHz, 20MHz, QPSK 100RB		-127		
HB RX Band Noise	2300 – 2700MHz, 20MHz QPSK 100RB		-153		
ISM 5G Noise (except harmonics)	5150 – 5850MHz, 20MHz QPSK 100RB		-160		
GPS Band Noise	1574 – 1577MHz, 20MHz QPSK 100RB		-137		
Harmonics at ANT ports (10MHz QPSK 12RB)	2f0		-10		dBm
	3f0		-18		
	≥4f0		-22		
Stability, spurious output level	Output Load VSWR 6:1, all phases angles, Pout = Prated Closed Loop, CW Modulation, VCC=3.8V to 4.6V, Temp = -30°C to +85°C			-70	dBc

MB_AUX 5G NR Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location, including both B25_TX (MB_AUX1) and B66_TX (MB_AUX2).

Parameter	Conditions		Min.	Typ.	Max.	Units
Operational Frequency Range	NR Band n2		1850	-	1910	MHz
	NR Band n25		1850	-	1915	
Maximum Linear Output Power	HPM, VCC = 3.8V	NR20M00	28.5			dBm
Gain	HPM, VCC = 3.8V	NR20M00		31.5		dB
	HPM, VCC = 3.8V, VBAT=3.8V, Temp = -20°C to +85°C	NR20M00		29.5		
	LPM, VCC =1.3V, Pout=12dBm	NR20M00		30		
	LPM, VCC =0.7V, Pout=2dBm	NR20M00		26		
PAE	HPM, VCC = 3.8V, Pout = Pmax	NR20M00		32		%
Current Consumption	HPM, VCC = 3.8V, Pout = Pmax	NR20M00		575		mA
	LPM, VCC = 0.7V, Pout=2dBm	NR20M00		85		
NR ACLR	HPM, VCC = 3.8V, Pout ≤ Pmax	NR20M30		-41	-33	dBc
UTRA - ACLR1	HPM, VCC = 3.8V, Pout ≤ Pmax	NR20M30		-42	-36	
UTRA - ACLR2	HPM, VCC = 3.8V, Pout ≤ Pmax	NR20M30		-54	-39	
EVM	HPM, VCC = 3.8V, Pout ≤ Pmax	NR20M65		1.0		%

MB_AUX 4G LTE Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, QPSK, 10MHz, 12 Resource Blocks with MPR=0. Performance referenced to module pin location, including both B25_TX (MB_AUX1) and B66_TX (MB_AUX2).

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 3	1710	-	1785	MHz
	Band 4	1710	-	1755	
	Band 66	1710	-	1780	
	Band 2	1850	-	1910	
	Band 25	1850	-	1915	
Maximum Linear Output Power	ET, VCC ≤ 5.1V	29.5			dBm
	HPM, VCC = 3.8V	28.5			
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C	27.5			
Gain	HPM, VCC = 3.8V		31		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		30.5		
	LPM, VCC =1.3V, Pout=15dBm		29		
	LPM, VCC =0.7V, Pout=5dBm		26		
EUTRA - ACLR	HPM, VCC = 3.8V, Pout ≤ Pmax		-41	-33	dBc
UTRA - ACLR1	HPM, VCC = 3.8V, Pout ≤ Pmax		-42	-36	
UTRA - ACLR2	HPM, VCC = 3.8V, Pout ≤ Pmax		-54	-39	
EVM	All modulations		1.2		%
Gain transient time	Gain transient time between PA modes		-	10	µs
PAE	HPM, VCC = 3.8V, Pout = Pmax		32		%
Quiescent Current	HPM, VCC = 3.8V, No RF		150		mA
Current Consumption	HPM, VCC = 3.8V, Pout = Pmax		570		mA
	LPM, VCC = 0.7V, Pout = 5dBm		60		

MB_AUX 3G WCDMA Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, R99. Performance referenced to module pin location, including both B25_TX (MB_AUX1) and B66_TX (MB_AUX2).

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 2	1850		1910	MHz
Maximum Output Power	HPM, VCC = 3.8V	29.5			dBm
	HPM, VCC = 3.8V, VBATT = 3.8V, Temp = -20°C to +85°C	28.5			
Gain	HPM, VCC = 3.8V		31.5		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		30.5		
UMTS ACLR1 (±5MHz)	Pout ≤ Pmax		-46	-36	dBc
UMTS ACLR2 (±10MHz)	Pout ≤ Pmax		-57	-46	
EVM	All Condition		1		%
PAE	HPM, Pout = Pmax		31		%
Current Consumption	HPM, Pout = Pmax		760		mA
Phase discontinuity variation		-15		15	Degree
ISM 2.4G Noise	2400 to 2483 MHz		-144		dBm/Hz
ISM 5G Noise (except harmonics)	5150 to 5850 MHz		-140		
GPS Band Noise	1574 to 1577 MHz		-140		
Harmonics	2f0		-14		dBm
	3f0		-27		

MB_AUX 3G CDMA2000 Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, 1xRTT C2k. Performance referenced to module pin location, including both B25_TX (MB_AUX1) and B66_TX (MB_AUX2).

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band Class 1	1850		1910	MHz
Maximum Output Power	HPM, VCC = 3.8V	29.5			dBm
	HPM, VCC = 3.8V, VBATT = 3.8V, Temp = -20°C to +85°C	28.5			
Gain	HPM, VCC = 3.8V		32.5		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		31.5		
CDMA ACLR1 (±1.25MHz)	Pout ≤ Pmax		-60	-45	dBc
CDMA ACLR2 (±1.98MHz)	Pout ≤ Pmax		-72	-53	
EVM	All Condition		2		%
PAE	HPM, Pout = Pmax		31		%
Current Consumption	HPM, Pout = Pmax		755		mA
Phase discontinuity variation		-15		15	Degree
ISM 2.4G Noise	2400 to 2483 MHz		-144		dBm/Hz
ISM 5G Noise (except harmonics)	5150 to 5850 MHz		-145		
GPS Band Noise	1574 to 1577 MHz		-139		
Harmonics	2f0		-9		dBm
	3f0		-20		

Band 7 4G LTE and 5G NR Common Tx Characteristics (Not available in E part number)

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 7	2500		2570	MHz
Noise at LNA Out (LNA_Out0 ~ LNA_Out3, LNA on, G1)					
RX Band Noise	2620 – 2690MHz, 20MHz QPSK 75RB		-153		dBm/Hz
B1 Rx Band Noise, DL CA	2110 – 2170MHz, 20MHz QPSK 75RB		-159		
B3 Rx Band Noise, DL CA	1805 – 1880MHz, 20MHz QPSK 75RB		-156		
B32 Rx Band Noise, DL CA	1452 – 1496MHz, 20MHz QPSK 75RB		-152		
Co-existence Noise at ANT (ANT1 or ANT2)					
LB RX Band Noise	699 – 960MHz, 40MHz QPSK 200RB		-188		dBm/Hz
GPS Band Noise	1574 – 1577MHz, 40MHz QPSK 200RB		-189		
ISM 2.4G Noise	2402 – 2422MHz, 40MHz QPSK 200RB		-168		
	2427 – 2447MHz, 40MHz QPSK 200RB		-168		
	2452 – 2477MHz, 40MHz QPSK 200RB		-141		
	2462 – 2482MHz, 40MHz QPSK 200RB		-136		
n77 RX Band Noise	3300 – 4200MHz, 20MHz QPSK 100RB		-166		
n79 RX Band Noise	4400 – 5000MHz, 20MHz QPSK 100RB		-164		
ISM 5G Noise (except harmonics)	5150 – 5850MHz, 40MHz QPSK 200RB		-187		
Harmonics at ANT ports (10MHz QPSK 12RB)	2f0		-56		dBm
	3f0		-53		
	≥4f0		-47		
Stability, spurious output level	Output Load VSWR 6:1, all phases angles, Pout = Prated Closed Loop, CW Modulation, VCC=3.4V to 4.6V, Temp = -30°C to +85°C			-70	dBc

Band 7 5G NR Tx Characteristics (Not available in E part number)

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

Parameter	Conditions		Min.	Typ.	Max.	Units
Operational Frequency Range	NR Band n7		2500		2570	MHz
Maximum Linear Output Power	HPM, VCC = 4.2V,	NR20M00	25			dBm
Gain	HPM, VCC = 4.2V	NR20M00		28.5		dB
	HPM, VCC = 4.2V, VBAT=3.8V, Temp = -20°C to +85°C	NR20M00		28		
	LPM, VCC =1.2V, Pout=10.5dBm	NR20M00		26		
	LPM, VCC =0.7V, Pout=2dBm	NR20M00		19		
PAE	HPM, VCC = 4.2V, Pout = Pmax	NR20M00		11		%
Current Consumption	HPM, VCC = 4.2V, Pout = Pmax	NR20M00		725		mA
	LPM, VCC ≤ 0.7V, Pout=2dBm	NR20M00		65		
EUTRA ACLR	HPM, VCC = 4.2V, Pout ≤ Pmax	NR20M30		-37	-33	dBc
UTRA - ACLR1	HPM, VCC = 4.2V, Pout ≤ Pmax	NR20M30		-38	-36	
UTRA - ACLR2	HPM, VCC = 4.2V, Pout ≤ Pmax	NR20M30		-52	-39	
EVM	HPM, VCC = 4.2V, Pout ≤ Pmax	NR20M65		2		%

Band 7 4G LTE Tx Characteristics (Not available in E part number)

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, QPSK, 10MHz, 12 Resource Blocks with MPR=0. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 7	2500		2570	MHz
Maximum Linear Output Power	HPM, VCC = 3.8V	25			dBm
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C	24			
Gain	HPM, VCC = 3.8V		29		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		28		
	LPM, VCC =1.2V, Pout=10dBm		26		
	LPM, VCC =0.7V, Pout=2dBm		19		
EUTRA - ACLR	HPM, VCC = 3.8V, Pout ≤ Pmax		-40	-33	dBc
UTRA - ACLR1	HPM, VCC = 3.8V, Pout ≤ Pmax		-42	-36	
UTRA - ACLR2	HPM, VCC = 3.8V, Pout ≤ Pmax		-55	-39	
EVM	All modulations		1.5		%
Gain transient time	Gain transient time between PA modes		--	10	µs
PAE	HPM, VCC = 3.8V, Pout = Pmax		12		%
Quiescent Current	HPM, VCC = 3.8V, No RF		130		mA
Current Consumption	HPM, VCC = 3.8V, Pout = Pmax		625		mA
	LPM, VCC = 0.7V, Pout=2dBm		80		

Band 7 Rx Characteristics (Not available in E part number)

Test conditions unless otherwise stated: VDD_LNA=1.2V, Temp = 25°C, VBATT = 3.8V, PA disabled, Gain state G1. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 7	2620		2690	MHz
RF Gain	Gain state 0 (G0)		15.2		dB
	Gain state 1 (G1)		12		
	Gain state 2 (G2)		10.6		
	Gain state 3 (G3)		7		
	Gain state 4 (G4)		4.8		
	Gain state 5 (G5)		0.5		
	Gain state 6 (G6)		-2.5		
	Gain state 7 (G7)		-6.6		
	Gain state 8 (G8)		TBD 8.2		
	Gain state 9 (G9)		-10		
	Gain state 10 (G10)		-15.8		
Drain Current	Gain state 0 (G0)		8.5		mA
	Gain state 1 (G1)		7.5		
	Gain state 2 (G2)		6.5		
	Gain state 3 (G3)		5.5		
	Gain state 4 (G4)		5.1		
	Gain state 5 (G5)		5.1		
	Gain state 6 (G6)		4.8		
	Gain state 7 (G7)		3.5		
	Gain state 8 (G8)		TBD 1		
	Gain state 9 (G9)		0.1		
	Gain state 10 (G10)		0.1		
Noise Figure	Gain state 0 (G0)		4.3		dB
	Gain state 1 (G1)		4.4		
	Gain state 2 (G2)		4.7		
	Gain state 3 (G3)		5		
	Gain state 4 (G4)		5.4		
	Gain state 5 (G5)		6.7		
	Gain state 6 (G6)		9.7		
	Gain state 7 (G7)		11.8		
	Gain state 8 (G8)		TBD 4.3		
	Gain state 9 (G9)		9.3		
	Gain state 10 (G10)		15.3		
Input Return Loss	Rx On, Gain state 1 (G1)		8.5		dB
Output Return Loss	Rx On, Gain state 1 (G1)		8.5		
Tx Leakage Power	Gain state 1 (G1), PA enabled, Tx Pout ≤ Pmax, 5MHz QPSK 25RB		TBD -25		dBm/5MHz
Reverse Isolation	Rx out to ANT, Active Gain state only		32		dB
Timing, LPM to Active	Gain settling within 0.2dB of final value when LNA is turned on (after Bus Park)		1.8		µs
Timing, LNA Enable			1.7		
Timing, Gain State Change	Switching between any two gain modes		0.5		

Band 40 4G LTE and 5G NR Common Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 40	2300		2400	MHz
Noise at LNA Out (LNA_Out0 ~ LNA_Out3, LNA on, G1)					
B1 Rx Band Noise, DL CA	2110 – 21700MHz, 20MHz QPSK 75RB		-155		dBm/Hz
B3 Rx Band Noise, DL CA	1805 – 18800MHz, 20MHz QPSK 75RB		-155		
Co-existence Noise at ANT (ANT1 or ANT2)					
LB RX Band Noise	699 – 960MHz, 40MHz QPSK 200RB		-182		dBm/Hz
GPS Band Noise	1574 – 1577MHz, 40MHz QPSK 200RB		-178		
GLONASS/Beidou Band Noise	1559 – 1606MHz, 40MHz QPSK 200RB		-178		
ISM 2.4G Noise	2402 – 2432MHz, 40MHz QPSK 200RB		-105		
	2427 – 2447MHz, 40MHz QPSK 200RB		-145		
	2452 – 2477MHz, 40MHz QPSK 200RB		-161		
	2462 – 2482MHz, 40MHz QPSK 200RB		-165		
n77 RX Band Noise	3300 – 4200MHz, 20MHz QPSK 100RB		-183		
n79 RX Band Noise	4400 – 5000MHz, 20MHz QPSK 100RB		-164		
ISM 5G Noise (except harmonics)	5150 – 5850MHz, 40MHz QPSK 200RB		-184		
Harmonics at ANT ports (10MHz QPSK 12RB)	2f0		-53		dBm
	3f0		-63		
	≥4f0		-46		
Stability, spurious output level	Output Load VSWR 6:1, all phases angles, Pout = Prated Closed Loop, CW Modulation, VCC=3.4V to 4.6V, Temp = -30°C to +85°C			-70	dBc

Band 40 5G NR Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

Parameter	Conditions		Min.	Typ.	Max.	Units
Operational Frequency Range	NR Band n40		2300		2400	MHz
Maximum Linear Output Power	HPM, VCC = 4.2V,	NR80M00	25			dBm
Gain	HPM, VCC = 4.2V	NR80M00		29		dB
	HPM, VCC = 4.2V, VBAT=3.8V, Temp = -20°C to +85°C	NR80M00		27		
	LPM, VCC =1.2V, Pout=12dBm	NR80M00		26		
	LPM, VCC =0.7V, Pout=2dBm	NR80M00		22		
PAE	HPM, VCC = 4.2V, Pout = Pmax	NR80M00		12		%
Current Consumption	HPM, VCC = 4.2V, Pout = Pmax	NR80M00		685		mA
	LPM, VCC ≤ 0.7V, Pout=2dBm	NR80M00		65		
EUTRA ACLR	HPM, VCC = 4.2V, Pout ≤ Pmax	NR80M30		-42	-33	dBc
UTRA - ACLR1	HPM, VCC = 4.2V, Pout ≤ Pmax	NR80M30		-44	-36	
UTRA - ACLR2	HPM, VCC = 4.2V, Pout ≤ Pmax	NR80M30		-51	-39	
EVM	HPM, VCC = 4.2V, Pout ≤ Pmax	NR80M65		2		%

Band 40 4G LTE Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, QPSK, 10MHz, 12 Resource Blocks with MPR=0. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 40	2300		2400	MHz
Maximum Linear Output Power	HPM, VCC = 3.8V	25			dBm
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C	24			
Maximum Linear Output Power (Power Class 2)	HPM, VCC = 4.8V		28		dBm
	HPM, VCC = 4.8V, VBATT=3.8V, Temp = -20°C to +85°C		27		
Gain	HPM, VCC = 3.8V		28.5		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		27.5		
	LPM, VCC =1.1V, Pout=12dBm		25		
	LPM, VCC =0.6V, Pout=2dBm		22		
EUTRA - ACLR	HPM, VCC = 3.8V, Pout ≤ Pmax		-45	-33	dBc
UTRA - ACLR1	HPM, VCC = 3.8V, Pout ≤ Pmax		-46	-36	
UTRA - ACLR2	HPM, VCC = 3.8V, Pout ≤ Pmax		-54	-39	
EVM	All modulations		2		%
Gain transient time	Gain transient time between PA modes		--	10	µs
PAE	HPM, VCC = 3.8V, Pout = Pmax		13		%
Quiescent Current	HPM, VCC = 3.8V, No RF		125		mA
Current Consumption	HPM, VCC = 3.8V, Pout = Pmax		600		mA
	LPM, VCC = 0.6V, Pout=2dBm		80		

Band 40 Rx Characteristics

Test conditions unless otherwise stated: VDD_LNA=1.2V, Temp = 25°C, VBATT = 3.8V, PA disabled, Gain state G1. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 40	2300		2400	MHz
RF Gain	Gain state 0 (G0)		15.7		dB
	Gain state 1 (G1)		13.8		
	Gain state 2 (G2)		10.4		
	Gain state 3 (G3)		7.6		
	Gain state 4 (G4)		4.4		
	Gain state 5 (G5)		0.5		
	Gain state 6 (G6)		-2.8		
	Gain state 7 (G7)		-6.4		
	Gain state 8 (G8)		TBD 5.8		
	Gain state 9 (G9)		-8.5		
	Gain state 10 (G10)		-14.2		
Drain Current	Gain state 0 (G0)		8.5		mA
	Gain state 1 (G1)		7.5		
	Gain state 2 (G2)		6.5		
	Gain state 3 (G3)		5.5		
	Gain state 4 (G4)		5.1		
	Gain state 5 (G5)		5.1		
	Gain state 6 (G6)		4.8		
	Gain state 7 (G7)		3.5		
	Gain state 8 (G8)		TBD 1		
	Gain state 9 (G9)		0.1		
	Gain state 10 (G10)		0.1		
Noise Figure	Gain state 0 (G0)		3.9		dB
	Gain state 1 (G1)		4.1		
	Gain state 2 (G2)		4.5		
	Gain state 3 (G3)		4.8		
	Gain state 4 (G4)		5.3		
	Gain state 5 (G5)		6.5		
	Gain state 6 (G6)		9.7		
	Gain state 7 (G7)		11.5		
	Gain state 8 (G8)		TBD 5		
	Gain state 9 (G9)		8.6		
	Gain state 10 (G10)		14		
Input Return Loss	Rx On, Gain state 1 (G1)		13		dB
Output Return Loss	Rx On, Gain state 1 (G1)		8		
Reverse Isolation	Rx out to ANT, Active Gain state only		33		dB
Timing, LPM to Active	Gain settling within 0.2dB of final value when LNA is turned on (after Bus Park)		1.6		µs
Timing, LNA Enable			1.5		
Timing, Gain State Change	Switching between any two gain modes		0.7		

Band 41/38 4G LTE and 5G NR Common Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 38	2570		2620	MHz
	Band 41 Limited for Power Class 2	2515		2675	
	Band 41	2496		2690	
Noise at LNA Out (LNA_Out0 ~ LNA_Out3, LNA on, G1)					
B1 Rx Band Noise, DL CA	2110 – 21700MHz, 40MHz QPSK 200RB		-156		dBm/Hz
B3 Rx Band Noise, DL CA	1805 – 18800MHz, 40MHz QPSK 200RB		-156		
Co-existence Noise at ANT (ANT1 or ANT2)					
LB RX Band Noise	699 – 960MHz, 40MHz QPSK 200RB		-180		dBm/Hz
GPS Band Noise	1574 – 1577MHz, 40MHz QPSK 200RB		-179		
GLONASS/Beidou Band Noise	1559 – 1606MHz, 40MHz QPSK 200RB		-179		
ISM 2.4G Noise	2402 – 2432MHz, 40MHz QPSK 200RB		-150		
	2427 – 2447MHz, 40MHz QPSK 200RB		-147		
	2452 – 2472MHz, 40MHz QPSK 200RB		-119		
	2457 – 2477MHz, 40MHz QPSK 200RB		-103		
	2457 – 2482MHz, 40MHz QPSK 200RB		-89		
n77 RX Band Noise	3300 – 4200MHz, 20MHz QPSK 100RB		-171		
n79 RX Band Noise	4400 – 5000MHz, 20MHz QPSK 100RB		-187		
ISM 5G Noise (except harmonics)	5150 – 5850MHz, 40MHz QPSK 200RB		-187		
Harmonics at ANT ports (10MHz QPSK 12RB)	2f0		TBD -38		dBm
	3f0		-57		
	≥4f0		-48		
Stability, spurious output level	Output Load VSWR 6:1, all phases angles, Pout = Prated Closed Loop, CW Modulation, VCC=3.4V to 4.6V, Temp = -30°C to +85°C			-70	dBc

Band 41/38 5G NR Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

Parameter	Conditions		Min.	Typ.	Max.	Units
Operational Frequency Range	NR Band 38		2570		2620	MHz
	NR Band 41 Limited for Power Class 2		2515		2675	
	NR Band 41		2496		2690	
Maximum Linear Output Power	HPM, VCC = 4.2V,	NR100M00	25			dBm
Gain	HPM, VCC = 4.2V	NR100M00		28		dB
	HPM, VCC = 4.2V, VBAT=3.8V, Temp = -20°C to +85°C	NR100M00		27		
	LPM, VCC =1.2V, Pout=12dBm	NR100M00		26		
	LPM, VCC =0.7V, Pout=2dBm	NR100M00		24		
PAE	HPM, VCC = 4.2V, Pout = Pmax	NR100M00		10		%
Current Consumption	HPM, VCC = 4.2V, Pout = Pmax	NR100M00		780		mA
	LPM, VCC ≤ 0.7V, Pout=2dBm	NR100M00		80		
NR ACLR	HPM, VCC = 4.2V, Pout ≤ Pmax	NR100M30		-38	-33	dBc
EVM	HPM, VCC = 4.2V, Pout ≤ Pmax	NR100M65		2		%

Band 41/38 4G LTE Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, QPSK, 10MHz, 12 Resource Blocks with MPR=0. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 38	2570		2620	MHz
	Band 41 Limited for Power Class 2	2515		2675	
	Band 41	2496		2690	
Maximum Linear Output Power (Power Class 3)	ET, VCC <= 5.1V	26			dBm
	HPM, VCC = 3.8V	25			
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C	24			
Maximum Linear Output Power (Power Class 2)	ET, VCC <= 5.1V		29		dBm
	HPM, VCC = 4.8V		28		
	HPM, VCC = 4.8V, VBATT=3.8V, Temp = -20°C to +85°C		27		
Gain	HPM, VCC = 3.8V, Power Class 3		28		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C, Power Class 3		27		
	HPM, VCC = 4.8V, Power Class 2		28		
	HPM, VCC = 4.8V, VBATT=3.8V, Temp = -20°C to +85°C, Power Class 2		27		
	LPM, VCC =1.2V, Pout=12dBm		25		
	LPM, VCC =0.7, Pout=2dBm		23		
EUTRA - ACLR	HPM, Pout ≤ Pmax		-40	-33	dBc
UTRA - ACLR1 (B38)	HPM, Pout ≤ Pmax Power Class 3		-43	-36	
UTRA - ACLR2 (B38)	HPM, Pout ≤ Pmax Power Class 3		-52	-39	
EVM	All modulations		1.8		%
Gain transient time	Gain transient time between PA modes		-	10	µs
PAE (Power Class 3)	HPM, VCC = 3.8V, Pout = Pmax		11		%
Quiescent Current	HPM, VCC = 3.8V, No RF		125		mA
Current Consumption (PC3)	HPM, VCC = 3.8V, Pout = Pmax		750		mA
	LPM, VCC = 0.7V, Pout=2dBm		60		

Band 41/38 Rx Characteristics

Test conditions unless otherwise stated: VDD_LNA=1.2V, Temp = 25°C, VBATT = 3.8V, PA disabled, Gain state G1. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 38	2570		2620	MHz
	Band 41	2496		2690	
RF Gain	Gain state 0 (G0)		14.7		dB
	Gain state 1 (G1)		12.9		
	Gain state 2 (G2)		9.8		
	Gain state 3 (G3)		7.2		
	Gain state 4 (G4)		4.1		
	Gain state 5 (G5)		0.6		
	Gain state 6 (G6)		-3.6		
	Gain state 7 (G7)		-6.9		
	Gain state 8 (G8)		TBD 7		
	Gain state 9 (G9)		-10.4		
	Gain state 10 (G10)		-16.2		
Drain Current	Gain state 0 (G0)		8.5		mA
	Gain state 1 (G1)		7.5		
	Gain state 2 (G2)		6.5		
	Gain state 3 (G3)		5.5		
	Gain state 4 (G4)		5.1		
	Gain state 5 (G5)		5.1		
	Gain state 6 (G6)		4.8		
	Gain state 7 (G7)		3.5		
	Gain state 8 (G8)		TBD 1		
	Gain state 9 (G9)		0.1		
	Gain state 10 (G10)		0.1		
Noise Figure	Gain state 0 (G0)		5.2		dB
	Gain state 1 (G1)		6		
	Gain state 2 (G2)		6.3		
	Gain state 3 (G3)		6.5		
	Gain state 4 (G4)		6.8		
	Gain state 5 (G5)		7.6		
	Gain state 6 (G6)		11.2		
	Gain state 7 (G7)		12.7		
	Gain state 8 (G8)		TBD 5.9		
	Gain state 9 (G9)		10.6		
	Gain state 10 (G10)		16.2		
Input Return Loss	Rx On, Gain state 1 (G1)		7		dB
Output Return Loss	Rx On, Gain state 1 (G1)		10		
Reverse Isolation	Rx out to ANT, Active Gain state only		36		dB
Timing, LPM to Active	Gain settling within 0. 2dB of final value when LNA is turned on (after Bus Park)		1.1		µs
Timing, LNA Enable			1.1		
Timing, Gain State Change	Switching between any two gain modes		0.9		

HB_AUX 4G LTE Tx Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode, QPSK, 10MHz, 12 Resource Blocks with MPR=0. Performance referenced to module pin location B30_TX (HB_AUX).

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	High Band 30	2305		2315	MHz
Maximum Linear Output Power	HPM, VCC = 3.8V		30		dBm
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		29		
Gain	HPM, VCC = 3.8V		32		dB
	HPM, VCC = 3.8V, VBATT=3.8V, Temp = -20°C to +85°C		31		
	LPM, VCC =1.1V, Pout=15dBm		27		
	LPM, VCC =0.6V, Pout=5dBm		22		
EUTRA - ACLR	HPM, VCC = 3.8V, Pout ≤ Pmax		-43	-33	dBc
UTRA - ACLR1	HPM, VCC = 3.8V, Pout ≤ Pmax		-46	-36	
UTRA - ACLR2	HPM, VCC = 3.8V, Pout ≤ Pmax		-53	-39	
EVM	All modulations		1.3		%
Gain transient time	Gain transient time between PA modes		--	10	µs
PAE	HPM, VCC = 3.8V, Pout = Pmax		33		%
Quiescent Current	HPM, VCC = 3.8V, No RF		125		mA
Current Consumption	HPM, VCC = 3.8V, Pout = Pmax		650		mA
	LPM, VCC = 0.6V, Pout = 5dBm		90		
LB RX Band Noise	699 – 960MHz, 40MHz QPSK 200RB		-157		dBm/Hz
MB RX Band Noise	1452 – 2200MHz, 40MHz QPSK 200RB		-147		
ISM 5G Noise (except harmonics)	5150 – 5850MHz, 20MHz QPSK 100RB		-156		
GPS Band Noise	1574 – 1577MHz, 20MHz QPSK 100RB		-146		
Harmonics	2f0		-15		dBm
	3f0		-24		
Stability, spurious output level	Output Load VSWR 6:1, all phases angles, Pout = Prated Closed Loop, CW Modulation, VCC=3.4V to 4.6V, Temp = -30°C to +85°C			-70	dBc

2G_HB_IN Port Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Frequency Range	DCS/PCS	1710		1990	MHz
Insertion Loss	DCS/PCS		0.85		dB
PCS/DCS Harmonics, 2f0 and 3f0	Pin=34dBm		-68		dBm

TRX Port Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Frequency Range		1700		2690	MHz
Insertion Loss TRX1	1700 – 2200MHz		1.9		dB
	2300 – 2690MHz		2.6		
Insertion Loss TRX2	1700 – 2200MHz		1.3		dB
	2300 – 2690MHz		1.9		
Insertion Loss TRX3	1700 – 2200MHz		1.6		dB
	2300 – 2690MHz		2.1		
Insertion Loss TRX4	1700 – 2200MHz		1.4		dB
	2300 – 2690MHz		2.0		
Harmonic, 2f0	Pin=28dBm		-85		dBm
Harmonic, 3f0	Pin=28dBm		-85		

Note: TRX port mismatch loss may be optimized with external tuning circuit.

CPL_Out Port Characteristics

Test conditions unless otherwise stated: All unused RF ports terminated in 50Ω, Input and Output = 50Ω, Temp = 25°C, VBATT = 3.8V, APT Mode with proper MPR. Performance referenced to module pin location.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operational Frequency Range	Band 1	1920		1980	MHz
Coupling factor	Coupler Mode = MB FWD		23.9		dB
	Coupler Mode = MB REV		21.8		
Directivity	Coupler Mode = MB FWD		26.8		dB
	Coupler Mode = MB REV		12.1		
Operational Frequency Range	Band 3/4/66	1710		1785	MHz
Coupling factor	Coupler Mode = MB FWD		24.9		dB
	Coupler Mode = MB REV		23.3		
Directivity	Coupler Mode = MB FWD		31.7		dB
	Coupler Mode = MB REV		11.6		
Operational Frequency Range	Band 7	2500		2570	MHz
Coupling factor	Coupler Mode = HB FWD		21.5		dB
	Coupler Mode = HB REV		20.9		
Directivity	Coupler Mode = HB FWD		18.8		dB
	Coupler Mode = HB REV		11.4		
Operational Frequency Range	Band 34	2010		2025	MHz
Coupling factor	Coupler Mode = MB FWD		23.7		dB
	Coupler Mode = MB REV		21.5		
Directivity	Coupler Mode = MB FWD		27.1		dB
	Coupler Mode = MB REV		12.3		
Operational Frequency Range	Band 39	1880		1920	MHz
Coupling factor	Coupler Mode = MB FWD		24.2		dB
	Coupler Mode = MB REV		21.3		
Directivity	Coupler Mode = MB FWD		21.5		dB
	Coupler Mode = MB REV		12.7		
Operational Frequency Range	Band 40	2300		2400	MHz
Coupling factor	Coupler Mode = HB FWD		21.9		dB
	Coupler Mode = HB REV		22.8		
Directivity	Coupler Mode = HB FWD		22.7		dB
	Coupler Mode = HB REV		9		
Operational Frequency Range	Band 41/38	2496		2690	MHz
Coupling factor	Coupler Mode = HB FWD		21.3		dB
	Coupler Mode = HB REV		19.9		
Directivity	Coupler Mode = HB FWD		19.2		dB
	Coupler Mode = HB REV		11.4		

MIPI RFFE Information

Bus Information

MIPI RFFE Bus	MIPI RFFE Version	Default USID	Product ID	Manufacturer ID
Bus #1 (VIO, SCLK, SDATA) Power Amplifier(s), Tx Rx Filters and Antenna Path Configuration	3.0	15 (0xF)	42 (0x2A)	966 (0x3C6) - Qorvo
Bus #2 (VIO2, SCLK2, SDATA2) LNA Gain, LNA Path Configuration	3.0	3 (0x3)	43 (0x2B)	966 (0x3C6) - Qorvo

Register Details

This section displays each register in table form. Table headers described here:

Bit(s) – Value 0 through 7 indicating bit position within the byte (8 bits). A range is indicated by M:L where M is the most significant and L is the least significant bit of the range.

Field Name – Name given to the bit field within Qorvo Optimizer software. All names must be unique.

Default – The value of the register after a power-on reset.

Description – description of the Bit Field and how the values are used.

R/W – Indicates whether a Bit Field is used for Read, Write, or both. NOTE: At the RFFE bus level, all registers can be read or written to. This column helps the user know what to expect after a bus level read or write. If a Bit Field is labeled “W” (write), a read will always return the default value. If a Bit Field is labeled “R” (read), a write can be performed, but it will not change the value.

B/G/M – Indicates whether a **B**roadcast, **G**roup, or **M**asked Write Command can be used to access the Bit Field.

Trig – Indicates whether the Write Command can be triggered. The value in the Trig column indicates which trigger causes the Bit Field to be loaded from the shadow register. “T012” means that any or all triggers will cause a load from shadow register. “T2” means that trigger 2 will load the register; trigger 1 or trigger 0 will have no effect. “No” means that triggered operation does not apply. Extended triggers noted with ET3 – ET10. The extended triggers are assigned to mT-A, mT-B, mT-C, mT-D in Registers 22 – 27. Extended trigger mask is Register 45. Extended trigger bits are in Register 46.

Bus #1 Register Details

Bus #1 Reg00 (0x00) – PA_CTRL0 (Configures and Enables MB or HB Power Amplifier)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	Reserved	1b0	Not Used	R/W	No	T0
6:3	PA_BAND	4b0000	0000: PA_disabled 0001: B1 0010: B3_B4 0011: B7 0100: MB_AUX1 0101: HB_AUX 0110: B39 0111: B34 1000: B40 1001: B41 1010: reserved 1011: MB_AUX2 1100-1111: reserved (=PA_disabled)			
2	PA_EN	1b0	0: PA Off 1: PA On			
1:0	PA_MODE	2b00	00: HPM vc (internal voltage control) 01: HPM cc (internal current control) 10: LPM cc (internal current control) 11: reserved			

Bus #1 Reg01 (0x01) – PA_CTRL1 (Configures Bias for Active Power Amplifier)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:5	Reserved	1b0	Not Used	R/W	No	T0
4:0	PA_BIAS_1	5b0_0000	PA Bias - driver stage			

Reg01 Usage

Recommended register values are available from Qorvo Application Engineering in a Bias table based on Modulation Signal, Band, and output power level. The values are developed for use on the evaluation board and subject to change.

Bus #1 Reg02 (0x02) – PA_CTRL2 (Configures Cap Switch and Bias for Active Power Amplifier)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	CAP_SW	1b0	Connects external decoupling capacitor to GND 0: open (usually ET mode) 1: closed (usually APT mode)	R/W	No	T0
6:5	Reserved	2b00	Reserved			
4:0	PA_BIAS_2	5b0_0000	PA Bias - power (final) stage			

PA_BIAS_2 Usage

Recommended register values are available from Qorvo Application Engineering in a Bias table based on Modulation Signal, Band, and output power level. The values are developed for use on the evaluation board and subject to change.

Bus #1 Reg03 (0x03) – ASW_CTRL (Configures Antenna Switches)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	ASW2	4b0000	Antenna Switch Control for ANT2 0000: off (high isolation) 0001: ANT2_HBIN_2G 0010: ANT2_TX_1_3_4_40_RX_1_3_4_32_40 0011: ANT2_TX_1_3_4_40_41_RX_1_3_4_32_40_41 0100: ANT2_TX_1_3_4_7_40_RX_1_3_4_7_32_40 0101: ANT2_TRX1 0110: Reserved 0111: ANT2_TX_34_39 1000: ANT2_TRX4 1001: ANT2_TRX2 1010: ANT2_TRX3 1011: ANT2_TX_41_RX_41 1100: ANT2_TX_41_RX_34_39_41 1101: ANT2_RX_34_39 1110-1111: off (high isolation)	R/W	M	T1
3:0	ASW1	4b0000	Antenna Switch Control for ANT1 0000: off (high isolation) 0001: ANT1_HBIN_2G 0010: ANT1_TX_1_3_4_40_RX_1_3_4_32_40 0011: ANT1_TX_1_3_4_40_41_RX_1_3_4_32_40_41 0100: ANT1_TX_1_3_4_7_40_RX_1_3_4_7_32_40 0101: ANT1_TRX1 0110: Reserved 0111: ANT1_TX_34_39 1000: ANT1_TRX4 1001: ANT1_TRX2 1010: ANT1_TRX3 1011: ANT1_TX_41_RX_41 1100: ANT1_TX_41_RX_34_39_41 1101: ANT1_RX_34_39 1110-1111: off (high isolation) Note - if Ant2 and Ant1 selection conflict, ANT1 routing takes effect.			

Bus #1 Reg04 (0x04) – XSW_CTRL (Configures Distribution Switches)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	XSW_MB	4b0000	Distribution Switch Control for MB 0000: off 0001: B3B4TX 0010: B1TX 0011: B34_ B39TX 0100: reserved 0101: MB_AUX2 0110: MB_AUX1 0111-1111: reserved			
3:0	XSW_HB	4b0000	Distribution Switch Control for HB 0000: off 0001: B40TX 0010: reserved 0011: B41TX 0100: HB_AUX 0101: B40RX 0110: B7TRX 0111: B41RX_B40RX_CA 1000: B41RX 1001: B40RX_CA 1010-1111: reserved	R/W	M	T1

Bus #1 Reg05 (0x05) – CPL_CTRL (Configures RF Power Coupler)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:5	Reserved	5b0_0000	reserved	R/W	No	T2
2:0	CPL	3b000	0000: off 0001: ANT1 MB FWD 0010: ANT1 HB FWD 0011: ANT1 MB REV 0100: ANT1 HB REV 0101: ANT2 MB FWD 0110: ANT2 HB FWD 0111: ANT2 MB REV 1000: ANT2 HB REV 1001: CPL bypass 1010-1111: off			

Bus #1 Reg06 (0x06) – ANT_CPL_CTRL (Configures Antenna and RF Power Coupler Swap)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:3	Reserved	6b00_0000	reserved	R/W	No	T1
1	CPL_INDEP	1b0	reserved			
0	ANT_CPL_SWAP	1b0	Antenna and coupler control swapping 0: default (Ant2 controlled by Reg3[7:4], Ant1 controlled by Reg2[3:0], 1: swapped (Ant1 controlled by Reg03[7:4], Ant2 controlled by Reg03[3:0]			

Bus #1 Reg07 (0x07) – XSW_CTRL2 (Configures MB Distribution Switch, Alternate Register)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	Reserved	4b0000	Reserved	R/W	M	T2
3:0	XSW_MB_MODE1	4b0000	Distribution Switch Control for MB 0000: off 0001: B3B4TX 0010: B1TX 0011: B34_ B39TX 0100: reserved 0101: MB_AUX2 0110: MB_AUX1 0111-1111: reserved			

Bus #1 Reg08 (0x08) – PA_CTRL3 (Configures Bias for Active Power Amplifier, Alternate Register)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	PA_BIAS_2_MODE2	4b0000	PA Bias – power (final) stage	R/W	No	T0
3:0	PA_BIAS_1_MODE2	4b0000	PA Bias - driver stage			

PA_BIAS Usage

Recommended register values are available from Qorvo Application Engineering in a Bias table based on Modulation Signal, Band, and output power level. The values are developed for use on the evaluation board and subject to change.

Bus #1 Reg09 (0x09) – PA_CTRL4 (Configures Cap Switch, Alternate Register)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:1	Reserved	7b0000_000	Reserved	R/W	No	T0
0	CAP_SW_MODE2	1b0	Connects external decoupling capacitor to GND 0: open (usually ET mode) 1: closed (usually APT mode)			

Bus #1 Reg28 (0x1C) – PM_TRIG (RFFE Power Mode and Triggers)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	PWR_MODE	1b1	0: Normal operation (ACTIVE) 1: Secondary mode (LOW POWER)	R/W	B/G	No
6	PWR_STATE	1b0	0: Normal operation 1: initialization state note - this bit always reads 0. Writing a 1 to this bit forces a reset.	W	B/G	No
5:3	TRIGGERMASK[2:0]	3b000	Setting these bits to '1' will cause the corresponding triggers to be masked (disabled), and RFFE writes to corresponding registers will change configuration immediately (no trigger command necessary). TriggerMask[2] = TriggerMask_2, TriggerMask[1] = TriggerMask_1, & TriggerMask[0] = TriggerMask_0 Note: Qorvo products do not allow changing the trigger mask and sending triggers within the same RFFE write.	R/W	No	No
2:0	TRIGGER[2:0]	3b000	Setting these bits to '1' will cause the registers associated with that trigger to be loaded with the contents of its corresponding shadow register. Trigger[2] = Trigger_2, Trigger[1] = Trigger_1, and Trigger[0] = Trigger_0 Note: Qorvo products do not allow changing the trigger mask and sending triggers within the same RFFE write.	W	B/G	No

Bus #1 Reg29 (0x1D) – PRODUCT_ID (Device Identification)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	PRODUCT_ID	8b0010_1010 0x2A	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	R	No	No

Bus #1 Reg30 (0x1E) – MANUFACTURER_ID (Device Identification)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	MANUFACTURER_ID_LSB	8b1100_0110 0xC6	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value. Note: This is the lower 8 least significant bits of the RFFE's MANUFACTURER_ID (i.e. MANUFACTURER_ID[7:0] = MANUFACTURER_ID_LSB	R	No	No

Bus #1 Reg31 (0x1F) – MAN_US_ID (Device Identification)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	MANUFACTURER_ID_MSB	4b0011 0x3	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value. Note: This is the 4 most significant bits of the RFFE's MANUFACTURER_ID (i.e. MANUFACTURER_ID[11:8] = MANUFACTURER_ID_MSB	R	No	No
3:0	USID	4b1111 0xF	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device (customer specified).	R/W	No	No

Bus #1 Reg32 (0x20) – EXT_PRODUCT_ID (Extended Product ID)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	EXT_PRODUCT_ID	8b0000_0000	'This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	R	No	No

Bus #1 Reg33 (0x21) – REVISION_ID (Revision ID)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	REVISION_ID	8b0000_0000	This is an RFFE2 register to contain information about the revision of this module. The intent here is to use this as a type of scratch register -- to contain various information or serialization.	R	No	No

Bus #1 Reg34 (0x22) – GROUP_ID2 (Programmable Group Slave ID)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	GSID0_2	4b0000	Group slave ID 0 There is only 1 register for GSID0 & GSID1, but this register can be accessed from either Reg27 or Reg34. This means that write to Reg34 will reflect in Reg27 also, and vice versa.	R/W	No	No
3:0	GSID1_2	4b0000	Group slave ID 1 There is only 1 register for GSID0 & GSID1, but this register can be accessed from either Reg27 or Reg34. This means that write to Reg34 will reflect in Reg27 also, and vice versa.			

Bus #1 Reg35 (0x23) – UDR_RST (RFFE_STATUS2)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	SW_RESET_2	1b0	0: Normal operation 1: Software reset (reset of all configurable registers to default values, except for USID) There is only 1 register for RFFE_STATUS, but this register can be accessed from either Reg26 or Reg35. This means that write to Reg35 will reflect in Reg26 also, and vice versa	W	No	No
6:0	Reserved	7b000_0000	Unused	W	No	No

Bus #1 Reg36 (0x24) – ERR_SUM (RFFE_STATUS3)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	Spare_Reg36	1b0	Unused	R	No	No
6	CMD_FRAME_P_ERR_2	1b0	Command Frame received with a parity error – discard command	R		
5	CMD_LEN_ERR_2	1b0	Command length error			
4	ADDR_FRAME_P_ERR_2	1b0	Address frame parity error			
3	DATA_FRAME_P_ERR_2	1b0	Data frame with parity error			
2	READ_UNUSED_REG_2	1b0	Read command to an invalid address			
1	WRITE_UNUSED_REG_2	1b0	Write command to an invalid address			
0	BID_GID_ERR_2	1b0	Read command with a Broadcast_ID or GROUP_ID			

Bus #1 Reg43 (0x2B) – BUS_LOAD (Configure SDATA driver for RFFE bus load in application)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	Reserved	4b0000	Not Used	R/W	No	No
3:0	BUS_LOAD	4b0100	SDATA Driver strength in Readback Mode 0x0: 10pf 0x1: 20pf 0x2: 30pf 0x3: 40pf 0x4: 50pf 0x5: 60pf 0x6: 80pf 0x7: 100pf 0x8: 120pf 0x9: 140pf 0xA: 160pf 0xB: 180pf 0xC: 200pf 0xD: 250pf 0xE-0xF: reserved	R/W	No	No

Bus #1 Reg44 (0x2C) – TEST_PATTERN (Fixed value for Slave Readback verification)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	TEST_PATTERN	8b1101_0010	A read of this register returns the test pattern	R	No	No

Bus #2 Register Details

Bus #2 Reg00 (0x00) – Place-holder (This register is not used)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	Reserved	8b0000_0000	reserved	R/W	M	No

Bus #2 Reg01 (0x01) – PATH0_CTRL0 (LNA Output 0 Gain, Enable)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	PATH0_BYP_TRIG	1b0	Path 0 Trigger Bypass If this bit is set, register write takes immediate effect regardless of trigger masks	R/W	M	mT-A
6	Reserved	1b1	Reserved			
5	Reserved	1b0	Reserved			
4	PATH0_LNA_EN	1b0	Path 0 LNA Enable 0 = disabled 1 = enabled			
3:0	PATH0_GAIN	4b0000	Gain state for the LNA connected on PATH0 0000 = G0 (max) 0001 = G1 (18dB) 0010 = G2 (15dB) 0011 = G3 (12dB) 0100 = G4 (9dB) 0101 = G5 (6dB) 0110 = G6 (3dB) 0111 = G7 (0dB) 1000 = G8 (-3dB) 1001 = G9 (-6dB) 1010 = G10 (-12dB) 1011 - 1111 = reserved (same as G9)			

Bus #2 Reg02 (0x02) – PATH0_CTRL1 (LNA Output 0 Tune Range, Enable2)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	PATH0_TUNE_RANGE	1b0	Selects the tuning range for the PATH0 LNA 0 = normal tuning 1 = special tuning	R/W	M	T1
6:1	Reserved	5b000_000	reserved			
0	PATH0_RF_EN	1b0	Path 0 LNA Enable #2 0 = disabled 1 = enabled Same functionality and Logic OR with PATH0_LNA_EN			

Bus #2 Reg03 (0x03) – PATH0_CTRL2 (LNA Output 0 Input/Band Select, Tune Value)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:5	PATH0_TUNE	3b000	PATH0 Tuning	R/W	M	T0
1	PATH0_MASK	1b0	Path 0 Trigger Mask (Trigger Bypass) Enables/disables triggered operation on Path0 gain register. 0: triggers enabled 1: triggers disabled (masked)			
3:0	LNA_PATH0	4b0000	Selects the band for LNA Output 0. (sets input and mux switches) 0000: off (hi iso) 0001: B39 0010: B3 0011: B25 0100: B34 0101: B1 0110: B66 0111: B40 1000: B41 1001: B7 1010: B30 1011: B32 1100: B40_CA 1101: B21 1110: MUX0_IN 1111: reserved (same as 0000)			

LNA_PATH0 Notes

PATH0_TUNE recommended register values are available from Qorvo Application Engineering in a Mode table of LNA paths and Bands. The values are developed for use on the evaluation board and subject to change.
Only one of B39, B3, or B25 may be selected between the 4 Paths.
Only one of B34, B1, or B66 may be selected between the 4 Paths
Only one of B40, B41, B7 or B30 may be selected between the 4 Paths.
Only one of B21, B32 or B40_CA may be selected between the 4 Paths
The same band may be selected to two Paths (gain may vary).

Bus #2 Reg06 (0x06) – PATH1_CTRL0 (LNA Output 1 Gain, Enable)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	PATH1_BYP_TRIG	1b0	Path 1 Trigger Bypass If this bit is set, register write takes immediate effect regardless of trigger masks	R/W	M	mT-B
6	Reserved	1b1	Reserved			
5	Reserved	1b0	Reserved			
4	PATH1_LNA_EN	1b0	Path 1 LNA Enable 0 = disabled 1 = enabled			
3:0	PATH1_GAIN	4b0000	Gain state for the LNA connected on PATH1 0000 = G0 (max) 0001 = G1 (18dB) 0010 = G2 (15dB) 0011 = G3 (12dB) 0100 = G4 (9dB) 0101 = G5 (6dB) 0110 = G6 (3dB) 0111 = G7 (0dB) 1000 = G8 (-3dB) 1001 = G9 (-6dB) 1010 = G10 (-12dB) 1011 - 1111 = reserved (same as G9)			

Bus #2 Reg07 (0x07) – PATH1_CTRL1 (LNA Output 1 Tune Range, Enable2)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	PATH1_TUNE_RANGE	1b0	Selects the tuning range for the PATH1 LNA 0 = normal tuning 1 = special tuning	R/W	M	T1
6:1	Reserved	5b000_000	reserved			
0	PATH1_RF_EN	1b0	Path 1 LNA Enable #2 0 = disabled 1 = enabled Same functionality and Logic OR with PATH1_LNA_EN			

Bus #2 Reg08 (0x08) – PATH1_CTRL2 (LNA Output 1 Input/Band Select, Tune Value)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:5	PATH1_TUNE	3b000	PATH1 Tuning			
1	PATH1_MASK	1b0	Path 1 Trigger Mask (Trigger Bypass) Enables/disables triggered operation on Path1 gain register. 0: triggers enabled 1: triggers disabled (masked)			
3:0	LNA_PATH1	4b0000	Selects the band for LNA Output 1. (sets input and mux switches) 0000: off (hi iso) 0001: B39 0010: B3 0011: B25 0100: B34 0101: B1 0110: B66 0111: B40 1000: B41 1001: B7 1010: B30 1011: B32 1100: B40_CA 1101: B21 1110: reserved 1111: reserved (same as 0000)	R/W	M	T0

LNA_PATH1 Notes

PATH1_TUNE recommended register values are available from Qorvo Application Engineering in a Mode table of LNA paths and Bands. The values are developed for use on the evaluation board and subject to change.
Only one of B39, B3, or B25 may be selected between the 4 Paths.
Only one of B34, B1, or B66 may be selected between the 4 Paths
Only one of B40, B41, B7 or B30 may be selected between the 4 Paths.
Only one of B21, B32 or B40_CA may be selected between the 4 Paths
The same band may be selected to two Paths (gain may vary).

Bus #2 Reg11 (0x0B) – PATH2_CTRL0 (LNA Output 2 Gain, Enable)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	PATH2_BYP_TRIG	1b0	Path 2 Trigger Bypass If this bit is set, register write takes immediate effect regardless of trigger masks	R/W	M	mT-C
6	PATH2_PRI	1b1	Path 2 Priority_A combines with Path 2 Priority B to select active gain register. 0: A modem cedes control 1: A register is used			
5	Reserved	1b0	Reserved			
4	PATH2_LNA_EN	1b0	Path 2 LNA Enable 0 = disabled 1 = enabled			
3:0	PATH2_GAIN	4b0000	Gain state for the LNA connected on PATH2 0000 = G0 (max) 0001 = G1 (18dB) 0010 = G2 (15dB) 0011 = G3 (12dB) 0100 = G4 (9dB) 0101 = G5 (6dB) 0110 = G6 (3dB) 0111 = G7 (0dB) 1000 = G8 (-3dB) 1001 = G9 (-6dB) 1010 = G10 (-12dB) 1011 - 1111 = reserved (same as G9)			

Bus #2 Reg12 (0x0C) – PATH2_CTRL1 (LNA Output 2 Tune Range, Enable2)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	PATH2_TUNE_RANGE	1b0	Selects the tuning range for the PATH2 LNA 0 = normal tuning 1 = special tuning	R/W	M	T1
6:1	Reserved	5b000_000	reserved			
0	PATH2_RF_EN	1b0	Path 2 LNA Enable #2 0 = disabled 1 = enabled Same functionality and Logic OR with PATH2_LNA_EN			

Bus #2 Reg13 (0x0D) – PATH2_CTRL2 (LNA Output 2 Input/Band Select, Tune Value)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:5	PATH2_TUNE	3b000	PATH2 Tuning	R/W	M	T0
1	PATH2_MASK	1b0	Path 2 Trigger Mask (Trigger Bypass) Enables/disables triggered operation on Path2 gain register. 0: triggers enabled 1: triggers disabled (masked)			
3:0	LNA_PATH2	4b0000	Selects the band for LNA Output 2. (sets input and mux switches) 0000: off (hi iso) 0001: B39 0010: B3 0011: B25 0100: B34 0101: B1 0110: B66 0111: B40 1000: B41 1001: B7 1010: B30 1011: B32 1100: B40_CA 1101: B21 1110: reserved 1111: reserved (same as 0000)			

LNA_PATH2 Notes

PATH2_TUNE recommended register values are available from Qorvo Application Engineering in a Mode table of LNA paths and Bands. The values are developed for use on the evaluation board and subject to change.
Only one of B39, B3, or B25 may be selected between the 4 Paths.
Only one of B34, B1, or B66 may be selected between the 4 Paths
Only one of B40, B41, B7 or B30 may be selected between the 4 Paths.
Only one of B21, B32 or B40_CA may be selected between the 4 Paths
The same band may be selected to two Paths (gain may vary).

Bus #2 Reg16 (0x10) – PATH3_CTRL0 (LNA Output 3 Gain, Enable)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	PATH3_BYP_TRIG	1b0	Path 3 Trigger Bypass If this bit is set, register write takes immediate effect regardless of trigger masks	R/W	M	mT-D
6	Reserved	1b1	Reserved			
5	Reserved	1b0	Reserved			
4	PATH3_LNA_EN	1b0	Path 3 LNA Enable 0 = disabled 1 = enabled			
3:0	PATH3_GAIN	4b0000	Gain state for the LNA connected on PATH3 0000 = G0 (max) 0001 = G1 (18dB) 0010 = G2 (15dB) 0011 = G3 (12dB) 0100 = G4 (9dB) 0101 = G5 (6dB) 0110 = G6 (3dB) 0111 = G7 (0dB) 1000 = G8 (-3dB) 1001 = G9 (-6dB) 1010 = G10 (-12dB) 1011 - 1111 = reserved (same as G9)			

Bus #2 Reg17 (0x11) – PATH3_CTRL1 (LNA Output 3 Tune Range, Enable2)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	PATH3_TUNE_RANGE	1b0	Selects the tuning range for the PATH3 LNA 0 = normal tuning 1 = special tuning	R/W	M	T1
6:1	Reserved	5b000_000	reserved			
0	PATH3_RF_EN	1b0	Path 3 LNA Enable #2 0 = disabled 1 = enabled Same functionality and Logic OR with PATH3_LNA_EN			

Bus #2 Reg18 (0x12) – PATH3_CTRL2 (LNA Output 3 Input/Band Select, Tune Value)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:5	PATH3_TUNE	3b000	PATH3 Tuning	R/W	M	T0
1	PATH3_MASK	1b0	Path 3 Trigger Mask (Trigger Bypass) Enables/disables triggered operation on Path3 gain register. 0: triggers enabled 1: triggers disabled (masked)			
3:0	LNA_PATH3	4b0000	Selects the band for LNA Output 3. (sets input and mux switches) 0000: off (hi iso) 0001: B39 0010: B3 0011: B25 0100: B34 0101: B1 0110: B66 0111: B40 1000: B41 1001: B7 1010: B30 1011: B32 1100: B40_CA 1101: B21 1110: MUX3_IN 1111: reserved (same as 0000)			

LNA_PATH3 Notes

PATH3_TUNE recommended register values are available from Qorvo Application Engineering in a Mode table of LNA paths and Bands. The values are developed for use on the evaluation board and subject to change.

Only one of B39, B3, or B25 may be selected between the 4 Paths.

Only one of B34, B1, or B66 may be selected between the 4 Paths

Only one of B40, B41, B7 or B30 may be selected between the 4 Paths.

Only one of B21, B32 or B40_CA may be selected between the 4 Paths

The same band may be selected to two Paths (gain may vary).

Bus #2 Reg21 (0x15) – PATH_RESET (Resets LNA path to default (Off state))

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	Reserved	4b0000	Reserved	W	M	No
3	PATH3_RESET	1b0	PATH3 Reset 0 = no action 1 = reset PATH3 path to 0000 (off) this bit auto-clears and will always read back as 0			
2	PATH2_RESET	1b0	PATH2 Reset 0 = no action 1 = reset PATH2 path to 0000 (off) this bit auto-clears and will always read back as 0			
1	PATH1_RESET	1b0	PATH1 Reset 0 = no action 1 = reset PATH1 path to 0000 (off) this bit auto-clears and will always read back as 0			
0	PATH0_RESET	1b0	PATH0 Reset 0 = no action 1 = reset PATH0 path to 0000 (off) this bit auto-clears and will always read back as 0			

Bus #2 Reg22 (0x16) –TRIG_SRC1 (Assigns Extended Trigger for mTrig_A)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	PATH0_TRIG_SOURCE	8b0000_0000	Trigger assignment for mTrig_A 00000001 = ET3 00000010 = ET4 00000100 = ET5 00001000 = ET6 00010000 = ET7 00100000 = ET8 01000000 = ET9 10000000 = ET10 00000000 = default (note - if multiple bits are set, resulting operation is undefined)	R/W	M	No

Bus #2 Reg23 (0x17) –TRIG_SRC2 (Assigns Extended Trigger for mTrig_B)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	PATH1_TRIG_SOURCE	8b0000_0000	Trigger assignment for mTrig_B 00000001 = ET3 00000010 = ET4 00000100 = ET5 00001000 = ET6 00010000 = ET7 00100000 = ET8 01000000 = ET9 10000000 = ET10 00000000 = default (note - if multiple bits are set, resulting operation is undefined)	R/W	M	No

Bus #2 Reg24 (0x18) –TRIG_SRC2 (Assigns Extended Trigger for mTrig_C)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	PATH2_TRIG_SOURCE	8b0000_0000	Trigger assignment for mTrig_C 00000001 = ET3 00000010 = ET4 00000100 = ET5 00001000 = ET6 00010000 = ET7 00100000 = ET8 01000000 = ET9 10000000 = ET10 00000000 = default (note - if multiple bits are set, resulting operation is undefined)	R/W	M	No

Bus #2 Reg25 (0x19) –TRIG_SRC3 (Assigns Extended Trigger for mTrig_D)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	PATH3_TRIG_SOURCE	8b0000_0000	Trigger assignment for mTrig_D 00000001 = ET3 00000010 = ET4 00000100 = ET5 00001000 = ET6 00010000 = ET7 00100000 = ET8 01000000 = ET9 10000000 = ET10 00000000 = default (note - if multiple bits are set, resulting operation is undefined)	R/W	M	No

Bus #2 Reg26 (0x1A) – MAP_TRIG1 (Assigns Default Extended Trigger for mT_A, mT_B)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	mTRIG_B	4b0001	Trigger assignment for mTrig_B (applies when "default" is selected in Reg0x17)	R/W	M	No
3:0	mTRIG_A	4b0000	Trigger assignment for mTrig_A (applies when "default" is selected in Reg0x16)			

Bus #2 Reg27 (0x1B) – MAP_TRIG2 (Assigns Default Extended Trigger for mT_C, mT_D)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	mTRIG_D	4b0010	Trigger assignment for mTrig_D (applies when "default" is selected in Reg0x19)	R/W	M	No
3:0	mTRIG_C	4b0011	Trigger assignment for mTrig_C (applies when "default" is selected in Reg0x18)			

Bus #2 Reg28 (0x1C) – PM_TRIG (RFFE Power Mode and Triggers)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	PWR_MODE	1b1	0: Normal operation (ACTIVE) 1: Secondary mode (LOW POWER)	R/W	Yes	No
6	PWR_STATE	1b0	0: Normal operation 1: initialization state note - this bit always reads 0. Writing a 1 to this bit forces a reset.	W	Yes	No
5:3	TRIGGERMASK[2:0]	3b000	Setting these bits to '1' will cause the corresponding triggers to be masked (disabled), and RFFE writes to corresponding registers will change configuration immediately (no trigger command necessary). TriggerMask[2] = TriggerMask_2, TriggerMask[1] = TriggerMask_1, & TriggerMask[0] = TriggerMask_0 Note: Qorvo does not allow for changing the trigger mask and sending triggers within the same RFFE write.	R/W	No	No
2:0	TRIGGER[2:0]	3b000	Setting these bits to '1' will cause the registers associated with that trigger to be loaded with the contents of its corresponding shadow register. Trigger[2] = Trigger_2, Trigger[1] = Trigger_1, and Trigger[0] = Trigger_0 Note: Qorvo does not allow for changing the trigger mask and sending triggers within the same RFFE write.	W	Yes	No

Bus #2 Reg29 (0x1D) – PRODUCT_ID (Device Identification)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	PRODUCT_ID	8b00101011 0x2B	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	R	No	No

Bus #2 Reg30 (0x1E) – MANUFACTURER_ID (Device Identification)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	MANUFACTURER_ID_LSB	8b1100_0110 0xC6	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value. Note: This is the lower 8 least significant bits of the RFFE's MANUFACTURER_ID (i.e. MANUFACTURER_ID[7:0] = MANUFACTURER_ID_LSB	R	No	No

Bus #2 Reg31 (0x1F) – MAN_US_ID (Device Identification)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	MANUFACTURER_ID_MSB	4b0011 0x3	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value. Note: This is the 4 most significant bits of the RFFE's MANUFACTURER_ID (i.e. MANUFACTURER_ID[11:8] = MANUFACTURER_ID_MSB	R	No	No
3:0	USID	4b0011 0x3	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device (customer specified).	W/R	No	No

Bus #2 Reg32 (0x20) – EXT_PRODUCT_ID (Extended Product ID)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	EXT_PRODUCT_ID	8b0000_0000	'This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	R	No	No

Bus #2 Reg33 (0x21) – REVISION_ID (Revision ID)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	REVISION_ID	8b0000_0000	This is an RFFE2 register to contain information about the revision of this module. The intent here is to use this as a type of scratch register -- to contain various information or serialization.	R	No	No

Bus #2 Reg34 (0x22) – GROUP_ID2 (Programmable Group Slave ID)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	GSID0_2	4b0000	Group slave ID 0	R/W	No	No
3:0	GSID1_2	4b0000	Group slave ID 1			

Bus #2 Reg35 (0x23) – VDD_RST (RFFE_STATUS2)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	SW_RESET_2	1b0	0: Normal operation 1: Software reset (reset of all configurable registers to default values, except for USID)	W	No	No
6:0	Reserved	0b000_0000	Unused	W	No	No

Bus #2 Reg36 (0x24) – ERR_SUM (RFFE_STATUS3)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7	Spare_Reg36	1b0	Unused	R	No	No
6	CMD_FRAME_P_ERR_2	1b0	Command Frame received with a parity error – discard command	R		
5	CMD_LEN_ERR_2	1b0	Command length error			
4	ADDR_FRAME_P_ERR_2	1b0	Address frame parity error			
3	DATA_FRAME_P_ERR_2	1b0	Data frame with parity error			
2	READ_UNUSED_REG_2	1b0	Read command to an invalid address			
1	WRITE_UNUSED_REG_2	1b0	Write command to an invalid address			
0	BID_GID_ERR_2	1b0	Read command with a Broadcast_ID or GROUP_ID			

Bus #2 Reg43 (0x2B) – BUS_LOAD (Configure SDATA driver for RFFE bus load in application)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:4	Reserved	4b0000	Not Used	R/W	No	No
3:0	BUS_LOAD	4b0000	SDATA Driver strength in Readback Mode 0x0: 10pf 0x1: 20pf 0x2: 30pf 0x3: 40pf 0x4: 50pf 0x5: 60pf 0x6: 80pf 0x7: 100pf 0x8: 120pf 0x9: 140pf 0xA: 160pf 0xB: 180pf 0xC: 200pf 0xD: 250pf 0xE-0xF: reserved	R/W	No	No

Bus #2 Reg44 (0x2C) – TEST_PATTERN (Fixed value for Slave Readback verification)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	TEST_PATTERN	8b1101_0010	A read of this register returns the test pattern	R	No	No

Bus #2 Reg45 (0x2D) – EXT_TRIG_A_MASK (Extended Trigger Mask)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	EXT_TRIGGER_A_MASK	8b0000_0000	Setting these bits to '1' will cause the corresponding triggers to be masked (disabled), and RFFE writes to corresponding registers will change configuration immediately (no trigger command necessary). Ext_Trigger_Mask[7] = TriggerMask_10 ... Ext_Trigger_Mask[0] = TriggerMask_3 Note: if the part is set for LOW POWER and a write to this register changes the masks, the change to the masks takes effect.	R/W	No	No

Bus #2 Reg46 (0x2E) – EXT_TRIGGER_A (Extended Trigger Register)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig.
7:0	EXT_TRIGGER_BLK_A	8b0000_0000	Setting these bits to '1' will cause the registers associated with that trigger to be loaded with the contents of its corresponding shadow register. Ext_Trigger[7] = Trigger_10 ... Ext_Trigger[0] = Trigger_3 Note: if the part is set for LOW POWER, writes to this register are ignored.	W	B/G	No

Bus #2 Reg56 (0x38) – EXT_TRIG_CNT3 (Extended Trigger 3 Timer Count)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	EXT_TRIG_CNT3	8b0000_0000	Writing a non-zero value to this register loads the 8 msb of the 9-bit trigger timer. The timer decrements on every SCLK and the trigger is asserted when the timer hits 0.	R/W	B/G	No

Bus #2 Reg57 (0x39) – EXT_TRIG_CNT4 (Extended Trigger 4 Timer Count)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	EXT_TRIG_CNT4	8b0000_0000	Writing a non-zero value to this register loads the 8 msb of the 9-bit trigger timer. The timer decrements on every SCLK and the trigger is asserted when the timer hits 0.	R/W	B/G	No

Bus #2 Reg58 (0x3A) – EXT_TRIG_CNT5 (Extended Trigger 5 Timer Count)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	EXT_TRIG_CNT5	8b0000_0000	Writing a non-zero value to this register loads the 8 msb of the 9-bit trigger timer. The timer decrements on every SCLK and the trigger is asserted when the timer hits 0.	R/W	B/G	No

Bus #2 Reg59 (0x3B) – EXT_TRIG_CNT6 (Extended Trigger 6 Timer Count)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	EXT_TRIG_CNT6	8b0000_0000	Writing a non-zero value to this register loads the 8 msb of the 9-bit trigger timer. The timer decrements on every SCLK and the trigger is asserted when the timer hits 0.	R/W	B/G	No

Bus #2 Reg60 (0x3C) – EXT_TRIG_CNT7 (Extended Trigger 7 Timer Count)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	EXT_TRIG_CNT7	8b0000_0000	Writing a non-zero value to this register loads the 8 msb of the 9-bit trigger timer. The timer decrements on every SCLK and the trigger is asserted when the timer hits 0.	R/W	B/G	No

Bus #2 Reg61 (0x3D) – EXT_TRIG_CNT8 (Extended Trigger 8 Timer Count)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	EXT_TRIG_CNT8	8b0000_0000	Writing a non-zero value to this register loads the 8 msb of the 9-bit trigger timer. The timer decrements on every SCLK and the trigger is asserted when the timer hits 0.	R/W	B/G	No

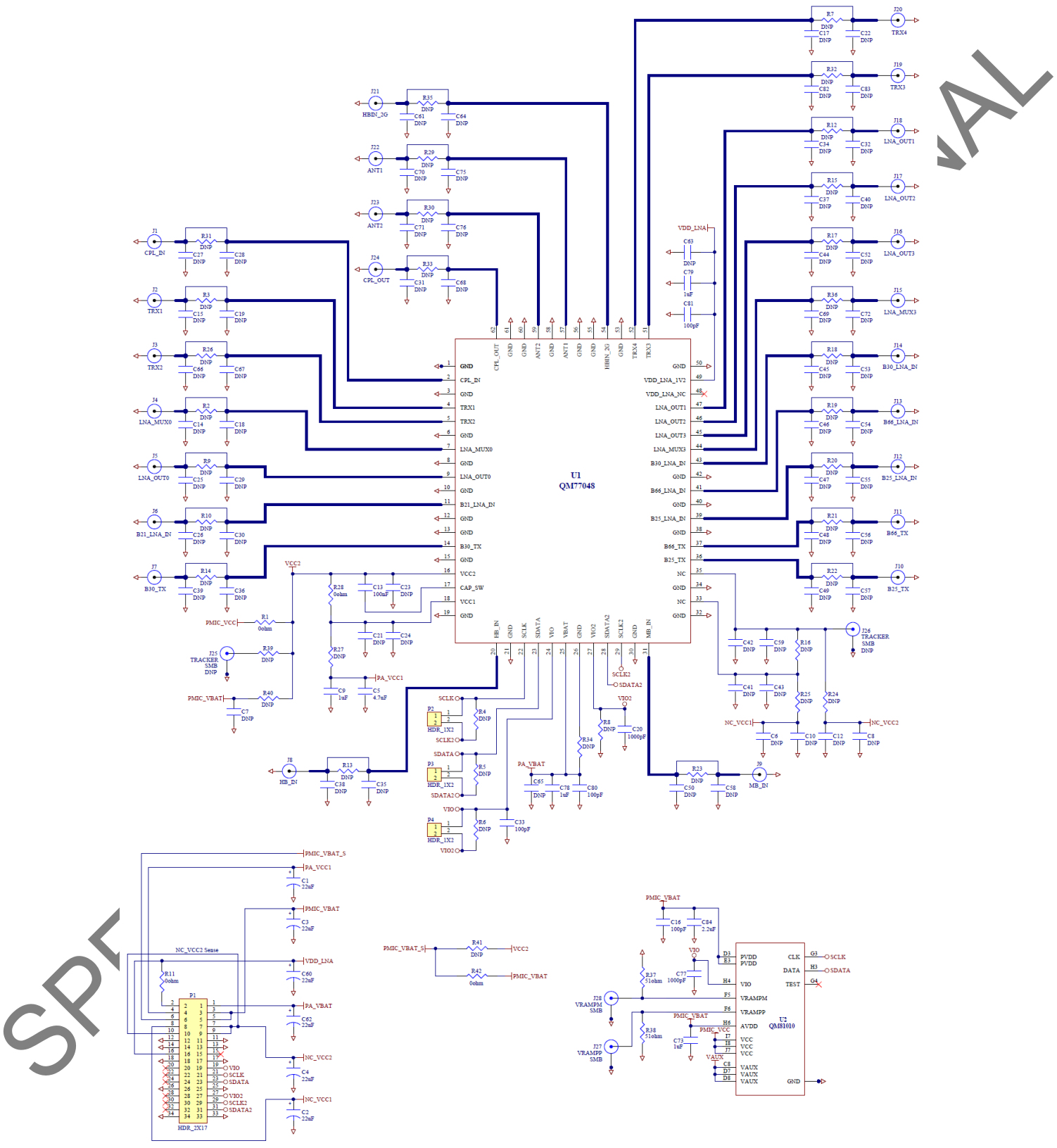
Bus #2 Reg62 (0x3E) – EXT_TRIG_CNT9 (Extended Trigger 9 Timer Count)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	EXT_TRIG_CNT9	8b0000_0000	Writing a non-zero value to this register loads the 8 msb of the 9-bit trigger timer. The timer decrements on every SCLK and the trigger is asserted when the timer hits 0.	R/W	B/G	No

Bus #2 Reg63 (0x3F) – EXT_TRIG_CNT10 (Extended Trigger 10 Timer Count)

Bit(s)	Field Name	Default	Description	R/W	B/G/M	Trig
7:0	EXT_TRIG_CNT10	8b0000_0000	Writing a non-zero value to this register loads the 8 msb of the 9-bit trigger timer. The timer decrements on every SCLK and the trigger is asserted when the timer hits 0.	R/W	B/G	No

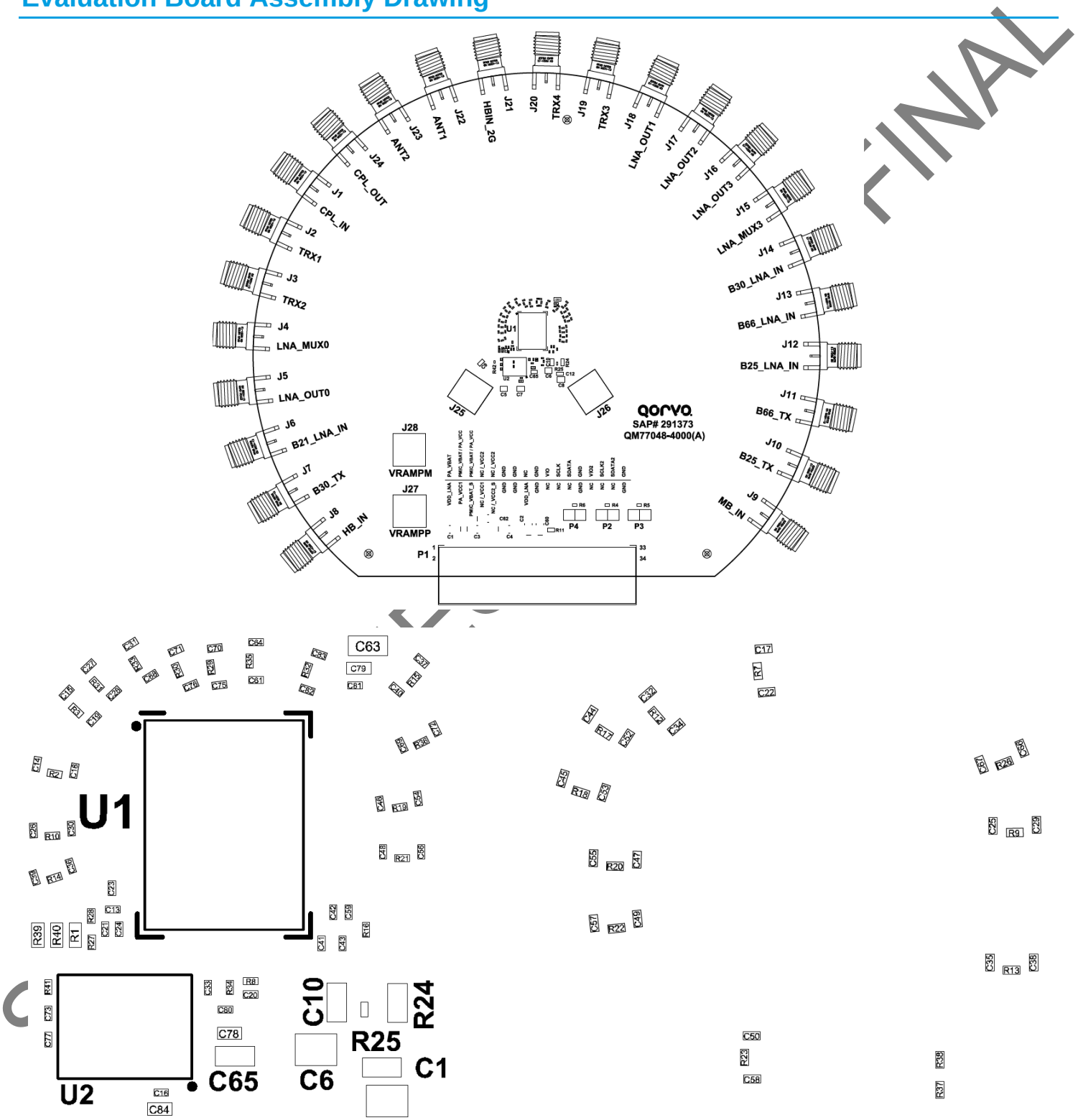
Evaluation Board Schematic



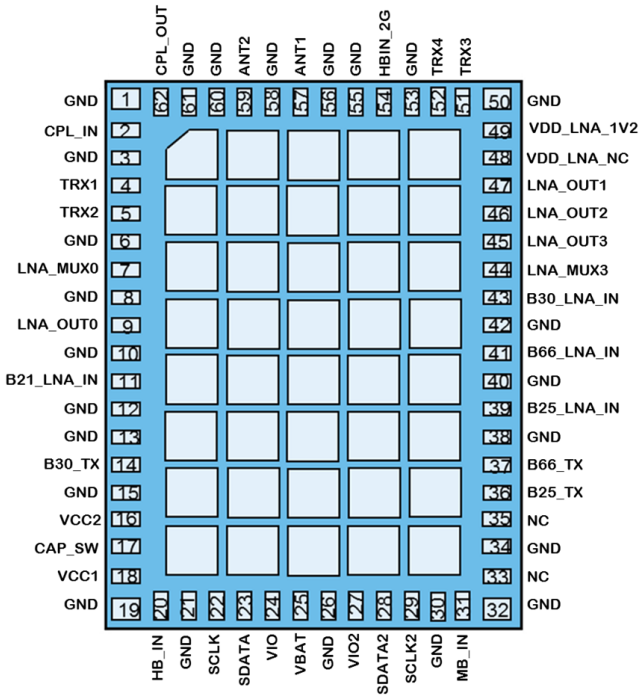
Application Circuit Schematic

TBD (Refer to Evaluation Board Schematic)

Evaluation Board Assembly Drawing



Pin Configuration and Description



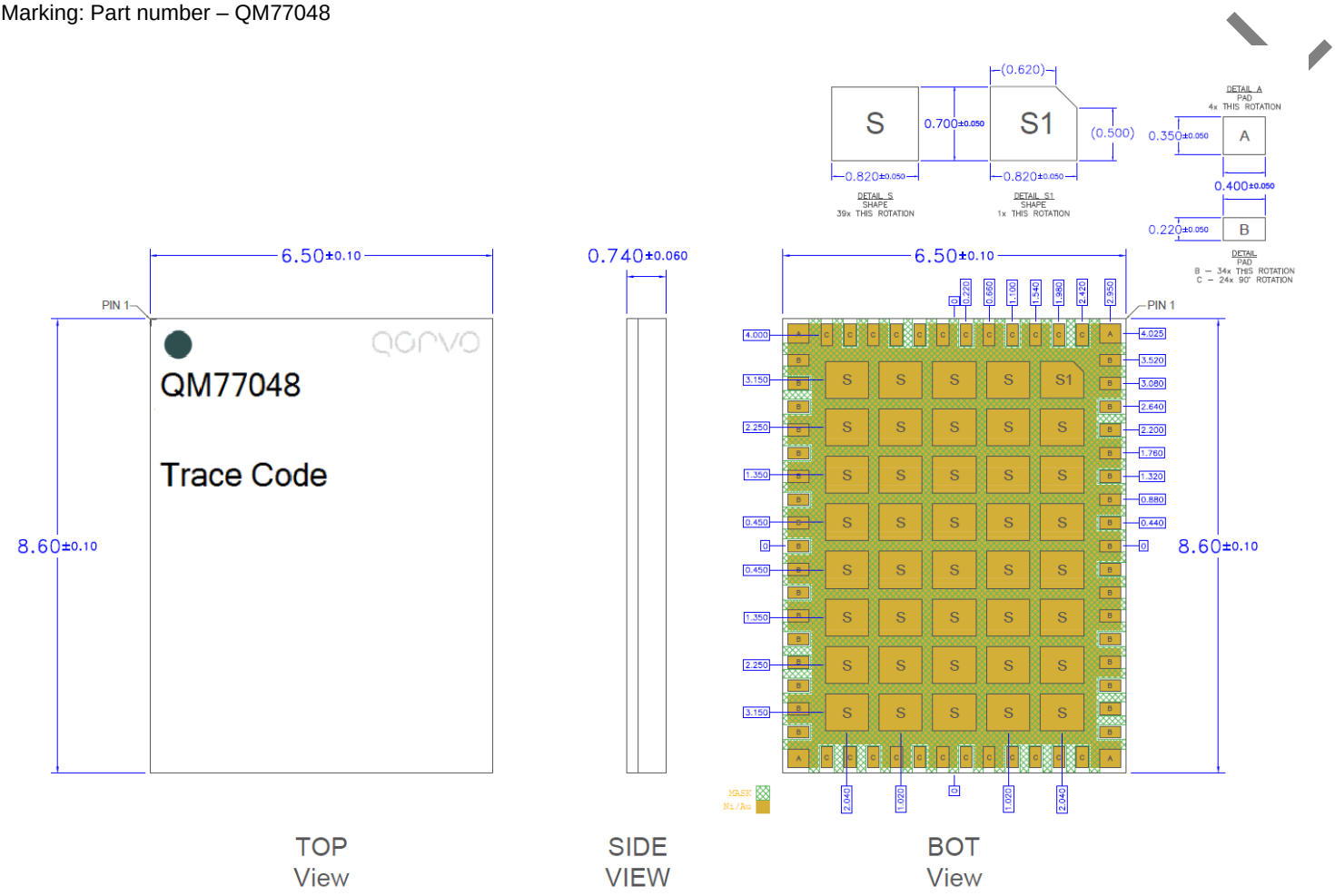
Top View

PIN NUMBER	LABEL	DESCRIPTION
Multiple, see description for full list.	GND	1,3,6,8,10,12,13,15,19,21,26,30,32,34,38,40,42,50,53,55,56,58,60,61. These pins are connected to main module ground and will be grounded on the PCB for best RF performance.
Backside Pad	GND	Ground connection. The back side of the package should be connected to the ground plane through as short of a connection as possible. PCB vias under the device are required.
2	CPL IN	Input port to support applications that use daisy chain connected couplers.
4	TRX1	Auxiliary RF input / output to antenna switch.
5	TRX2	Auxiliary RF input / output to antenna switch – lower loss path.
7	LNA MUX0	Input port to route external LNA signal through LNA OUT0.
9	LNA OUT0	Internal LNA output. Switches connect this port to any one of the four internal LNAs or to LNA MUX0.
11	B21 LNA IN	Input port to route external Band 21 receive signal through the LNA.
14	B30 TX	High band power amplifier auxiliary output from distribution switch. Not DC blocked.
16	VCC2	DC supply for high band power amplifier output stage. Internal capacitance 102pF.
17	CAP SW	Input to FET switch controlled by RFFE programming. Connect to GND side of VCC decoupling capacitor. Do Not connect to GND!
18	VCC1	DC supply for high band power amplifier driver stage. Internal capacitance 136pF.
20	HB IN	RF input to the high band power amplifier. Internal shunt inductor to GND.
22	SCLK	Serial interface clock input signal for programming the MIPI RFFE bus #1 (PA and switches).
23	SDATA	Serial interface data I/O signal for programming the MIPI RFFE bus #1 (PA and switches).
24	VIO	DC supply voltage for the MIPI RFFE serial interface bus #1 (PA and switches).
25	VBAT	DC supply for RF switches and amplifier bias circuitry.
27	VIO2	DC supply voltage for the MIPI RFFE serial interface bus #2 (LNA).
28	SDATA2	Serial interface data I/O signal for programming the MIPI RFFE bus #2 (LNA).
29	SCLK2	Serial interface clock input signal for programming the MIPI RFFE bus #2 (LNA).
31	MB IN	RF input to the mid band power amplifier.
33	NC	Not connected internally.
35	NC	Not connected internally.
36	B25 TX	Mid band power amplifier auxiliary output from distribution switch. Not DC blocked.
37	B66 TX	Mid band power amplifier auxiliary output from distribution switch. Not DC blocked.
39	B25 LNA IN	Input port to route external Band 2 or 25 receive signal through the LNA.
41	B66 LNA IN	Input port to route external Band 66 receive signal through the LNA.
43	B30 LNA IN	Input port to route external Band 30 receive signal through the LNA.
44	LNA MUX3	Input port to route external LNA signal through LNA OUT3.
45	LNA OUT3	Internal LNA output. Switches connect this port to any one of the four internal LNAs or to LNA MUX3.
46	LNA OUT2	Internal LNA output. Switches connect this port to any one of the four internal LNAs.
47	LNA OUT1	Internal LNA output. Switches connect this port to any one of the four internal LNAs.
48	NC	Not connected internally.
49	VDD_LNA	DC supply for LNA circuitry. Nominal voltage 1.2V.
51	TRX3	Auxiliary RF input / output to antenna switch. Not DC blocked.
52	TRX4	Auxiliary RF input / output to antenna switch. Not DC blocked.
54	2G HB IN	Input port to route 2G HB signal through the antenna switch.
57	ANT1	Antenna 1 bidirectional RF port. An inductor makes this port appear as a DC short to ground.
59	ANT2	Antenna 2 bidirectional RF port. An inductor makes this port appear as a DC short to ground.
62	CPL OUT	Coupler output, selectable from ANT1 or ANT2.

Mechanical Information

Package Marking and Dimensions

Marking: Part number – QM77048



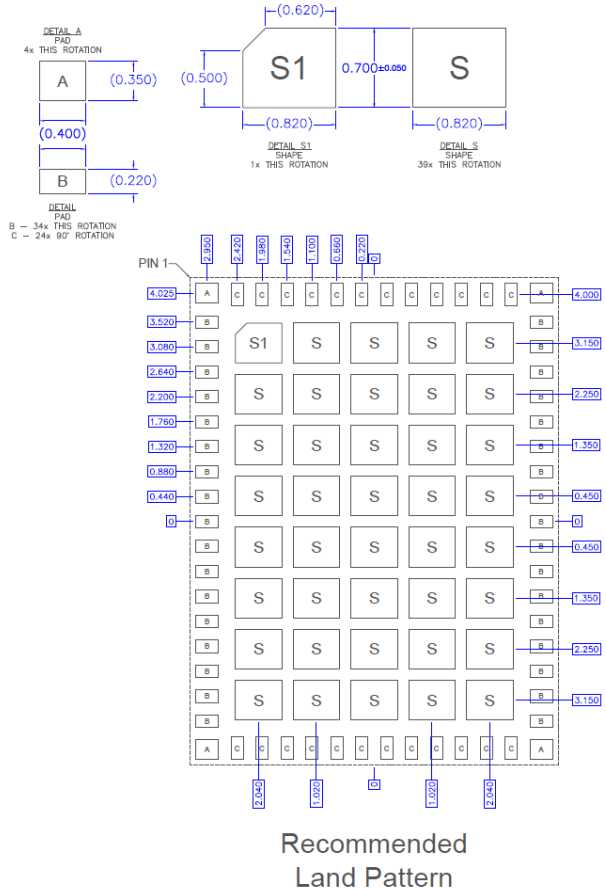
TOP View

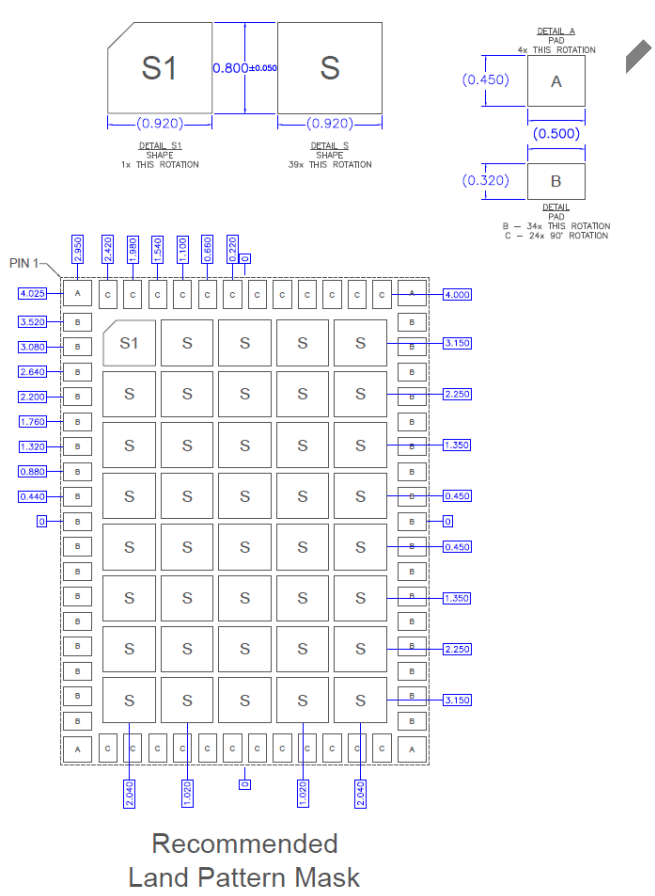
SIDE VIEW

BOT View

PCB Design Guidelines

PCB Metal Land and Solder Mask Pattern





Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Handling Precautions

PARAMETER	RATING	STANDARD
ESD – Human Body Model (HBM)	Class 1C (1000V)	ESDA/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3 (1000V)	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	TBD	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following ** *preliminary* ** attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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REVISION HISTORY

Revision	Date	Description
REV A	08/07/2019	Initial Preliminary (Brief) Release. Information is subject to change!
REV B	1/22/2020	General updates and corrections. Add draft data tables (performance varies with sample maturity). Update LNA register map to align with Engineering Samples.
REV C	04/04/2020	RFFE bus information corrected to show support for MIPI RFFE v3.0. Correction to Bus#1 Reg00 PA_MODE. Update Register map for ES2 samples. Add evaluation board schematic, and block diagram. Update specification values and operating conditions.
REV D	04/15/2020	Corrections to descriptions of LNA registers and Enable bits.
REV E	07/15/2020	Updated Ordering Information. Changed B41 GS0 NF from 5.9 to 5.2.