

 AAC AAC ACOUSTIC TECHNOLOGIES (SHENZHEN) CO., LTD.		ISSUE: X10
PART No. SDM0502B-FDS371-M02	Remark: GP compliant	DATE: Nov.28 th . 2024

APPROVAL SHEET FOR MICROPHONE

CUSTOMER: _____

CHECKER: _____ Zeng Peng _____

APPROVER: _____ Wu Zhijiang _____

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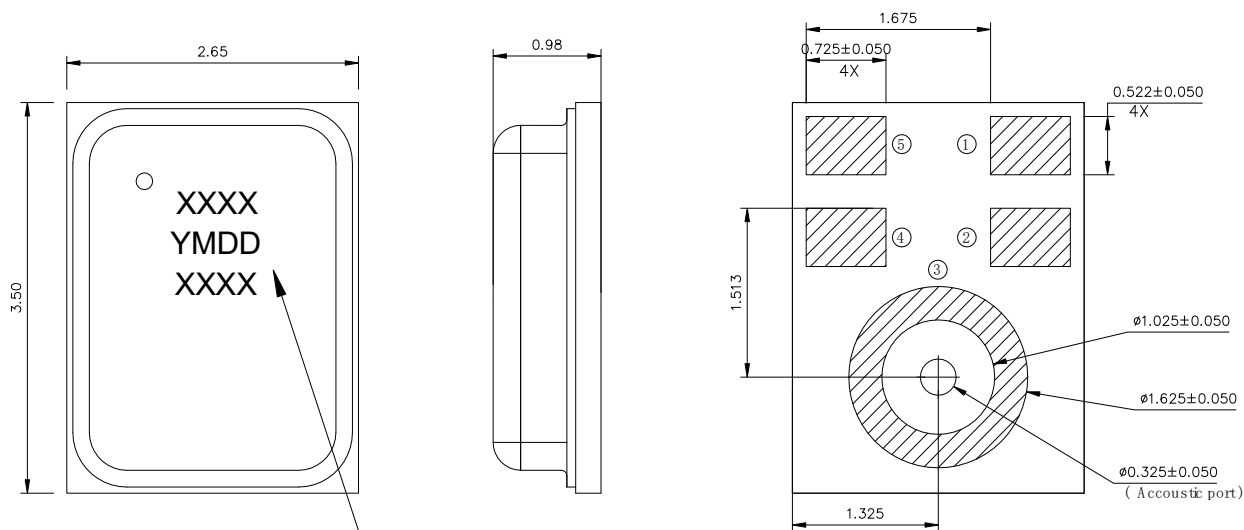
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1. Mechanical Layout and Dimensions



Y	Year, 1 number, 0~9 stand for 2010~2019
M	Month, 1 number, 1~9,A,B,C
DD	Date, 2 numbers, 01~31

Pin description

No.	Name	Description
1	Data	PDM data output from the microphone
2	L/R	Left/Right(DATA2/DATA1) channel selection
3	Ground	Ground
4	Clock	Clock input to the microphone
5	Power	Supply and IO voltage for the microphone

Product size

Item	Dim.	Tol.(+/-)	Unit
Length	3.50	0.10	mm
Width	2.65	0.10	mm
Height	0.98	0.10	mm
Port Hole	0.325	0.05	mm

Note: Tolerance +/-0.15mm unless otherwise specified

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2. Product Specifications:

Unless otherwise specified, test conditions are:

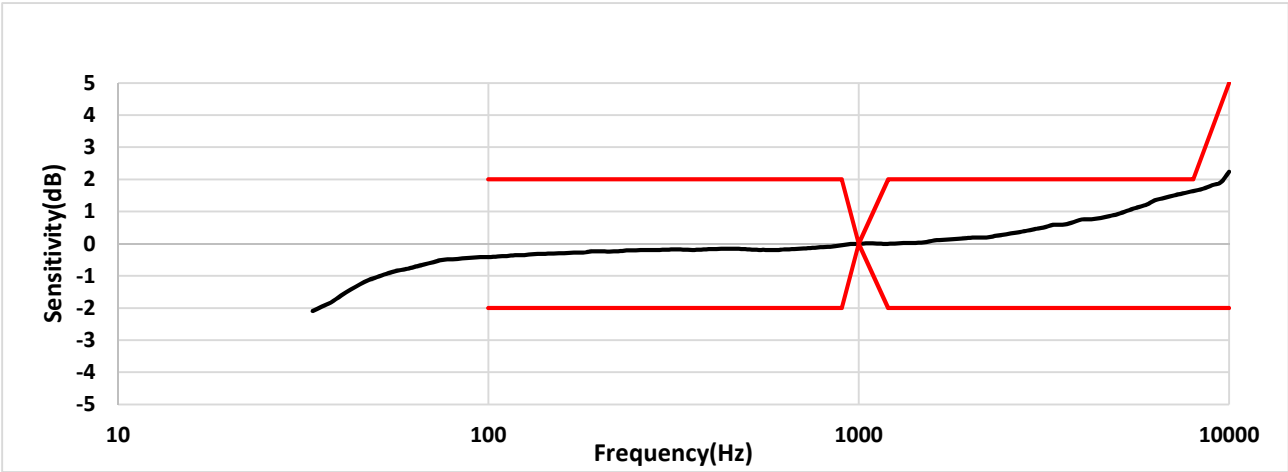
- Vdd = 1.8V
- Duty cycle = 50%
- F_{IN} = 1 kHz @ 94dB SPL
- Ta = 27°C, Room Humidity = 50%

SNR & noise measurement is based on 20-20kHz pass band with A-weighting filter applied

Items	Symbol	Condition	Limits			Unit
			Min.	Typ.	Max.	
ELECTRICAL CHARACTERISTICS						
2.1 Directivity		Omni-Directional				
2.2 Supply Voltage	V _{dd}		1.64	1.8	3.6	V
2.3 Clock Frequency	F _{clk}	Standard Performance Mode	1.45	2.4	4.8	MHz
		Low Power Mode	500	750	1100	KHz
		Sleep Mode			250	KHz
2.4 Duty Cycle			40	50	60	%
2.5 Clock rise/fall time	Tr/Tf	10%-90%			60	ns
2.6 Logic high IO Voltage	V _{IOH}		0.65*V _{dd}		V _{dd} +0.3	V
2.7 Logic Low IO Voltage	V _{IOL}		-0.3		0.35*V _{dd}	V
2.8 Sleep Current	I _{sleep}				50	uA
2.9 Short Circuit Current		Maximum logic output current	1		20	mA
2.10 Load Capacitance					150	pF
2.11 Delay Time for Data Driven	t _A		40		80	ns
2.12 Delay Time for High-Z	t _B				24	ns
2.13 Wake-up Time					35	ms
2.14 Fall-asleep Time	t _{FSL}				10	ms
2.15 Polarity	Increase Sound Pressure		Increase 1's density			

Standard Performance Mode(F _{clk} =2.4MHz, Vdd=1.8V)						
2.16 Sensitivity	S	1kHz, 94dB SPL	-38	-37	-36	dBFS
2.17 Signal-to-Noise Ratio	SNR	A-weighting at 1kHz 1Pa		65.5		dB(A)
2.18 Total Harmonic Distortion	THD	94dB SPL@1kHz		0.2	0.5	%
	THD	1% THD@1kHz	128	130		dBSPPL
2.19 Power Supply Rejection Ratio	PSRR	200 mVpp sinewave @ 1 kHz		87		dB V/FS
2.20 Power Supply Rejection	PSR+N	200 mVpp 7/8 duty cycle rectangular waveform @ 217 Hz, A-weighted, BW = 20kHz		-97		dBFS(A)
2.21 Acoustic Overload Point	AOP	1kHz THD @ 10%	130.5	132.5		dBSPPL
2.22 Current Consumption	I _s			670		μA

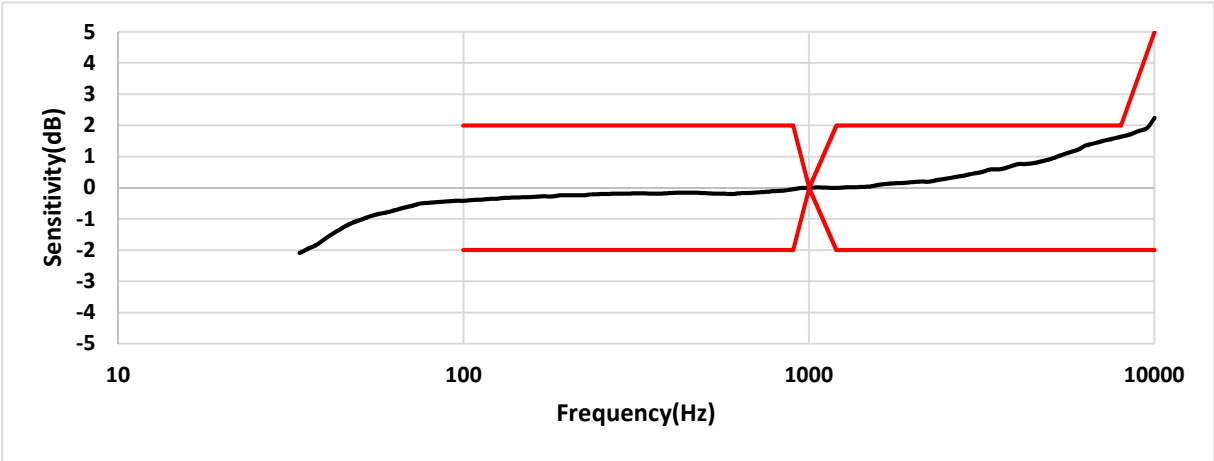
2.23 Frequency Response Limits



Frequency(Hz)	100	200	900	1000	1200	5000	8000	10000
Upper Limit(dB)	2	2	2	0	2	2	2	5
Lower Limit(dB)	-2	-2	-2	0	-2	-2	-2	-2

Low Power Mode($F_{clk}=768kHz$, $V_{dd}=1.8V$)						
2.24 Sensitivity	S	1kHz, 94dB SPL	-22	-21	-20	dBFS
2.25 Signal-to-Noise Ratio	SNR	A-weighting at 1kHz 1Pa	62.5	64.5		dB(A)
2.26 Total Harmonic Distortion	THD	1KHz, 94dB SPL		0.2	0.5	%
		1% THD@1kHz	111	113		dB SPL
2.27 Power Supply Rejection Ratio	PSRR	200 mVpp sinewave @ 1 kHz		76		dB V/FS
2.28 Power Supply Rejection	PSR+N	200 mVpp 7/8 duty cycle rectangular waveform @ 217 Hz, A-weighted, BW = 20kHz		-85		dBFS(A)
2.29 Acoustic Overload Point	AOP	1kHz THD @ 10%	114.5	116		dB SPL
2.30 Current Consumption	I_s			250		uA

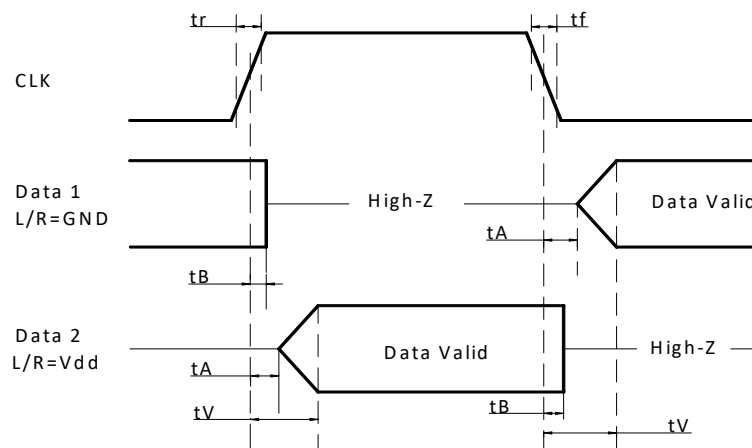
2.31 Frequency Response Limits



Frequency(Hz)	100	200	900	1000	1200	5000	8000	10000
Upper Limit(dB)	2	2	2	0	2	2	2	5
Lower Limit(dB)	-2	-2	-2	0	-2	-2	-2	-2

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2.32 Timing Diagram



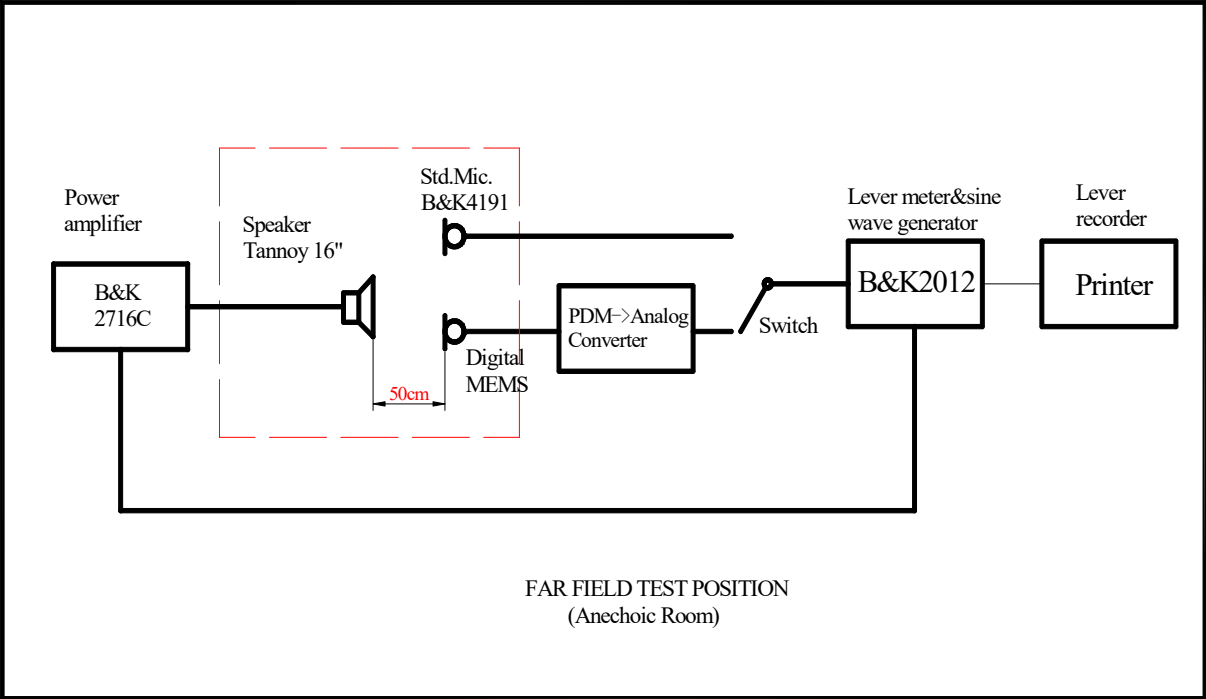
Label	L/R	Drives Data After	High-Z After
Data 1	Low (L)	Falling Clock Edge	Rising Clock Edge
Data 2	High (H)	Rising Clock Edge	Falling Clock Edge

ENVIRONMENTAL CHARACTERISTICS

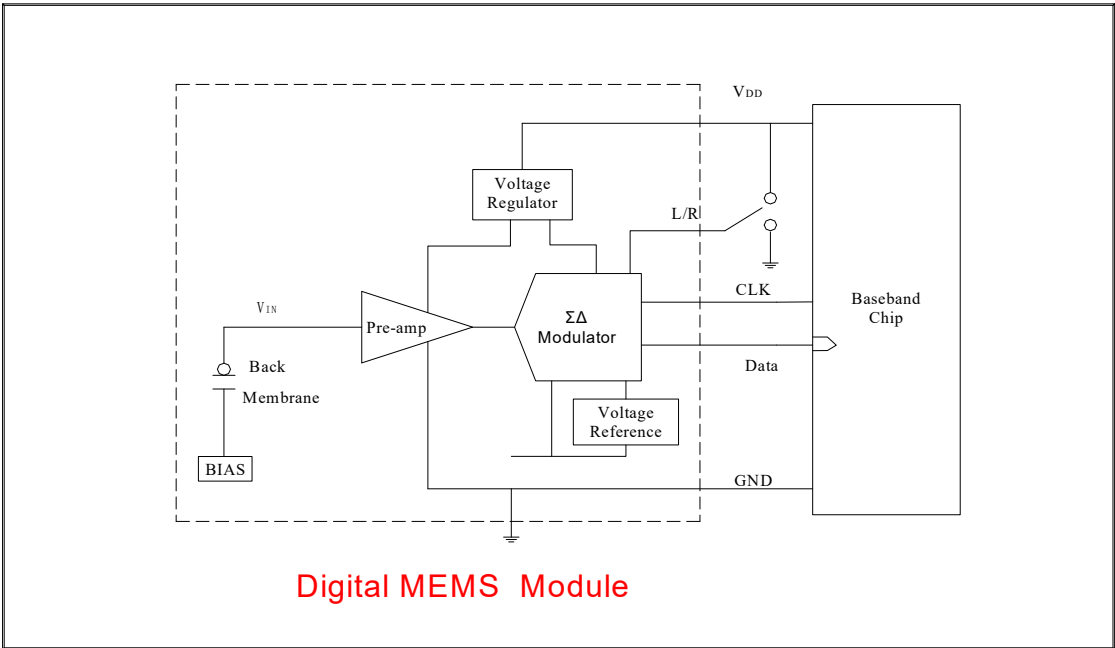
2.33 Operating Temperature			-30		+70	°C
2.34 Storage Temperature		Soldered onto PC Board	-40		+85	°C
		In Tape/Reel's	-10		+50	°C
2.35 Relative Humidity			25		85	%
2.36 Air Pressure			860		1060	mBar

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3. Test Setup



4. Recommended Interface Circuit



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5. Reliability Specifications

As per customer's requirements. If no customer's requirements available please refer to following tests.

Test item	Detail	Standard
Reflow Simulation	Refer to 7. solder reflow profile, total 3 times	/
Low Temperature	Conditions: -40±3℃ Duration: 72 hours	IEC60068-2-1
High Temperature	Conditions: 85±3℃ Duration: 72 hours	IEC60068-2-2
Temperature Shock	Conditions: 30 minutes at -40 °C followed by 30 minutes at 85 °C ,20 second maximum transition time between temperature extremes.32 cycles	EC60068-2-14
Vibration Test	Conditions: 10~60Hz: 0.35mm 60~500Hz: 5g 1 oct/min Duration: 15 minutes per plane.	IEC60068-2-6
Damp heat	Conditions: 55±3℃ 93%RH Duration: 96 hours	IEC60068-2-56
Drop Test	Conditions:1.5 Meter height onto a concrete surface each time at three direction in state of 150g weight packing	IEC60068-2-32
ESD	Conditions: 3 discharges at +/-8kV, 150pF, 330Ω direct contact to housing and per MIL-883F, method 3015.7, 3 discharges at +/-2kV direct contact to all pins	IEC61000-4-2

The measurement shall to be done after 2 hours of conditioning at room temperature.

The sensitivity change within ±3dBFS relative to initial value.

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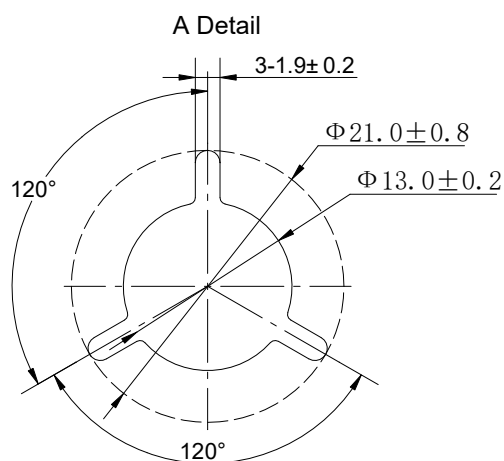
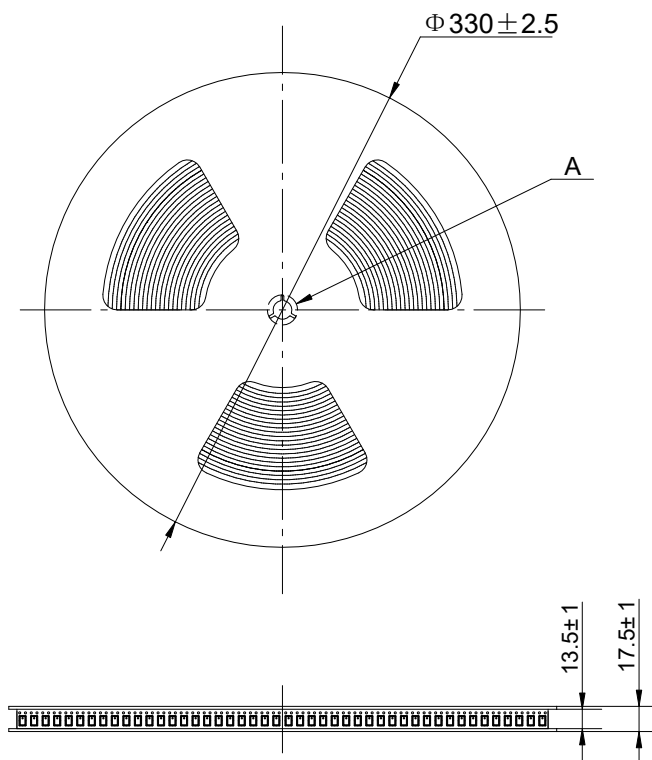
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4,500 PCS PRODUCTS/1 reel

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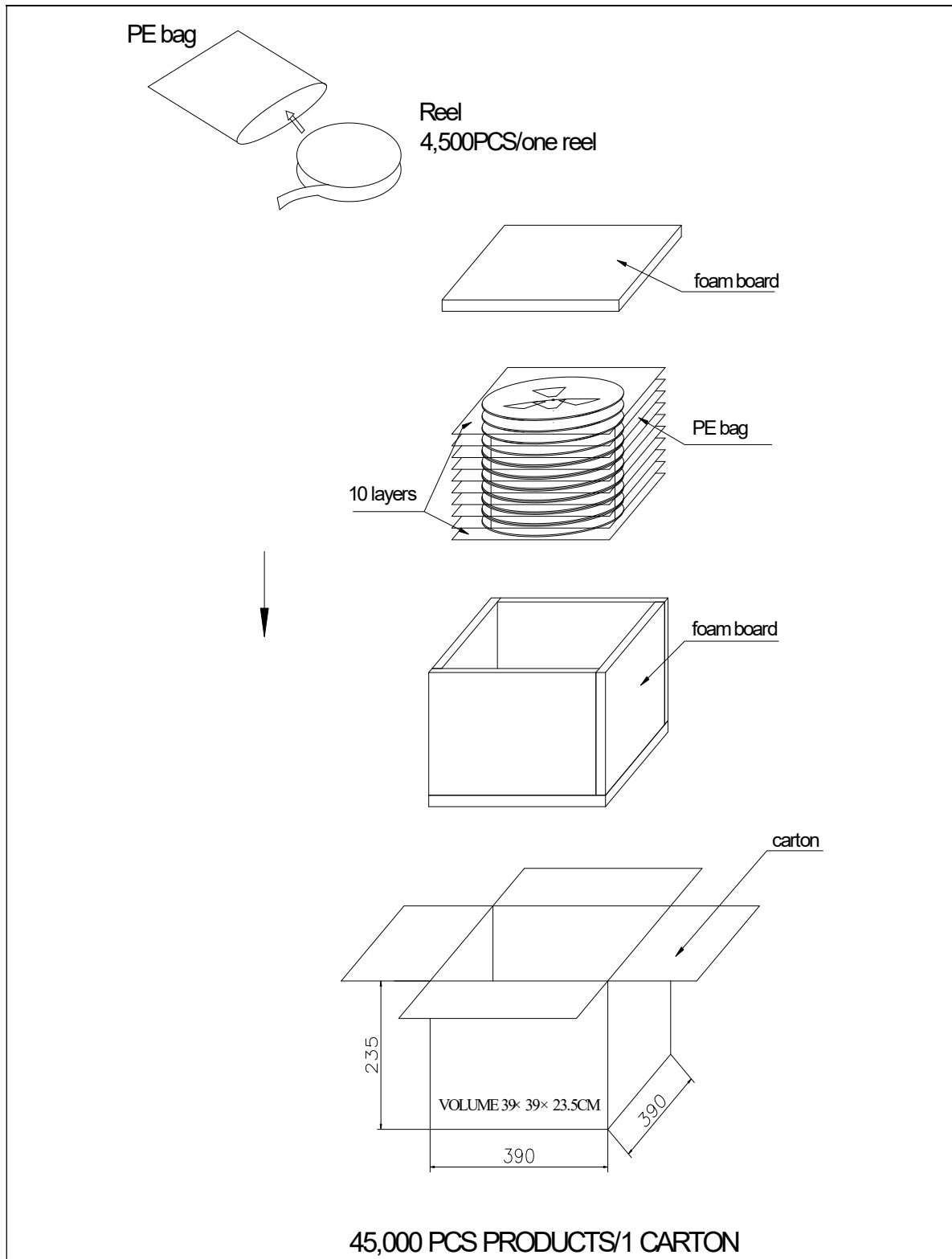
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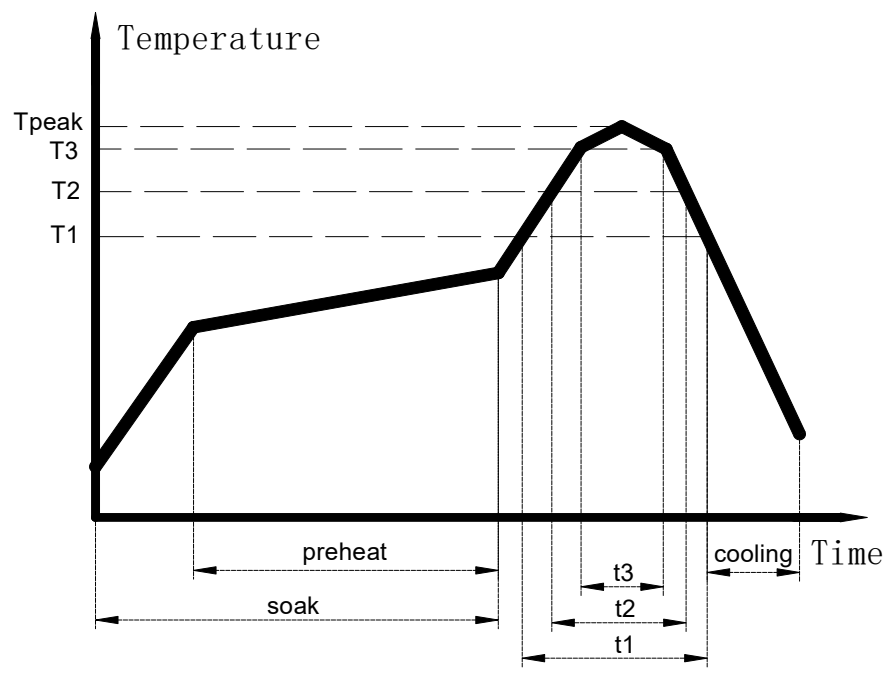
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7. Reflow Profile

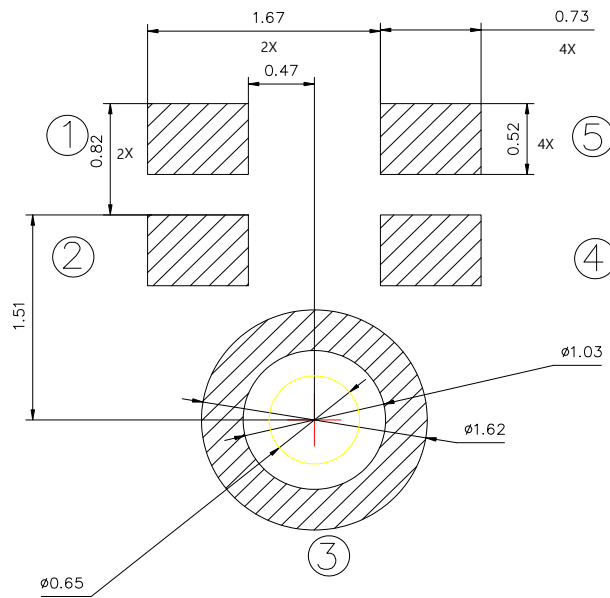


Average temperature gradient in preheating		Max 3°C/s
Preheat time	150-180°C	Max 120s
Soak time	t_{soak}	2-3 minutes
Time above 217°C	t_1	Max 90s
Time above 230°C	t_2	Max 60s
Time above 250°C	t_3	Max 30s
Peak temperature in reflow	T_{peak}	260°C(-0/+5°C)
Cooling time		Max 60s
Temperature gradient In cooling		Max -5°C/s

- Notes:**
- Pulling vacuum or blowing air over acoustical hole of the microphone is not allowed, Because the device can be damaged.
 - Wash the board after reflow process is not allowed, because board washing and cleaning agents can damage the device. Device should not be exposed to ultrasonic processing or cleaning, and air blowing.
 - Recommended number of reflow is no more than 3 times.

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8. Recommended Customer Land Pattern:



PCB through hole size

9. Specification History

ISSUE	PREP	CHKD	DETAIL SPEC CHANGES:	DATE
X1	Chen Zhiyuan	Wu Zhijiang	Initial Version Release	Jul.15 th . 2017
X2	Chen Zhiyuan	Wu Zhijiang	Update reliability spec.	Jan.5 th .2018
X3	Chen Zhiyuan	Wu Zhijiang	Update working clock range	Mar.5 th .2018
X4	Chen Zhiyuan	Wu Zhijiang	Update clock range	Jul. 3 rd .2018
X5	WangTianjiao	Wu Zhijiang	Update date code	Mar. 20 rd .2019
X6	Zeng Peng	Wu Zhijiang	Update wake-up time	May.16 th .2019
X7	Chen ZhaoPing	Wu Zhijiang	Update Frequency Response Limits in page 5,page 6.	May.25 th .2022
X8	Chen ZhaoPing	Wu Zhijiang	Update 1% THD@1kHz in page 5, Frequency Response Limits in page 5,page6	Sep.12 th .2023
X9	Chen ZhaoPing	Wu Zhijiang	Add Clock rise/fall time limit	Sep.13 th .2023
X10	Chen ZhaoPing	Wu Zhijiang	Update Clock rise/fall time limit	Nov.28 th .2024