

MOSFET – Dual, N-Channel, POWERTRENCH®

2.5 V Specified

FDS9926A

General Description

These N-Channel 2.5 V specified MOSFETs use onsemi's advanced POWERTRENCH process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5 V – 10 V).

Features

- 6.5 A, 20 V. $R_{DS(ON)} = 30\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
 $R_{DS(ON)} = 43\text{ m}\Omega @ V_{GS} = 2.5\text{ V}$
- Optimized for Use in Battery Protection Circuits
- Low Gate Charge
- This Device is Pb-Free and Halide Free

Applications

- Battery Protection
- Load Switch
- Power Management

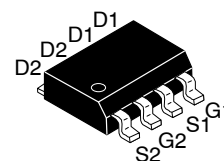
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 10	V
I_D	Drain Current	Continuous (Note 1a)	6.5
		Pulsed	20
P_D	Power Dissipation	for Dual Operation	2
		for Single Operation (Note 1a)	1.6
		(Note 1b)	1
		(Note 1c)	0.9
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

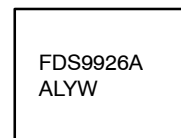
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	40	$^\circ\text{C/W}$



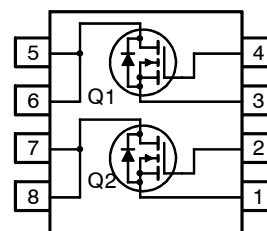
SOIC8
CASE 751EB

MARKING DIAGRAM



FDS9926A = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

ELECTRICAL CONNECTION



ORDERING INFORMATION

Device	Package	Shipping†
FDS9926A	SOIC8	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDS9926A

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	–	14	–	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$	–	–	1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 8\text{ V}, V_{DS} = 0\text{ V}$	–	–	± 100	nA

ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6	1	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	–	–3	–	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 6.5\text{ A}$	–	25	30	m Ω
		$V_{GS} = 2.5\text{ V}, I_D = 5.4\text{ A}$	–	35	43	
		$V_{GS} = 4.5\text{ V}, I_D = 6.5\text{ A}, T_J = 125^\circ\text{C}$	–	35	50	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ A}$	15	–	–	A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 6.5\text{ A}$	–	22	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	650	–	pF
C_{oss}	Output Capacitance		–	150	–	pF
C_{rss}	Reverse Transfer Capacitance		–	85	–	pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$	–	1.4	–	Ω

SWITCHING CHARACTERISTICS (Note 2)

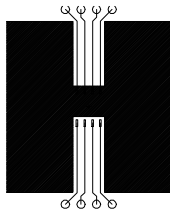
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A}, V_{GS} = 4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$	–	8	16	ns
t_r	Turn-On Rise Time		–	9	17	ns
$t_{d(off)}$	Turn-Off Delay Time		–	15	26	ns
t_f	Turn-Off Fall Time		–	4	9	ns
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 3\text{ A}, V_{GS} = 4.5\text{ V}$	–	6.2	9	nC
Q_{gs}	Gate-Source Charge		–	1.2	–	nC
Q_{gd}	Gate-Drain Charge		–	1.7	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

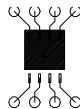
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)	–	0.73	1.3	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 6.5\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$	–	15	–	ns
Q_{rr}	Diode Reverse Recovery Charge		–	5	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

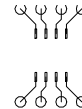
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $78^\circ\text{C}/\text{W}$ when mounted on a 0.5 in^2 pad of 2 oz. Copper



b) $125^\circ\text{C}/\text{W}$ when mounted on a 0.02 in^2 pad of 2 oz. copper



c) $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

- Pulse Test Pulse Width $< 300\text{ }\mu\text{s}$, Duty Cycle $< 2.0\%$

TYPICAL CHARACTERISTICS

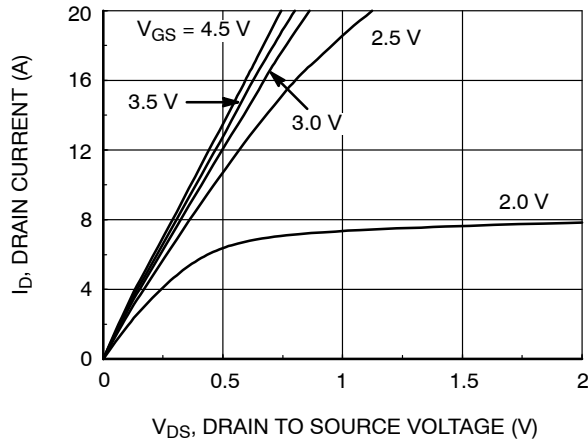


Figure 1. On-Region Characteristics

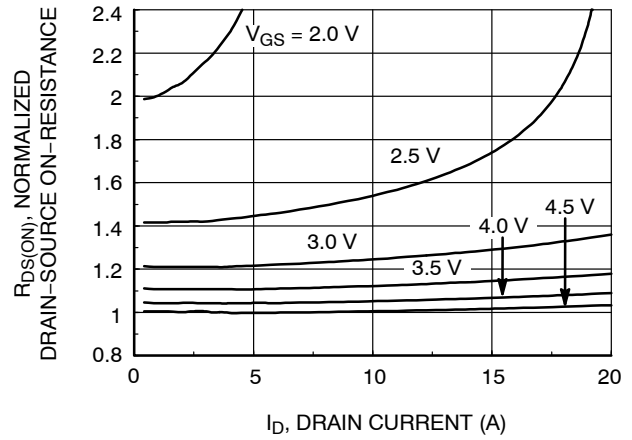


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

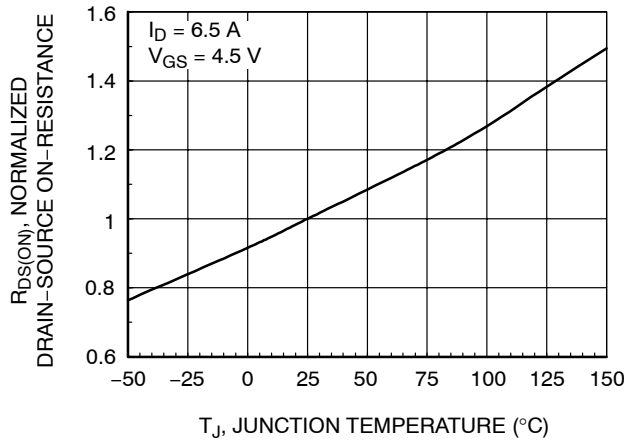


Figure 3. On-Resistance Variation with Temperature

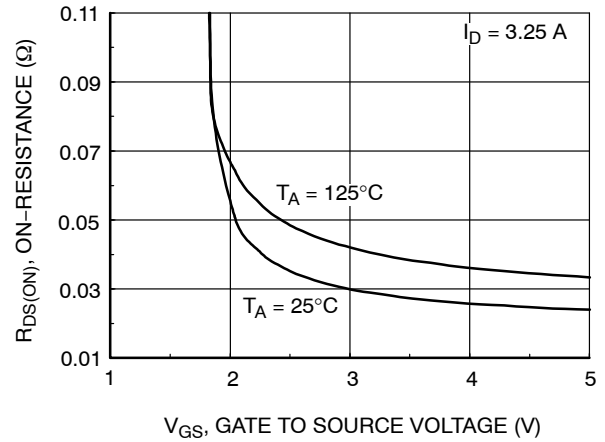


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

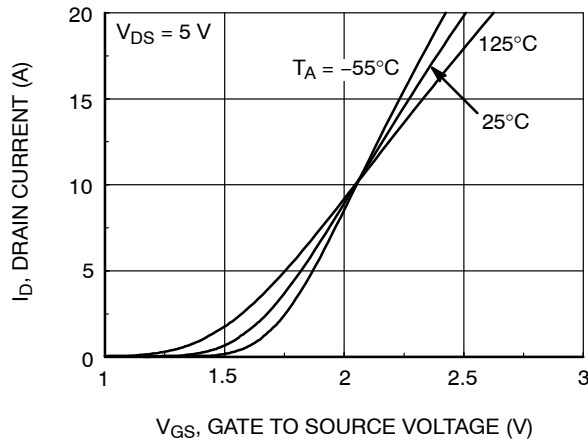


Figure 5. Transfer Characteristics

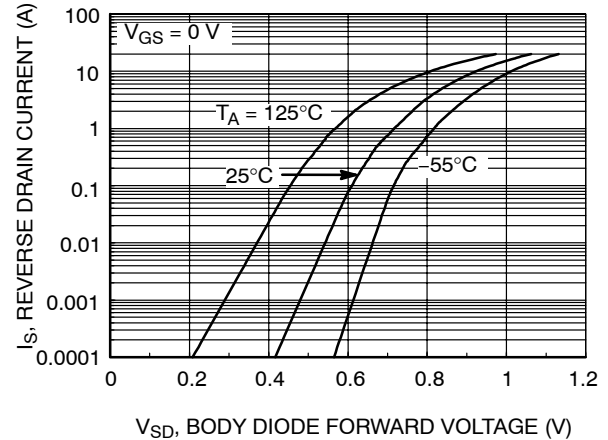


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

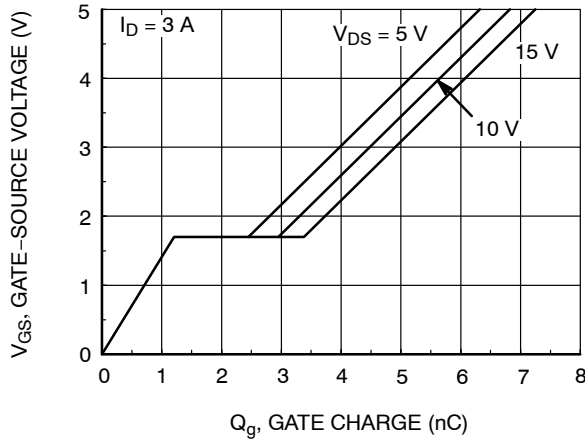


Figure 7. Gate-Charge Characteristics

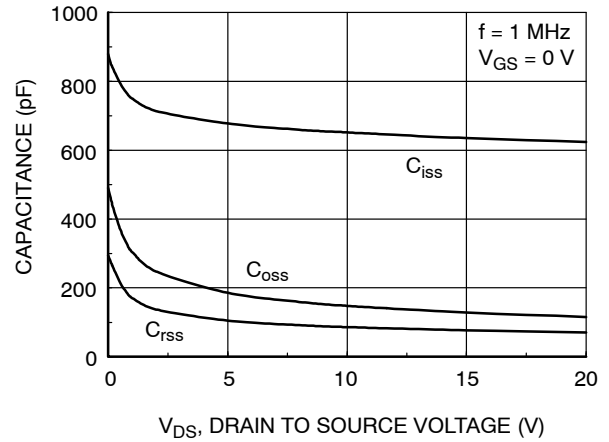


Figure 8. Capacitance Characteristics

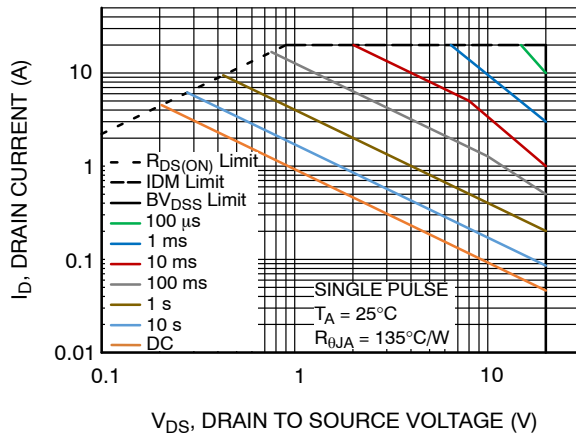


Figure 9. Maximum Safe Operating Area

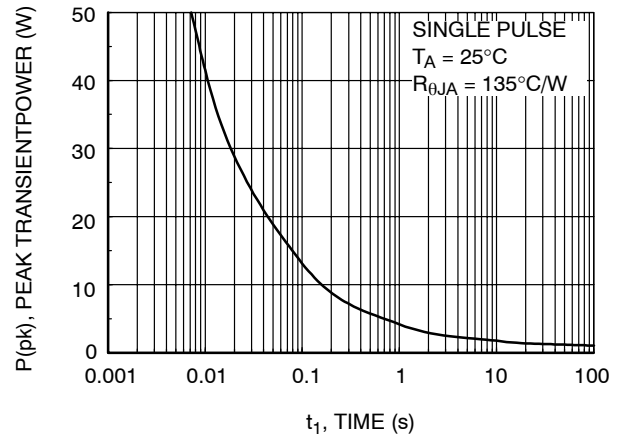


Figure 10. Single Pulse Maximum Power Dissipation

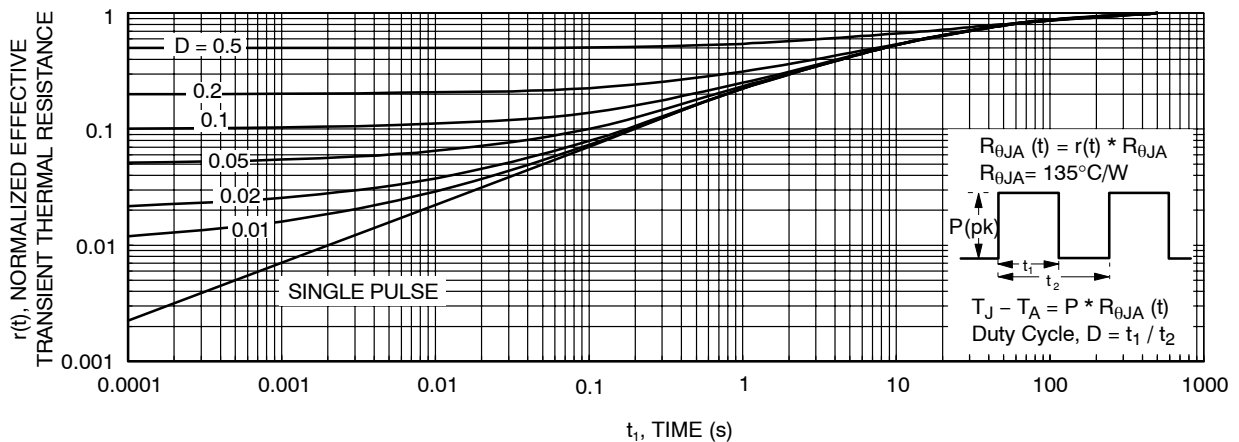


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

MECHANICAL CASE OUTLINE

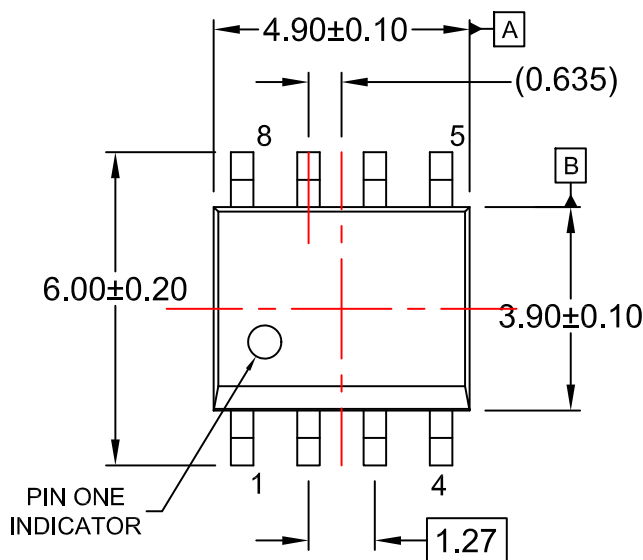
PACKAGE DIMENSIONS

ON Semiconductor®

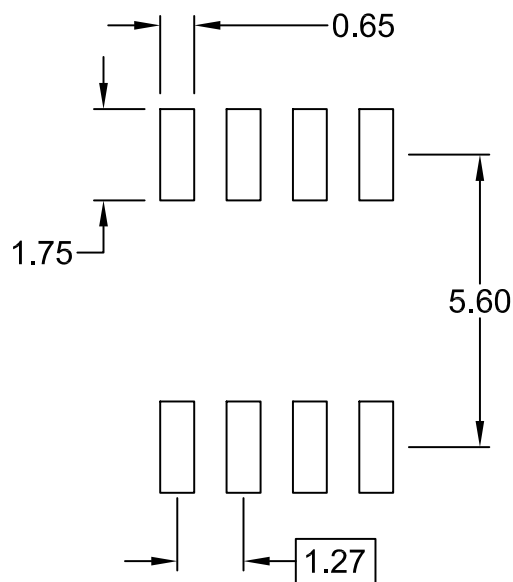


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CASE 751EB
ISSUE A

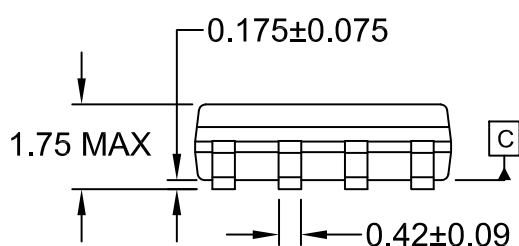
DATE 24 AUG 2017



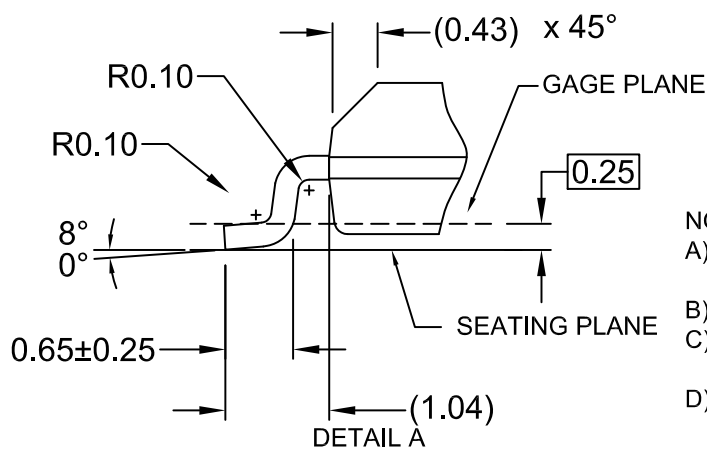
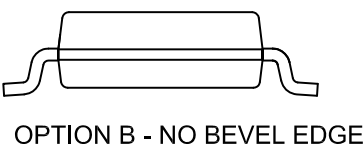
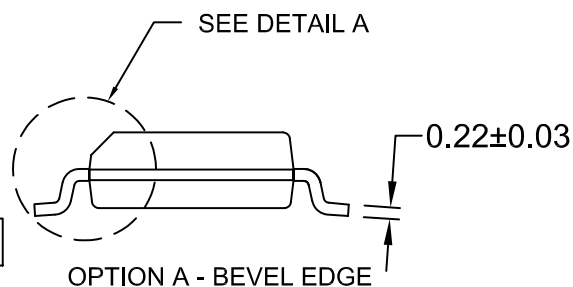
⌀ 0.25 (M) C B A



LAND PATTERN RECOMMENDATION



0.10



SCALE: 2:1

NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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