DESCRIPTION

The GLF7210x product family is an advanced technology fully integrated I_QSmart™ load switch device with reverse current blocking (RCB) protection and slew rate control of the output voltage.

The GLF7210x product family offers industry leading reverse current blocking (RCB) protection performance, featuring an ultra-low threshold voltage. The GLF7210x product family minimizes reverse current flow in the event that the VOUT voltage exceeds the VIN voltage.

The GLF7210x product family has an industry leading power efficiency. The GLF7210x product family features an on-resistance (R_{ON}) as low as 37 mΩ typical at 5.5 V, reducing power loss during conduction. The GLF7210x product family also features ultra-low shutdown current (I_{SD}) to reduce power loss and battery drain in the off state. When EN is pulled low, and the output is grounded, the GLF7210x product family can achieve an I_{SD} as low as 20 nA typical at 5.5 V.

The GLF7210x product family of load switch device supports an industry leading wide input voltage range that helps to improve system operating life and overall performance. One GLF7210x device can be used in multiple voltage rail applications which helps mitigate inventory management and reduces BOM cost.

The GLF7210x product family utilizes a chip scale package with 4 bumps in a 0.77 mm x 0.77 mm x 0.46 mm die size and a 0.4 mm pitch.

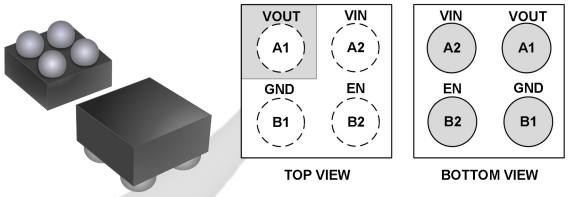
FEATURES

- Wide Input Range: 1.5 V to 5.5 V
  6 V_{abs} max
- Ultra-Low I_Q: 0.45 µA Typ at 5.5 V_{IN}
- Ultra-Low I_{SD}: 20 nA Typ at 5.5 V_{IN}
- Low R_{ON}: 37 mΩ Typ at 5.5 V_{IN}
- I_{OUT} Max: 2 A
- Reverse Current Blocking Protection
- Controlled V_{OUT} Rise Time
- Internal EN Pull-up/down Resistor on EN Pin
- Integrated Output Discharge Switch:
  GLF72101, GLF72103, GLF72105

APPLICATIONS

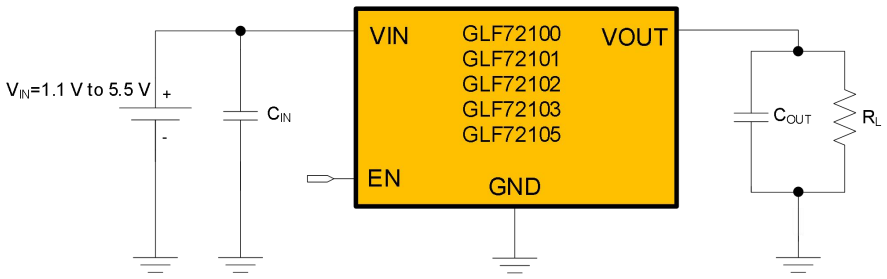
- Portable Devices
- Wearable Devices
- Low Power Subsystems
- Smart IoT Devices

PACKAGE



0.77 mm x 0.77 mm x 0.46 mm WLCSP

APPLICATION DIAGRAM



ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R_{ON} (Typ) at 5.5 V	Output Discharge	V_{OUT} Rise Time t_R (Typ) at 3.3 V	EN Activity	Package
GLF72100	J	37 mΩ	NA	570 µs	High	WLCSP
GLF72101	F		85 Ω		High	WLCSP
*GLF72102 **	*K*		*NA*		*Low*	*WLCSP*
GLF72103	M		85 Ω	48 µs	High	WLCSP with Backside Laminate
GLF72105	N		85 Ω	890 µs	Low	WLCSP with Backside Laminate

Note: GLF72102 is upon request

FUNCTIONAL BLOCK DIAGRAM

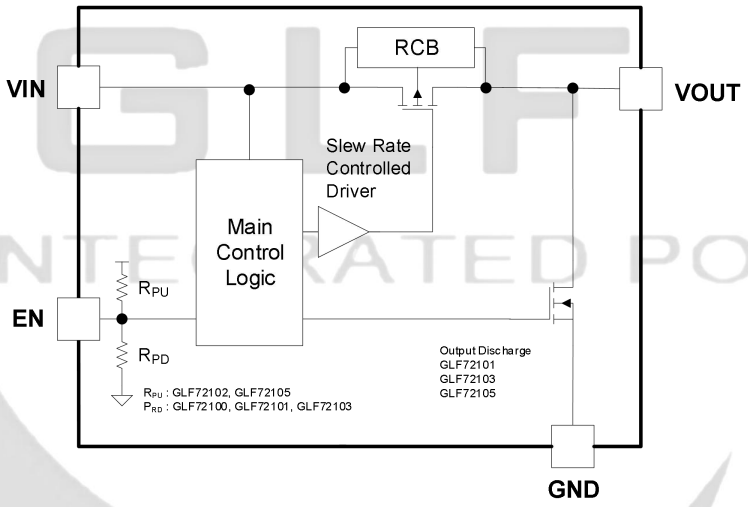


Figure 1. Functional Block Diagram

PIN CONFIGURATION

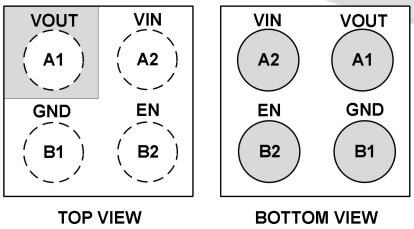


Figure 2. 0.77 mm x 0.77 mm x 0.46 mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1	VOUT	Switch Output
A2	VIN	Switch Input. Supply Voltage for IC
B1	GND	Ground
B2	EN	Enable to control the switch

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, V_{EN}	Each Pin Voltage Range to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			2	A
P_D	Power Dissipation at T_A = 25 °C			1.2	W
T_J	Maximum Junction Temperature			150	°C
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Ambient Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	±4		kV
		Charged Device Model, JESD22-C101	±2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VIN	Supply Voltage	1.5	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

Values are at V_{IN} = 3.3 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Basic Operation							
I_Q	Quiescent Current (1)	EN = Enable, I_{OUT}= 0 mA, V_{IN} = 5.5 V			0.45	1	µA
		EN = Enable, I_{OUT}= 0 mA, V_{IN}= 5.5 V, T_A= 85 °C (4)			0.5		
I_{SD}	Shut Down Current	EN = Disable, I_{OUT}= 0 mA, V_{IN}= 1.5 V			5		nA
		EN = Disable, I_{OUT}= 0 mA, V_{IN}= 3.3 V			9		
		EN = Disable, I_{OUT}= 0 mA, V_{IN}= 4.2 V			12		
		EN = Disable, I_{OUT}= 0 mA, V_{IN}= 5.5 V			20	100	
		EN = Disable, I_{OUT}= 0 mA, V_{IN}= 5.5 V, T_A= 55 °C (4)			50		
R_{ON}	On-Resistance	V_{IN}= 5.5 V, I_{OUT}= 500 mA	T_A = 25 °C		37	42	mΩ
			T_A = 85 °C (4)		43		
		V_{IN}= 3.3 V, I_{OUT}= 500 mA	T_A = 25 °C		47	52	
			T_A = 85 °C (4)		56		
		V_{IN}= 1.8 V, I_{OUT}= 300 mA	T_A = 25 °C (4)		80		
		V_{IN}= 1.5 V, I_{OUT}= 100 mA	T_A = 25 °C		100		
R_{DSC}	Output Discharge Resistance	EN=Low , I_{FORCE}= 10 mA for GLF72101, GLF72103, EN=High , I_{FORCE}= 10 mA for GLF72105			85		Ω
V_{IH}	EN Input Logic High Voltage	V_{IN}= 1.5-5.5 V		1.2			V
V_{IL}	EN Input Logic Low Voltage	V_{IN}= 1.5-5.5 V				0.45	V
R_{EN}	EN Internal Resistance	Pull-down Resistance: GLF72100, GLF72101, GLF72103 Pull-up Resistance: GLF72102, GLF72105			10		MΩ
I_{EN}	EN Current	V_{EN} = V_{IN} or GND			0.5		µA
V_{RCB_TH}	RCB Protection Threshold Voltage	V_{OUT} – V_{IN}			25		mV
V_{RCB_RL}	RCB Protection Release Voltage	V_{IN} – V_{OUT}			30		mV
Switching Characteristics (2): GLF72100, GLF72101							
t_{dON}	Turn-On Delay	R_L= 150 Ω, C_{OUT}= 0.1 µF, GLF72100, GLF72101			430		µs
t_R	V_{OUT} Rise Time				570		
t_{dOFF}	Turn-Off Delay (3), (4)	R_L= 150 Ω, C_{OUT}= 0.1 µF, GLF72100			17		
t_F	V_{OUT} Fall Time (3), (4)				30		
t_{dOFF}	Turn-Off Delay (3), (4)	R_L= 150 Ω, C_{OUT}= 0.1 µF, GLF72101			17		
t_F	V_{OUT} Fall Time (3), (4)				15		
Switching Characteristics (2): GLF72103							
t_{dON}	Turn-On Delay	R_L= 150 Ω, C_{OUT}= 0.1 µF			50		µs
t_R	V_{OUT} Rise Time				48		
t_{dOFF}	Turn-Off Delay (3), (4)				17		
t_F	V_{OUT} Fall Time (3), (4)				15		
Switching Characteristics (2): GLF72105							
t_{dON}	Turn-On Delay	R_L= 150 Ω, C_{OUT}= 0.1 µF			640		µs
t_R	V_{OUT} Rise Time				890		
t_{dOFF}	Turn-Off Delay (3), (4)				16		
t_F	V_{OUT} Fall Time (3), (4)				10		

Notes:
1. I_Q does not include the enable pull down current (I_{EN}) through the pull-down resistor R_{EN}.
2. t_{ON} = t_{dON} + t_R, t_{OFF} = t_{dOFF} + t_F
3. Output discharge path is enabled during off.
4. By design; characterized, not production tested.

TIMING DIAGRAM

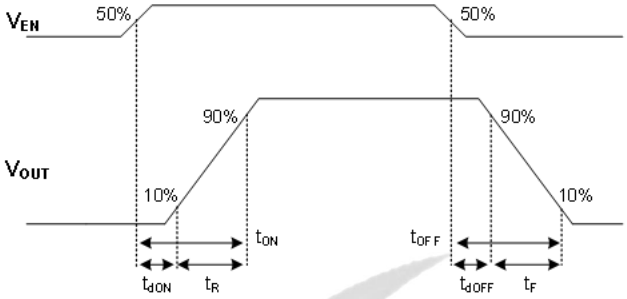


Figure 3. GLF72100/ GLF72101/ GLF72103 Timing Diagram

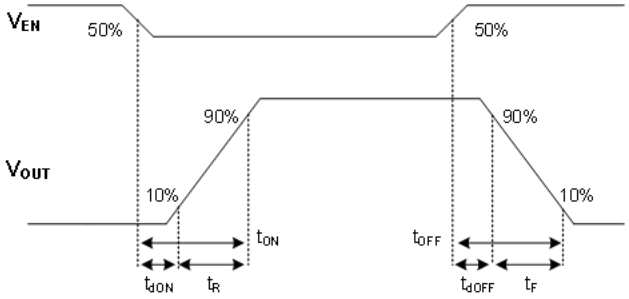


Figure 4. GLF72102/GLF72105 Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

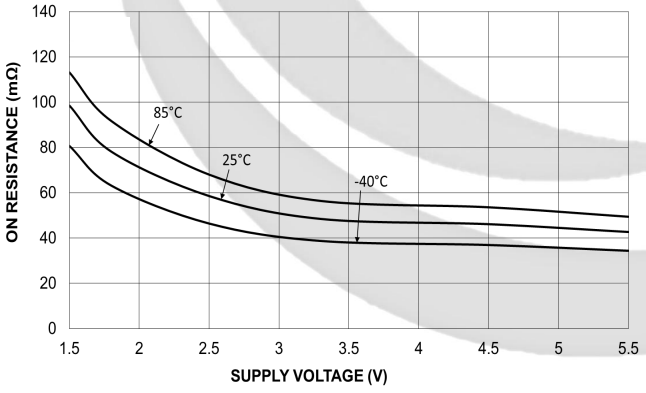


Figure 5. On-Resistance vs. Supply Voltage

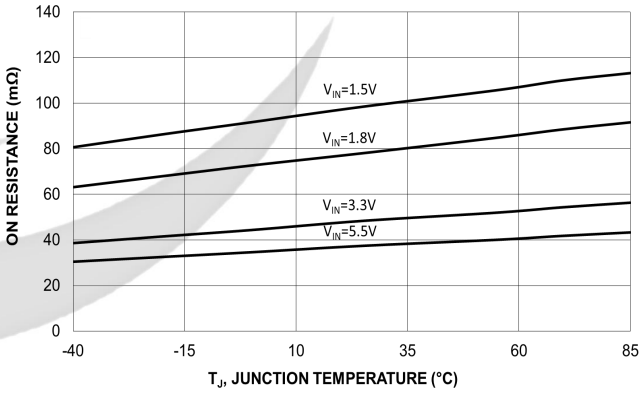


Figure 6. On-Resistance vs. Temperature

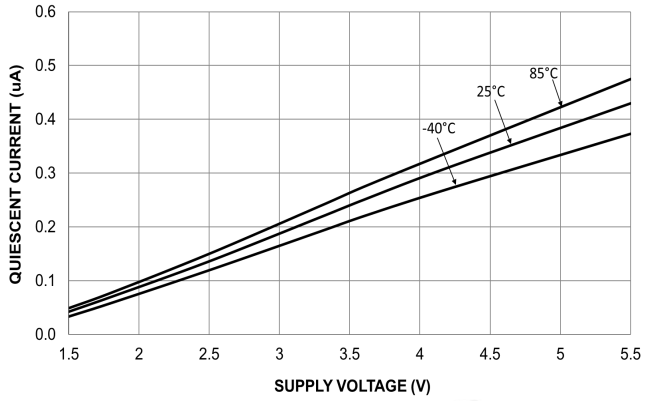


Figure 7. Quiescent Current vs. Supply Voltage

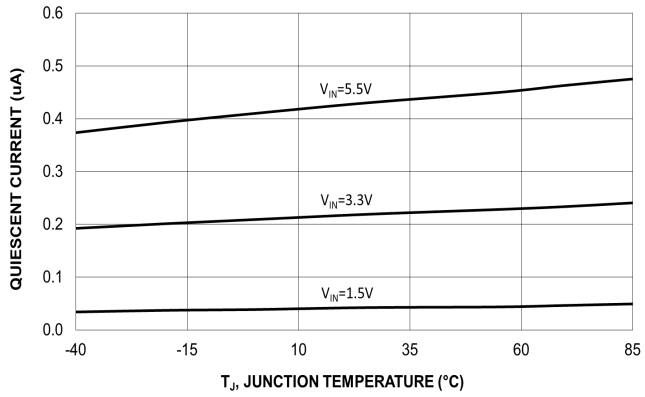


Figure 8. Quiescent Current vs. Temperature

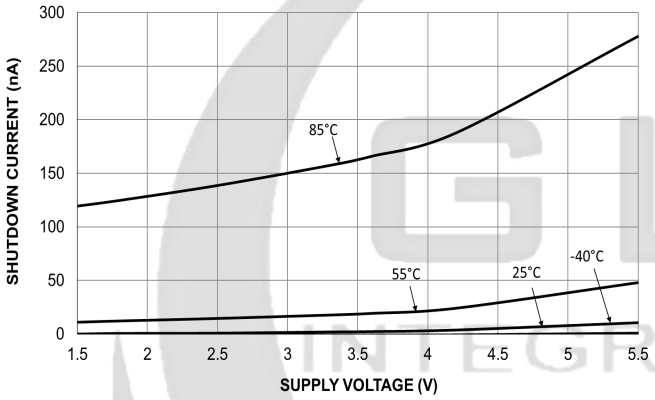


Figure 9. Shutdown Current vs. Supply Voltage

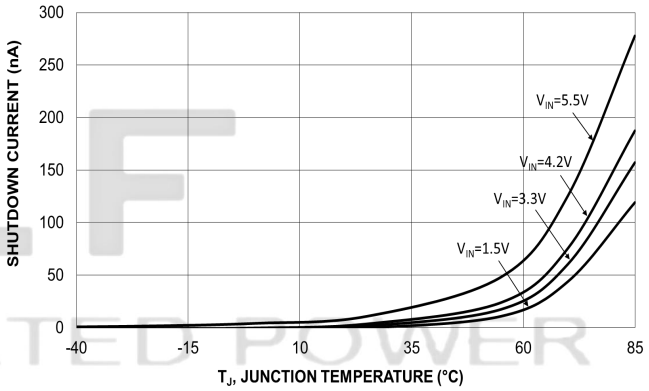


Figure 10. Shutdown Current vs. Temperature

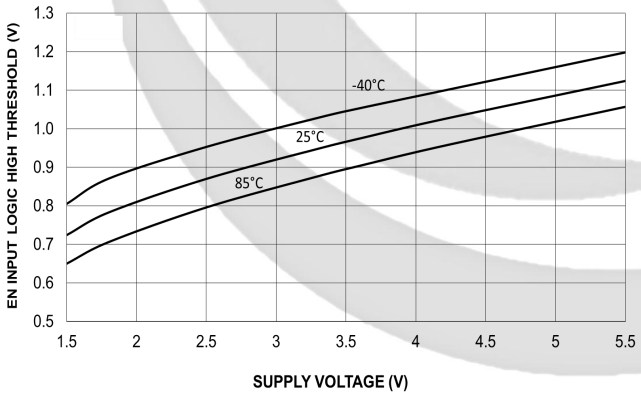


Figure 11. EN Input Logic High Threshold

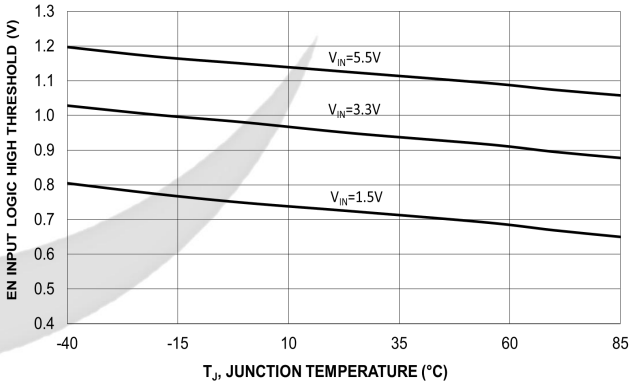


Figure 12. EN Input Logic High Threshold Vs. Temperature

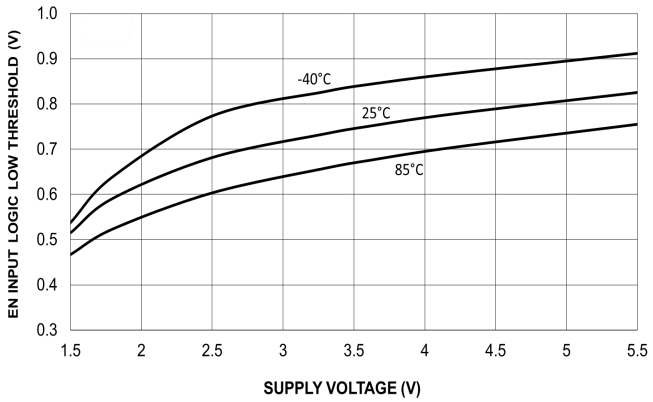


Figure 13. EN Input Logic Low Threshold

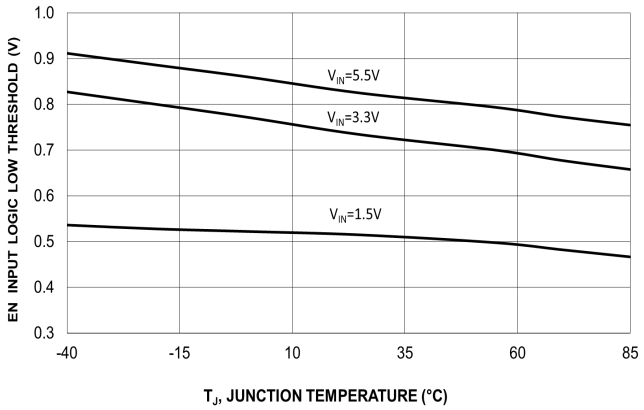


Figure 14. EN Input Logic Low Threshold Vs. Temperature

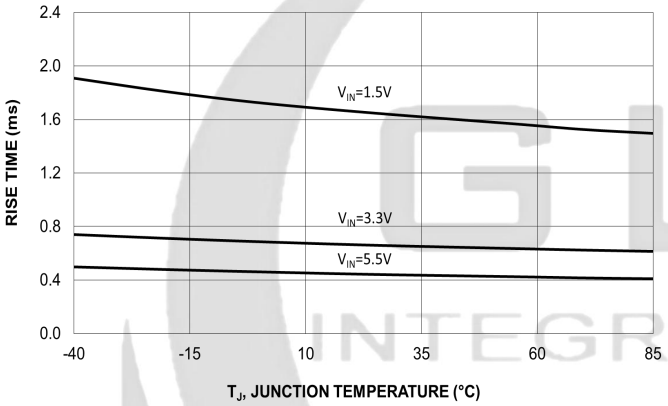


Figure 15. V_{OUT} Rise Time vs. Temperature
GLF72100 and GLF72101

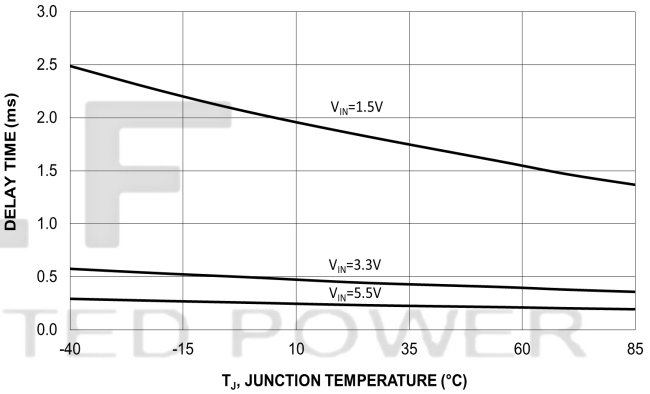


Figure 16. Turn-On Delay Time vs. Temperature
GLF72100 and GLF72101

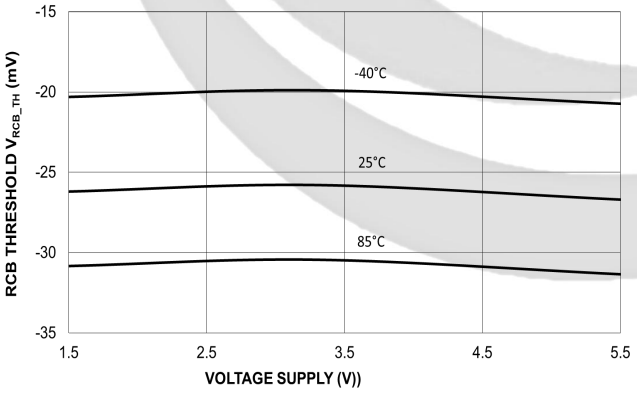


Figure 17. RCP Threshold Voltage vs. Supply Voltage

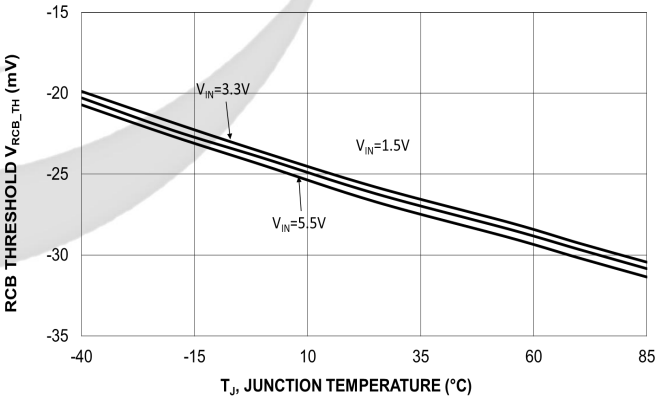


Figure 18. RCP Threshold Voltage vs. Temperature

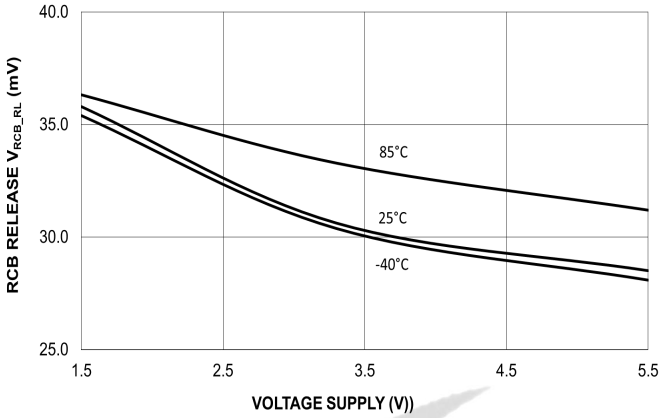


Figure 19. RCP Release Voltage vs. Supply Voltage

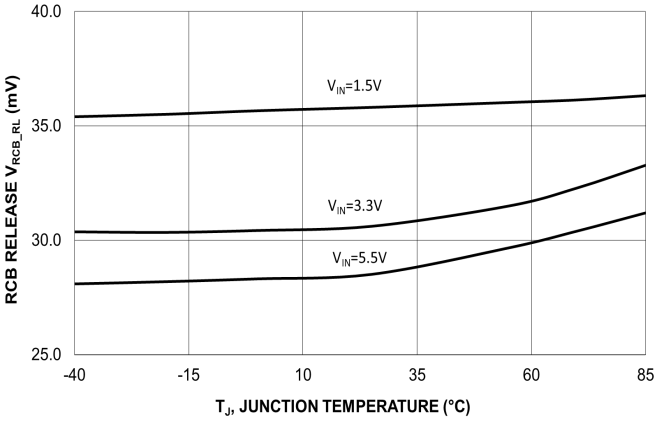


Figure 20. RCP Release Voltage vs. Temperature

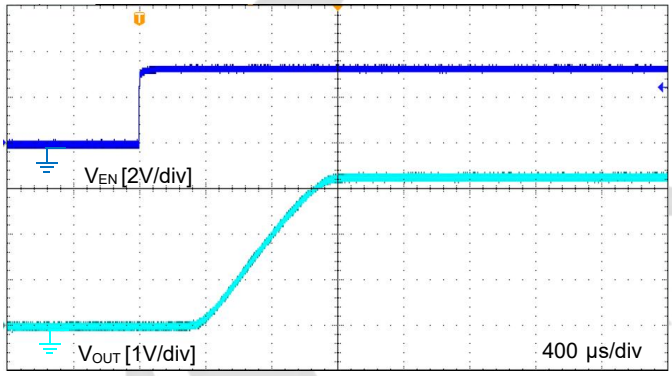


Figure 21. Turn-On Response, GLF72100
V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=0.1 µF, R_L=150 Ω

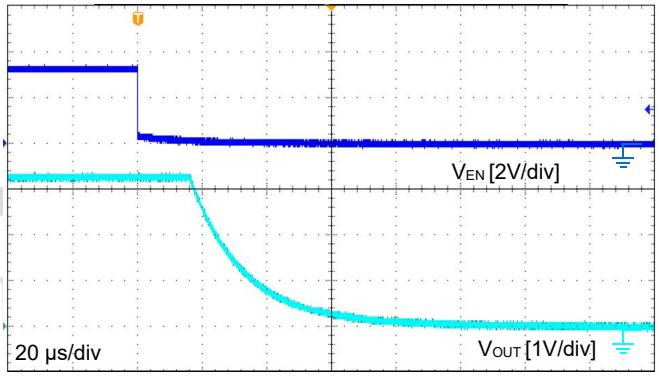


Figure 22. Turn-Off Response, GLF72100
V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=0.1 µF, R_L=150 Ω

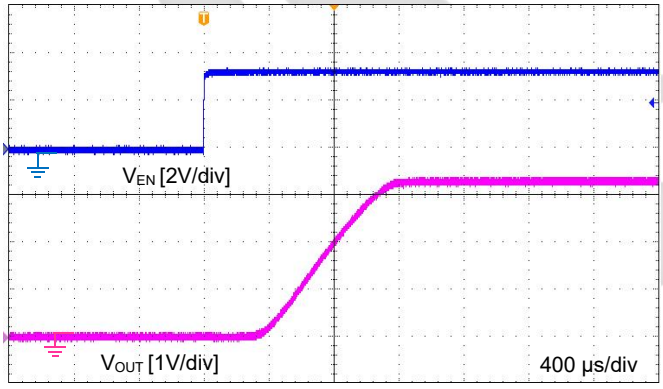


Figure 23. Turn-On Response, GLF72101
V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=0.1 µF, R_L=150 Ω

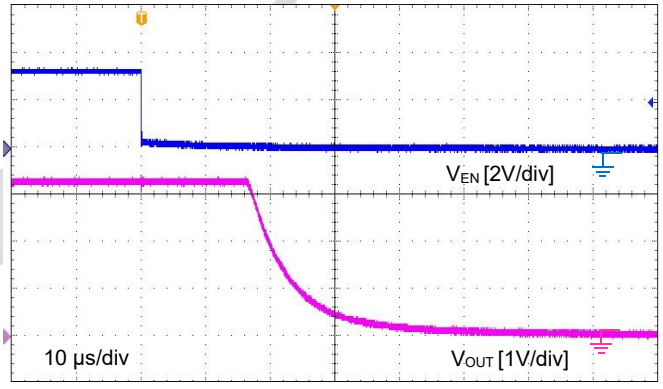


Figure 24. Turn-Off Response, GLF72101
V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=0.1 µF, R_L=150 Ω

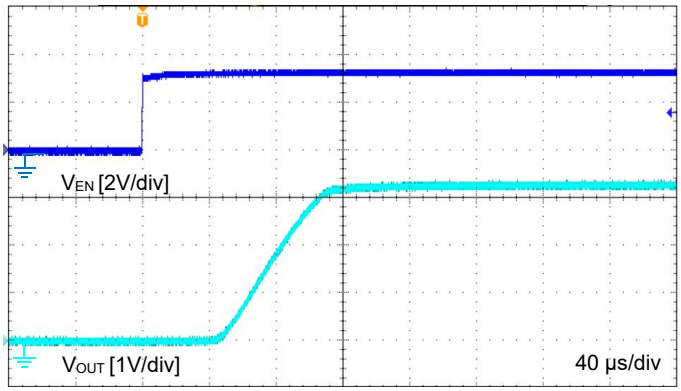


Figure 25. Turn-On Response, GLF72103
V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=0.1 µF, R_L=150 Ω

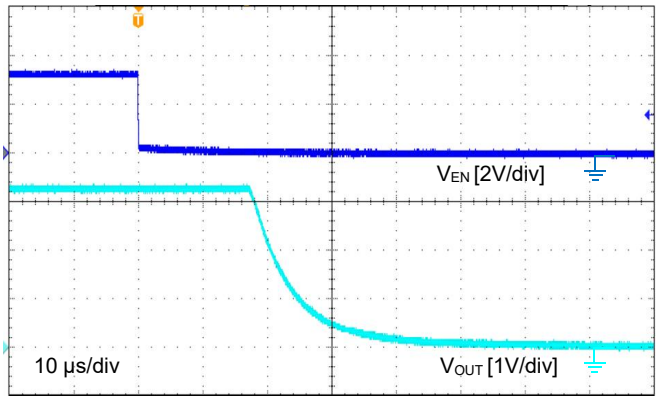


Figure 26. Turn-Off Response, GLF72103
V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=0.1 µF, R_L=150 Ω

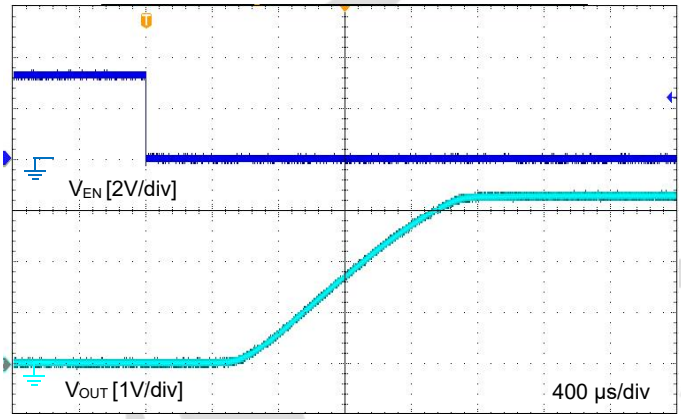


Figure 27. Turn-On Response, GLF72105
V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=0.1 µF, R_L=150 Ω

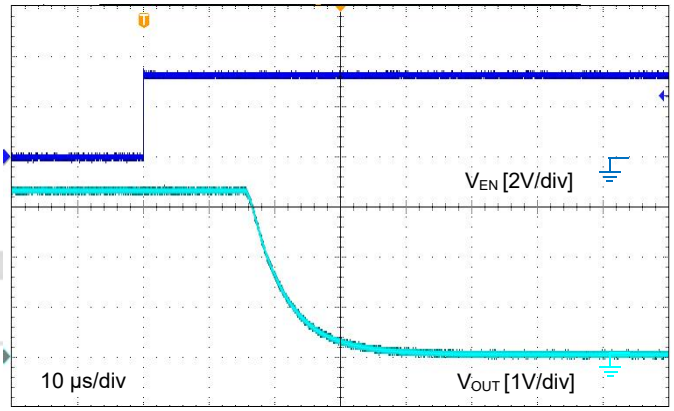


Figure 28. Turn-Off Response, GLF72105
V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=0.1 µF, R_L=150 Ω

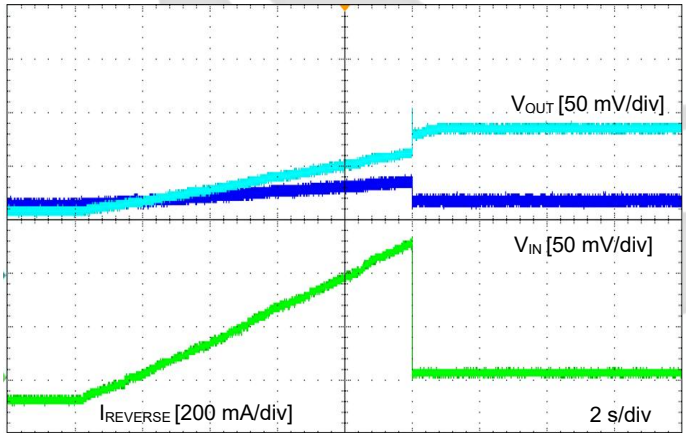


Figure 29. Reverse Current Blocking Threshold
V_{IN}=3.3 V, V_{OUT}=Up to 3.4 V in C_{IN}=0.1 µF, C_{OUT}=0.1 µF

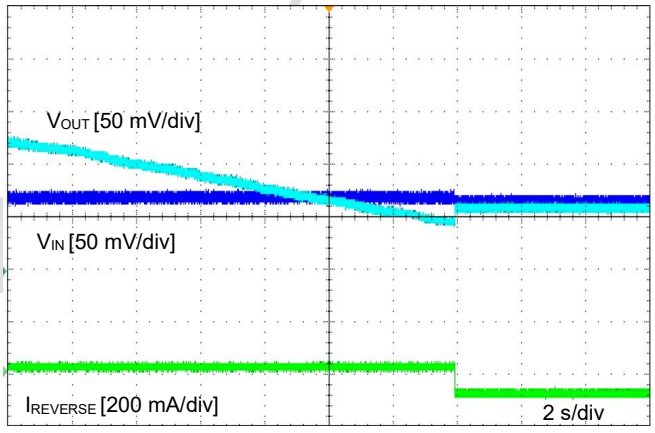


Figure 30. Reverse Current Blocking Release
V_{IN}=3.3 V, V_{OUT}=Down to 3.2 V in C_{IN}=0.1 µF, C_{OUT}=0.1 µF

APPLICATION INFORMATION

The GLF7210x product family is an integrated 2 A, nano current leakage I_QSmart™ load switches with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.5 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power. The package is a 0.77 mm x 0.77 mm x 0.46 mm wafer level chip scale package, saving space in compact applications. It is constructed using 4 bumps, with a 0.4 mm pitch for manufacturability.

Input Capacitor

The GLF7210x product family does not require an input capacitor. However, to reduce the voltage drop on the input power rail caused by transient inrush current at start-up, a 0.1 µF capacitor is recommended to be placed close to the VIN pin. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

The GLF7210x product family does not require an output capacitor. However, use of an output capacitor is recommended to mitigate voltage undershoot on the output pin when the switch is turning off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be spaced close to the VOUT and GND pins.

EN Pin

The GLF72100, GLF72101, and GLF72103 can be activated by forcing EN pin high level and the GLF72102, GLF72105 by EN pin low level. Note that the EN pin has an internal pull-down/ pull-up resistor to help pull the main switch to a known “off state” when no EN signal is applied from an external controller.

Reverse Current Blocking

The GLF7210x product family has a built-in reverse current blocking protection which always monitors the output voltage level regardless of the status of EN pin to check if it is greater than the input voltage. When the output voltage goes beyond the input voltage by 25 mV, that is the reverse current blocking protection threshold voltage (V_{RCB_TH}), the reverse current blocking function block turns off the switch. Note that some reverse current can occur until the V_{RCB_TH} is triggered. The main switch will resume normal operation when the output voltage drops below the input source by the reverse current blocking protection release voltage (V_{RCB_RL}).

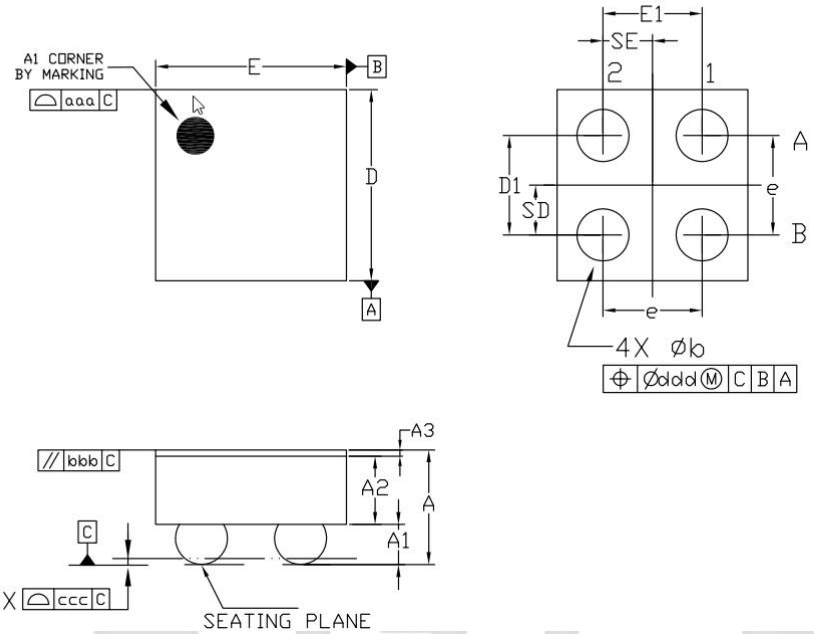
Output Discharge Function

The GLF72101, GLF72103, and GLF72105 have an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

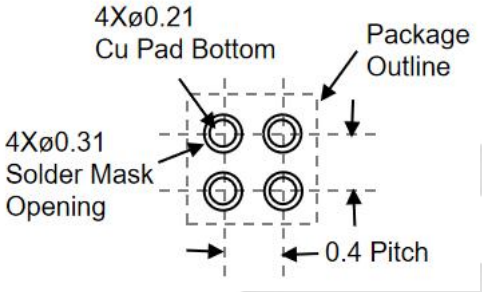
All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

PACKAGE OUTLINE



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.410	0.460	0.510
A1	0.135	0.160	0.185
A2	0.250	0.275	0.300
A3	0.020	0.025	0.030
D	0.755	0.770	0.785
E	0.755	0.770	0.785
D1	0.350	0.400	0.450
E1	0.350	0.400	0.450
b	0.170	0.210	0.250
e	0.400 BSC		
SD	0.200 BSC		
SE	0.200 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Recommended Footprint

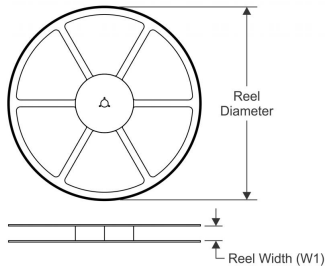


Notes

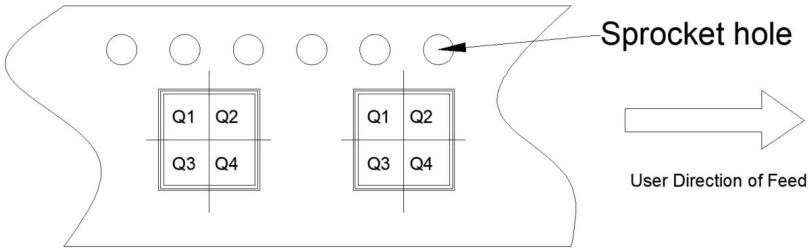
1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

TAPE AND REEL INFORMATION

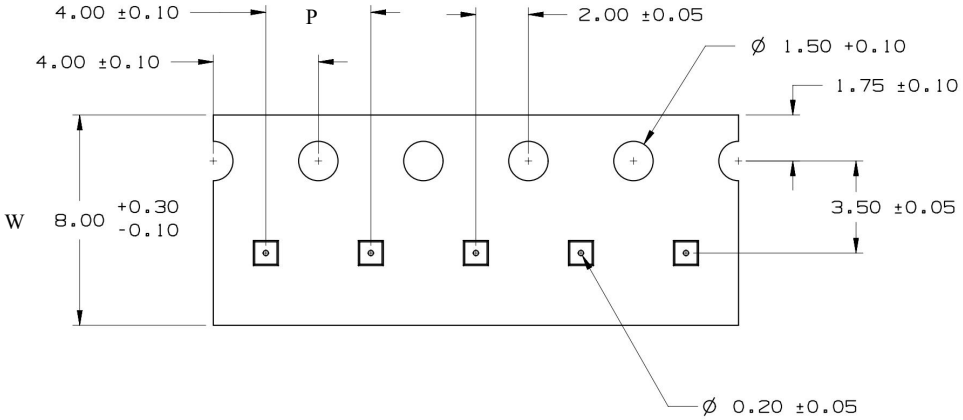
Reel Dimensions

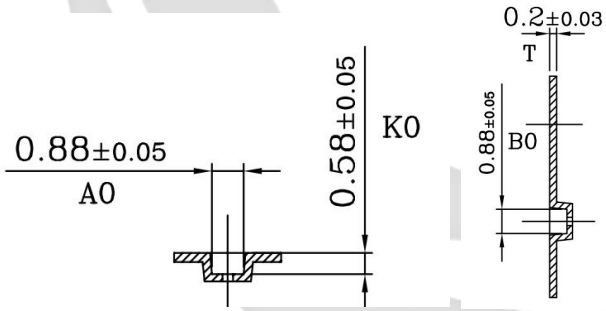


Quadrant Assignments PIN1 Orientation Tape



Tape Dimensions





Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF72100	WLCSP	4	4000	179	9	0.88	0.88	0.58	4	8	Q1
GLF72101	WLCSP	4	4000	179	9	0.88	0.88	0.58	4	8	Q1
GLF72102	WLCSP	4	4000	179	9	0.88	0.88	0.58	4	8	Q1
GLF72103	WLCSP	4	4000	179	9	0.88	0.88	0.58	4	8	Q1
GLF72105	WLCSP	4	4000	179	9	0.88	0.88	0.58	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P1: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Parameters including the typical, minimum, and maximum values are desired, or target. GLF reserves the right to change contents at any time without warning or notification. A target specification will not guarantee the future production of the device.	Design / Development
Preliminary Specification	This is a draft version of a product specification which is under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification will not guarantee the future production of the device.	Qualification
Product Specification	This document represents the characteristics of the device.	Production

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