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DATASHEET

HS-1100RH

Radiation Hardened, Ultra High Speed Current Feedback Amplifier

FN4100
Rev 2.00
August 1999

The HS-1100RH is a radiation hardened high speed, wideband, fast settling current feedback amplifier. Built with Intersil's proprietary, complementary bipolar UHF-1 (DI bonded wafer) process, it is the fastest monolithic amplifier available from any semiconductor manufacturer. These devices are QML approved and are processed and screened in full compliance with MIL-PRF-38535.

The HS-1100RH's wide bandwidth, fast settling characteristic, and low output impedance make this amplifier ideal for driving fast A/D converters.

Component and composite video systems will also benefit from this amplifier's performance, as indicated by the excellent gain flatness, and 0.03%/0.05 Deg. Differential Gain/Phase specifications ($R_L = 75\Omega$).

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-94676. A "hot-link" is provided on our homepage for downloading. http://www.intersil.com/spacedefense/space.htm

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)
5962F9467602VPA	HS7-1100RH-Q	-55 to 125
5962F9467602VPC	HS7B-1100RH-Q	-55 to 125
HFA1100IJ (Sample)	HFA1100IJ	-40 to 85
HFA11XXEVAL	Evaluation Board	

Features

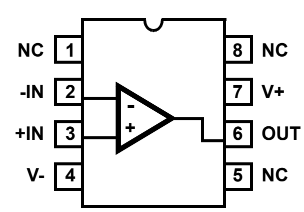
- Electrically Screened to SMD # 5962-94676
- QML Qualified per MIL-PRF-38535 Requirements
- Low Distortion (HD3, 30MHz) . . . . -84dBc (Typ)
- Wide -3dB Bandwidth. . . . . 850MHz (Typ)
- Very High Slew Rate . . . . 2300V/µs (Typ)
- Fast Settling (0.1%) . . . . 11ns (Typ)
- Excellent Gain Flatness (to 50MHz). . . . . . . 0.05dB (Typ)
- High Output Current . . . . 65mA (Typ)
- Fast Overdrive Recovery . . . . <10ns (Typ)
- Total Gamma Dose . . . . 300kRAD(Si)
- Latch Up. . . . . None (DI Technology)

Applications

- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Imaging Systems

Pinout

HS-1100RH
GDIP1-T8 (CERDIP)
OR CDIP2-T8 (SBDIP)
TOP VIEW



Typical Applications

Optimum Feedback Resistor

The enclosed plots of inverting and non-inverting frequency response illustrate the performance of the HS-1100RH in various gains. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HS-1100RH design is optimized for a 510Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (ACL)	R_F (Ω)	BANDWIDTH (MHz)
-1	430	580
+1	510	850
+2	360	670
+5	150	520
+10	180	240
+19	270	125

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

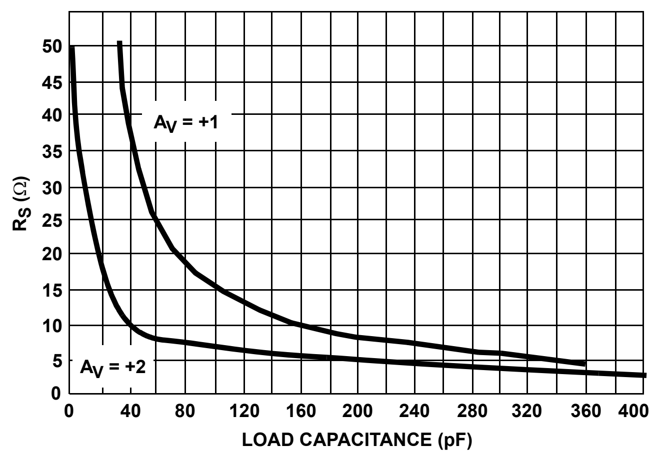


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at A_V = +1, R_S = 50Ω, C_L = 30pF, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at A_V = +1, R_S = 5Ω, C_L = 340pF.

Evaluation Board

The performance of the HS-1100RH may be evaluated using the HFA11XXEVAL Evaluation Board.

The layout and schematic of the board are shown in Figure 2. To order evaluation boards, please contact your local sales office.

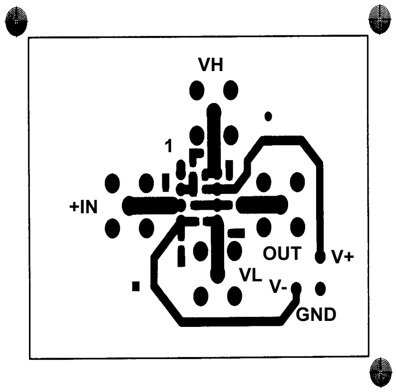


FIGURE 2A. TOP LAYOUT

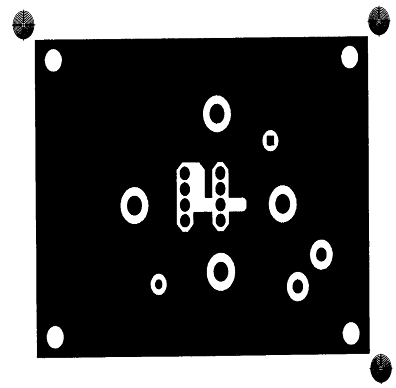


FIGURE 2B. BOTTOM LAYOUT

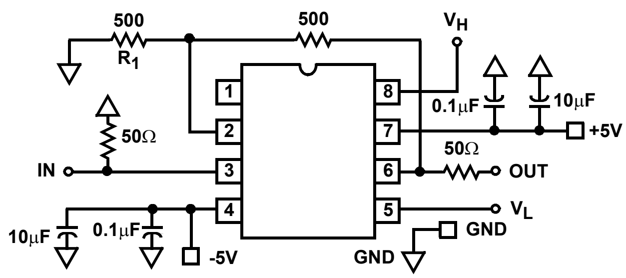


FIGURE 2C. SCHEMATIC

FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Typical Performance Characteristics

Device Characterized at: V_{SUPPLY} = ±5V, R_F = 360Ω, A_V = +2V/V, R_L = 100Ω, Unless Otherwise Specified

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	UNITS
Input Offset Voltage (Note 1)	V_{CM} = 0V	25°C	2	mV
Average Offset Voltage Drift	Versus Temperature	Full	10	µV/°C
V_{IO} CMRR	ΔV_{CM} = ±2V	25°C	46	dB
V_{IO} PSRR	ΔV_S = ±1.25V	25°C	50	dB
+Input Current (Note 1)	V_{CM} = 0V	25°C	25	µA
Average +Input Current Drift	Versus Temperature	Full	40	nA/°C
- Input Current (Note 1)	V_{CM} = 0V	25°C	12	µA
Average -Input Current Drift	Versus Temperature	Full	40	nA/°C
+Input Resistance	ΔV_{CM} = ±2V	25°C	50	kΩ
- Input Resistance		25°C	16	Ω
Input Capacitance		25°C	2.2	pF
Input Noise Voltage (Note 1)	f = 100kHz	25°C	4	nV/√Hz
+Input Noise Current (Note 1)	f = 100kHz	25°C	18	pA/√Hz
-Input Noise Current (Note 1)	f = 100kHz	25°C	21	pA/√Hz
Input Common Mode Range		Full	±3.0	V
Open Loop Transimpedance	A_V = -1	25°C	500	kΩ

Typical Performance Characteristics (Continued)

Device Characterized at: V_{SUPPLY} = ±5V, R_F = 360Ω, A_V = +2V/V, R_L = 100Ω, Unless Otherwise Specified

PARAMETERS	CONDITIONS	TEMPERATURE	TYPICAL	UNITS
Output Voltage	A_V = -1, R_L = 100Ω	25°C	±3.3	V
	A_V = -1, R_L = 100Ω	Full	±3.0	V
Output Current (Note 1)	A_V = -1, R_L = 50Ω	25°C to 125°C	±65	mA
	A_V = -1, R_L = 50Ω	-55°C to 0°C	±50	mA
DC Closed Loop Output Resistance		25°C	0.1	W
Quiescent Supply Current (Note 1)	R_L = Open	Full	24	mA
-3dB Bandwidth (Note 1)	A_V = -1, R_F = 430Ω, V_{OUT} = 200mV_{P-P}	25°C	580	MHz
	A_V = +1, R_F = 510Ω, V_{OUT} = 200mV_{P-P}	25°C	850	MHz
	A_V = +2, R_F = 360Ω, V_{OUT} = 200mV_{P-P}	25°C	670	MHz
Slew Rate	A_V = +1, R_F = 510Ω, V_{OUT} = 5V_{P-P}	25°C	1500	V/μs
	A_V = +2, V_{OUT} = 5V_{P-P}	25°C	2300	V/μs
Full Power Bandwidth	V_{OUT} = 5V_{P-P}	25°C	220	MHz
Gain Flatness (Note 1)	To 30MHz, R_F = 510Ω	25°C	±0.014	dB
	To 50MHz, R_F = 510Ω	25°C	±0.05	dB
	To 100MHz, R_F = 510Ω	25°C	±0.14	dB
Linear Phase Deviation (Note 1)	To 100MHz, R_F = 510Ω	25°C	±0.6	Degrees
2nd Harmonic Distortion (Note 1)	30MHz, V_{OUT} = 2V_{P-P}	25°C	-55	dBc
	50MHz, V_{OUT} = 2V_{P-P}	25°C	-49	dBc
	100MHz, V_{OUT} = 2V_{P-P}	25°C	-44	dBc
3rd Harmonic Distortion (Note 1)	30MHz, V_{OUT} = 2V_{P-P}	25°C	-84	dBc
	50MHz, V_{OUT} = 2V_{P-P}	25°C	-70	dBc
	100MHz, V_{OUT} = 2V_{P-P}	25°C	-57	dBc
3rd Order Intercept (Note 1)	100MHz, R_F = 510Ω	25°C	30	dBm
1dB Compression	100MHz, R_F = 510Ω	25°C	20	dBm
Reverse Isolation (S12)	40MHz, R_F = 510Ω	25°C	-70	dB
	100MHz, R_F = 510Ω	25°C	-60	dB
	600MHz, R_F = 510Ω	25°C	-32	dB
Rise and Fall Time	V_{OUT} = 0.5V_{P-P}	25°C	500	ps
	V_{OUT} = 2V_{P-P}	25°C	800	ps
Overshoot (Note 1)	V_{OUT} = 0.5V_{P-P}, Input t_R/t_F = 550ps	25°C	11	%
Settling Time (Note 1)	To 0.1%, V_{OUT} = 2V to 0V, R_F = 510Ω	25°C	11	ns
	To 0.05%, V_{OUT} = 2V to 0V, R_F = 510Ω	25°C	19	ns
	To 0.02%, V_{OUT} = 2V to 0V, R_F = 510Ω	25°C	34	ns
Differential Gain	A_V = +2, R_L = 75Ω, NTSC	25°C	0.03	%
Differential Phase	A_V = +2, R_L = 75Ω, NTSC	25°C	0.05	Degrees
Overdrive Recovery Time	R_F = 510Ω, V_{IN} = 5V_{P-P}	25°C	7.5	ns

NOTE:

1. See Typical Performance Curves for more information.

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $R_L = 100\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

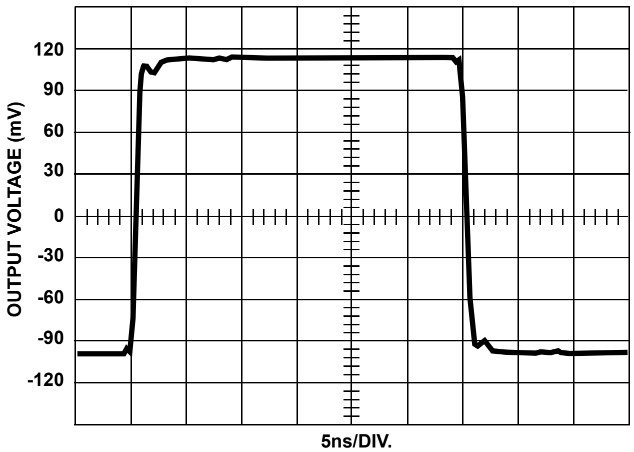


FIGURE 3. SMALL SIGNAL PULSE RESPONSE (A_V = +2)

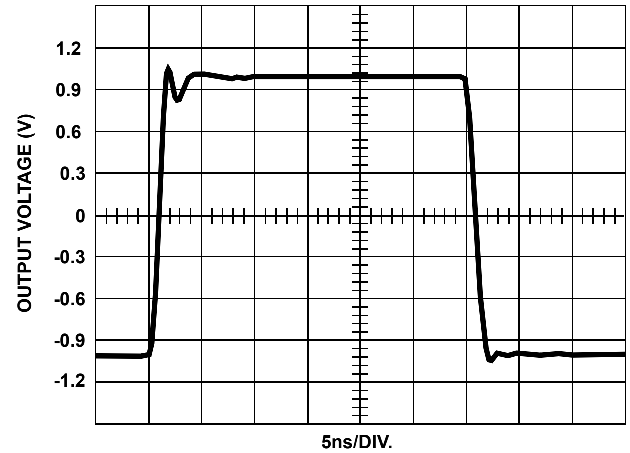


FIGURE 4. LARGE SIGNAL PULSE RESPONSE (A_V = +2)

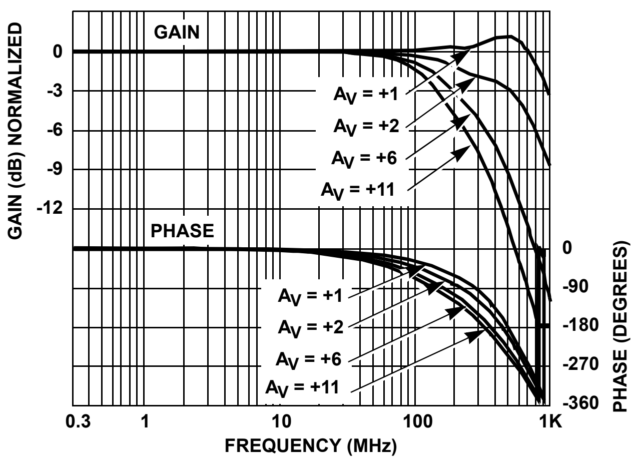


FIGURE 5. NON-INVERTING FREQUENCY RESPONSE (V_{OUT} = 200mV_{P-P})

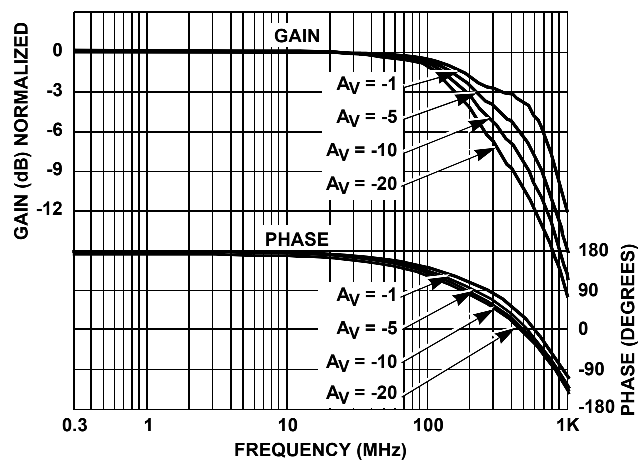


FIGURE 6. INVERTING FREQUENCY RESPONSE (V_{OUT} = 200mV_{P-P})

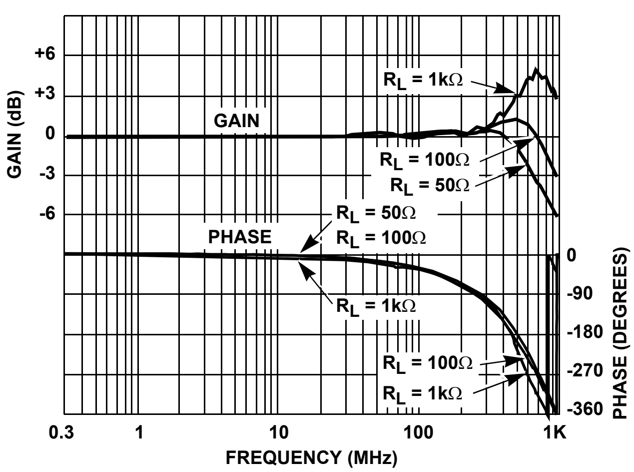


FIGURE 7. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS (A_V = +1, V_{OUT} = 200mV_{P-P})

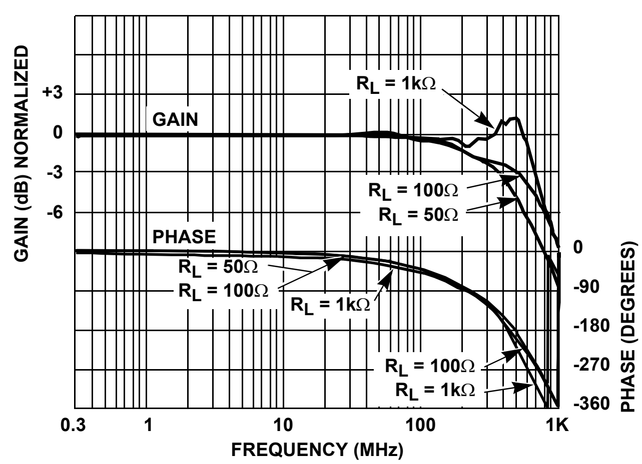


FIGURE 8. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS (A_V = +2, V_{OUT} = 200mV_{P-P})

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $R_L = 100\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

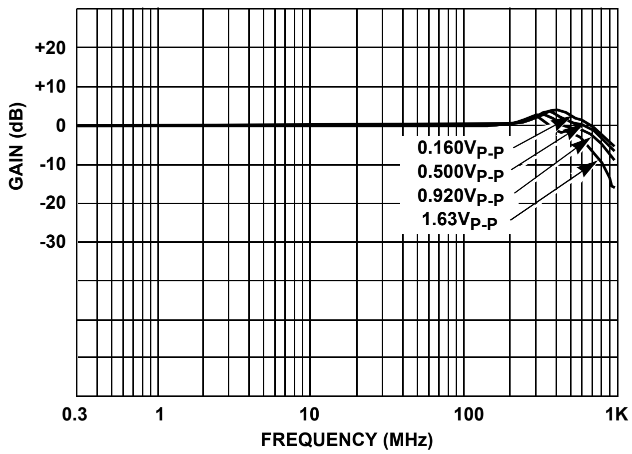


FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES ($A_V = +1$)

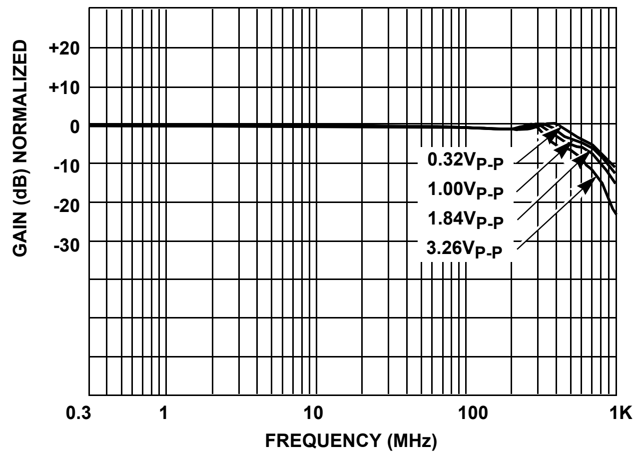


FIGURE 10. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES ($A_V = +2$)

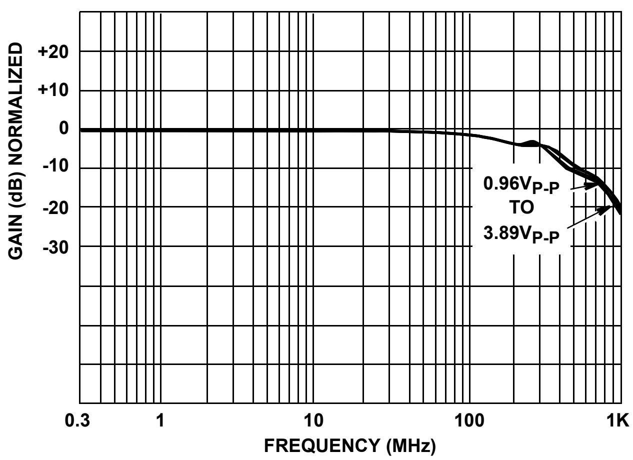


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES ($A_V = +6$)

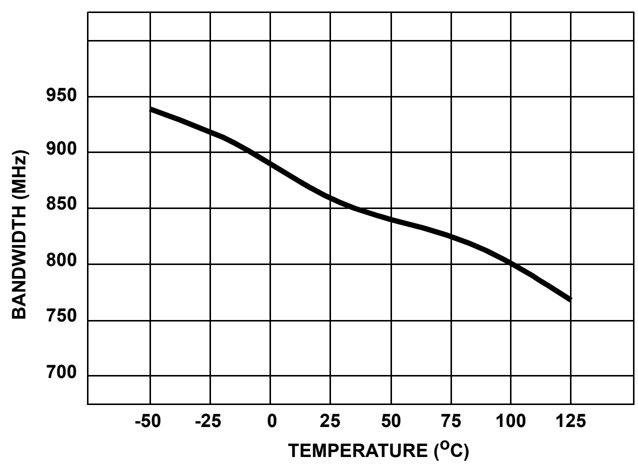


FIGURE 12. -3dB BANDWIDTH vs TEMPERATURE ($A_V = +1$)

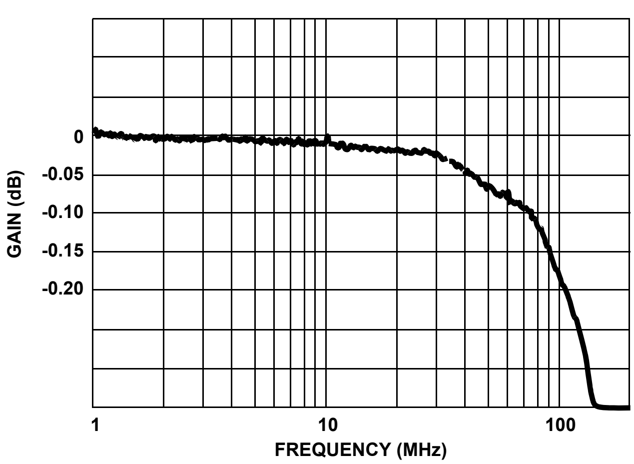


FIGURE 13. GAIN FLATNESS ($A_V = +2$)

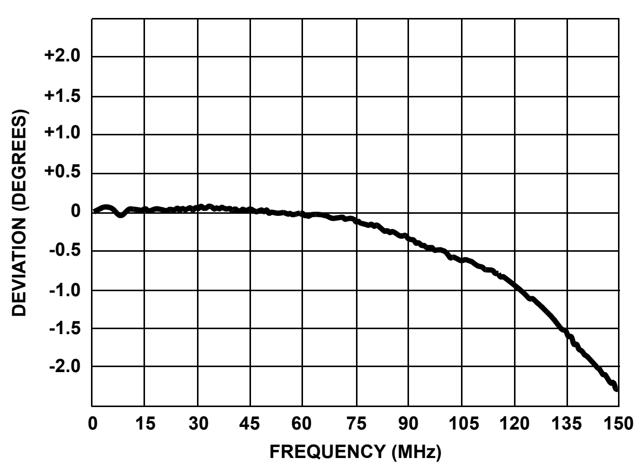


FIGURE 14. DEVIATION FROM LINEAR PHASE ($A_V = +2$)

Typical Performance Curves V_{SUPPLY} = ±5V, R_F = 510Ω, R_L = 100Ω, T_A = 25°C, Unless Otherwise Specified **(Continued)**

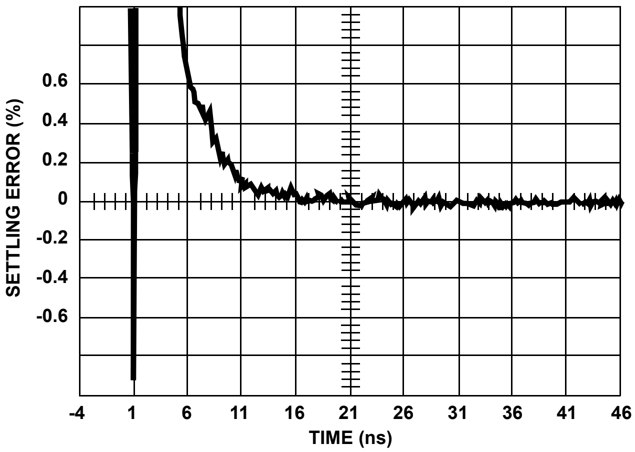


FIGURE 15. SETTLING RESPONSE (A_V = +2, V_{OUT} = 2V)

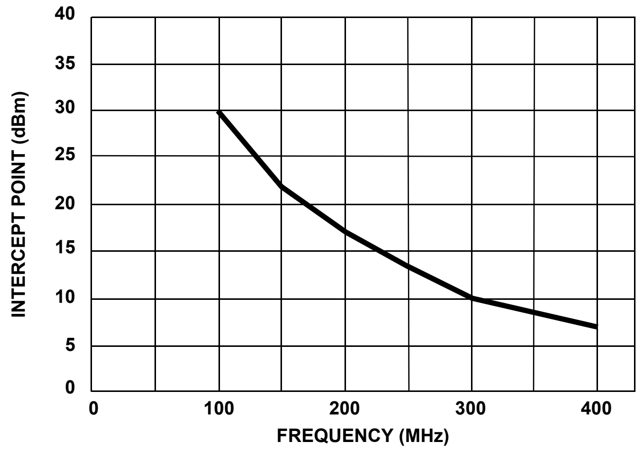


FIGURE 16. 3RD ORDER INTERMODULATION INTERCEPT (2-TONE)

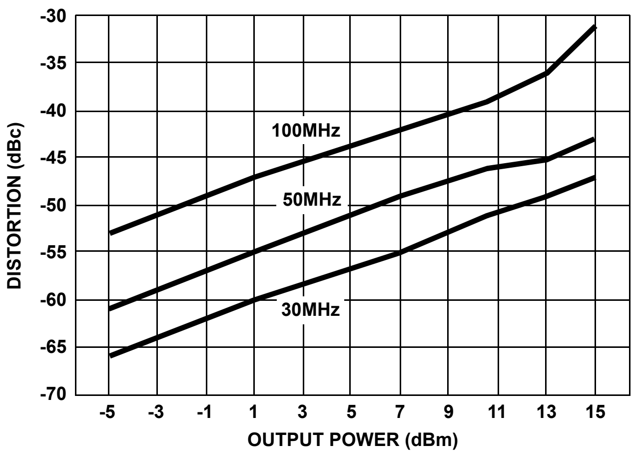


FIGURE 17. 2ND HARMONIC DISTORTION vs P_{OUT}

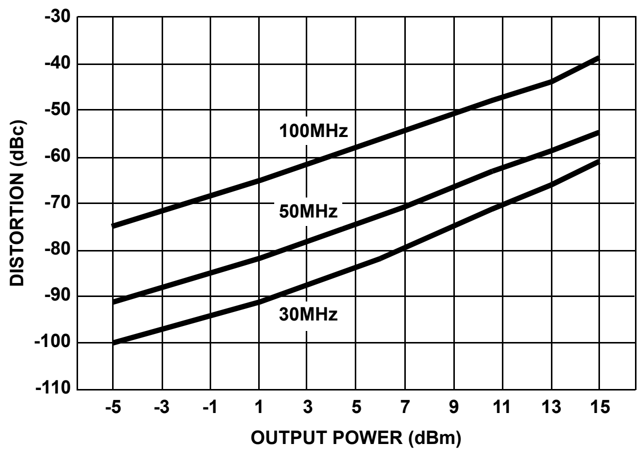


FIGURE 18. 3RD HARMONIC DISTORTION vs P_{OUT}

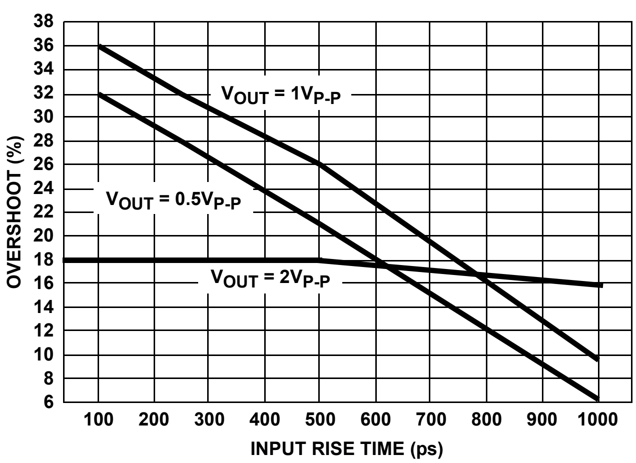


FIGURE 19. OVERSHOOT vs INPUT RISE TIME (A_V = +1)

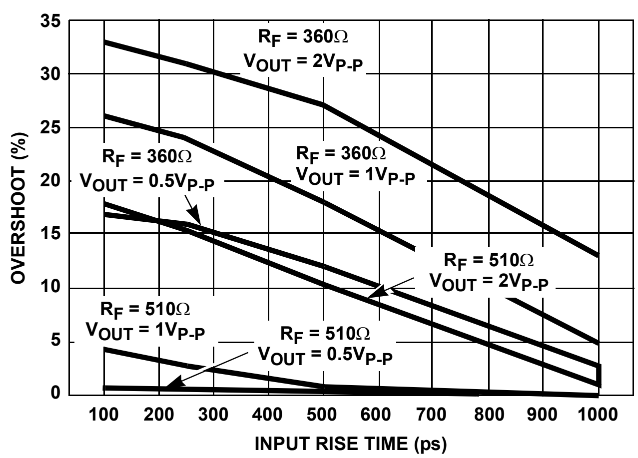


FIGURE 20. OVERSHOOT vs INPUT RISE TIME (A_V = +2)

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $R_F = 510\Omega$, $R_L = 100\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

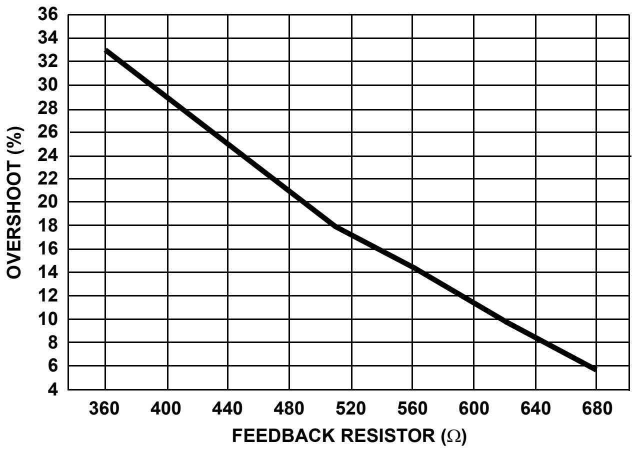


FIGURE 21. OVERSHOOT vs FEEDBACK RESISTOR (A_V = +2, t_R = 200ps, V_{OUT} = 2V_{P-P})

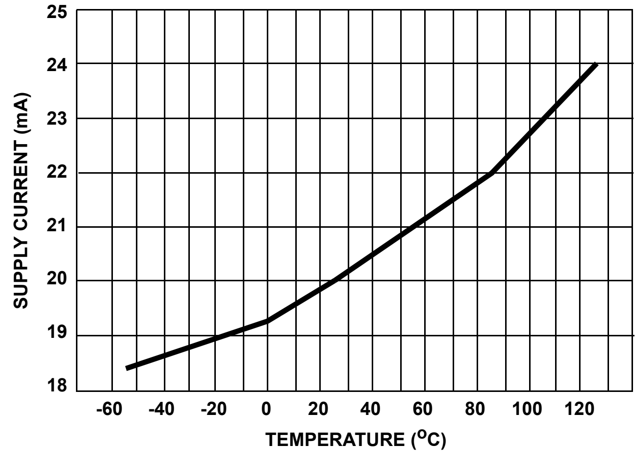


FIGURE 22. SUPPLY CURRENT vs TEMPERATURE

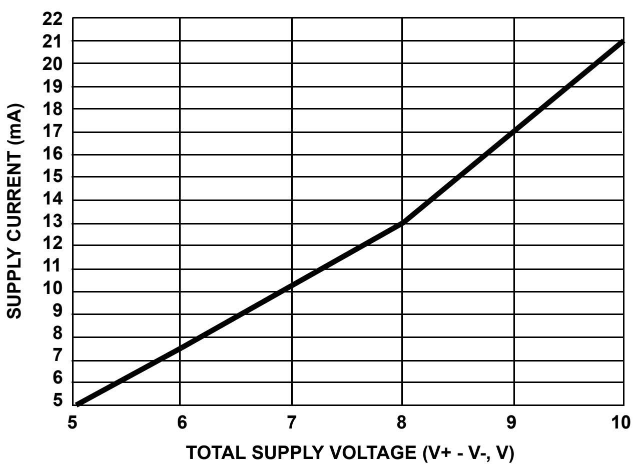


FIGURE 23. SUPPLY CURRENT vs SUPPLY VOLTAGE

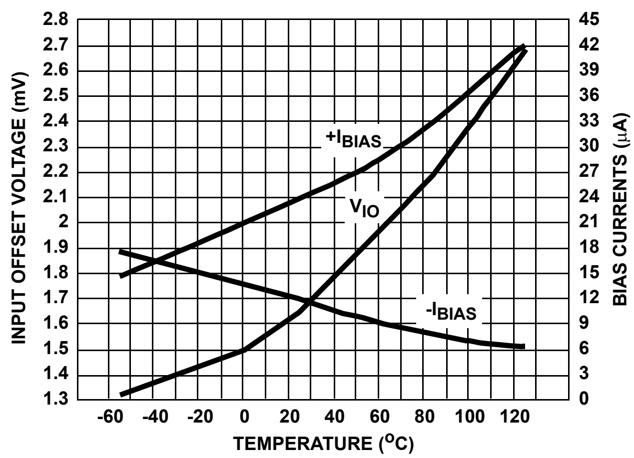


FIGURE 24. V_{IO} AND BIAS CURRENTS vs TEMPERATURE

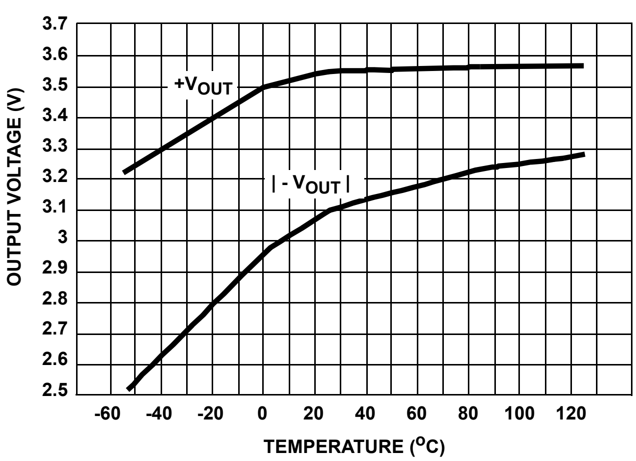


FIGURE 25. OUTPUT VOLTAGE vs TEMPERATURE (A_V = -1, R_L = 50Ω)

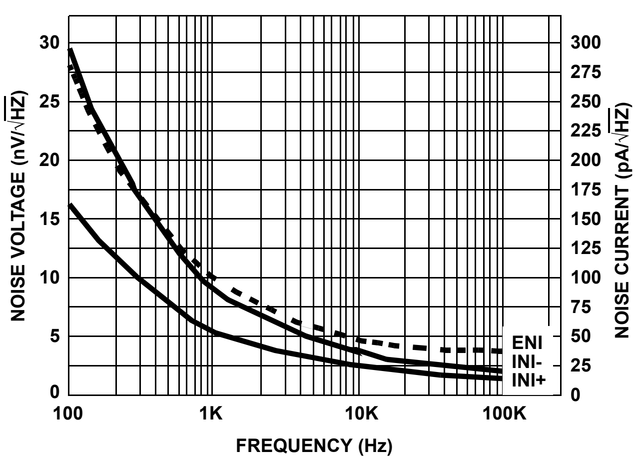
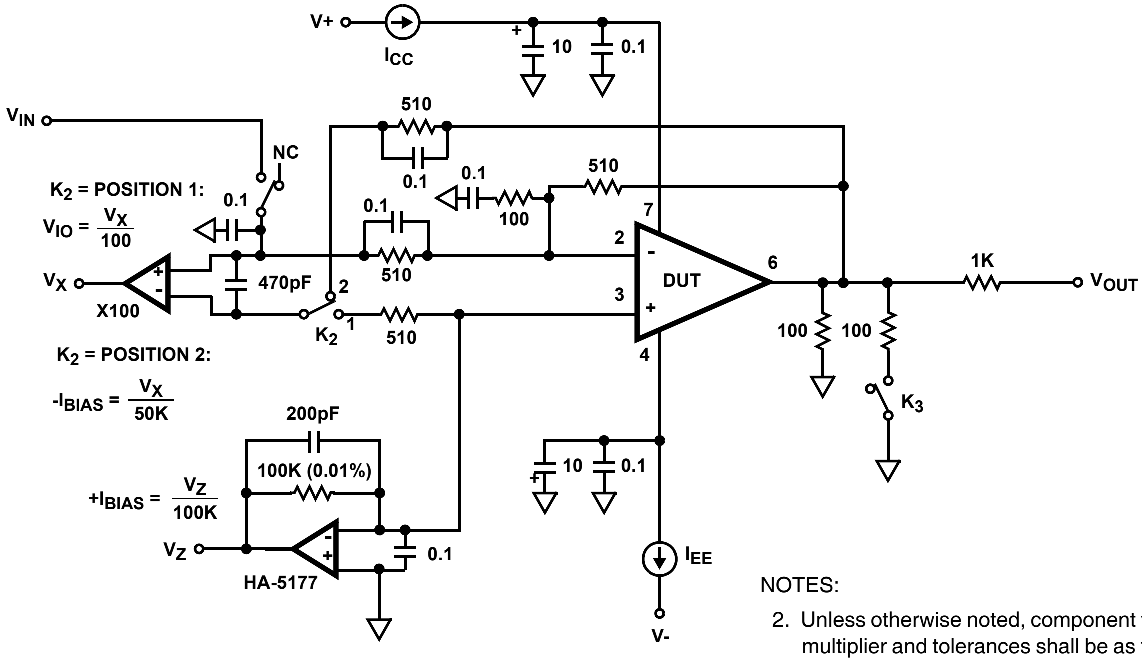


FIGURE 26. INPUT NOISE vs FREQUENCY

Test Circuit

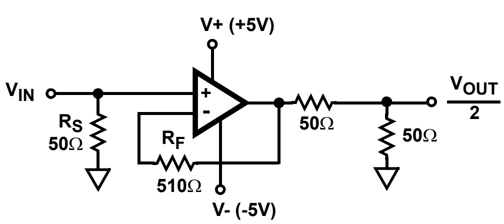


NOTES:

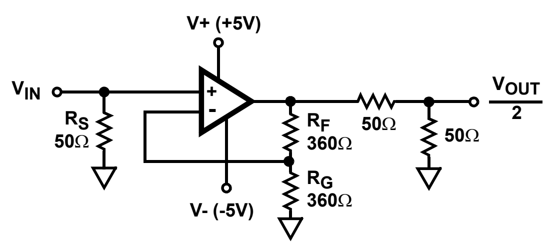
2. Unless otherwise noted, component value multiplier and tolerances shall be as follows:
   Resistors, Ω ±1%.
   Capacitors, μF ±10%
3. Chip Components Recommended.

Test Waveforms

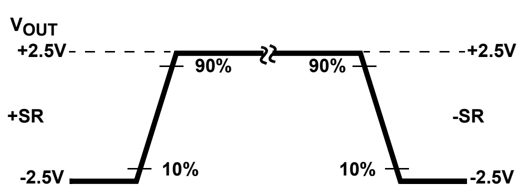
SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL PULSE RESPONSE



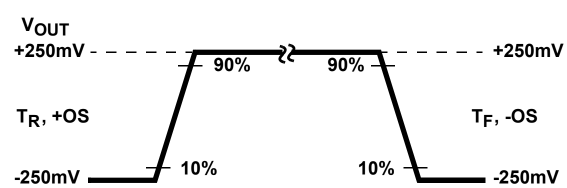
A_V = +1 TEST CIRCUIT



A_V = +2 TEST CIRCUIT



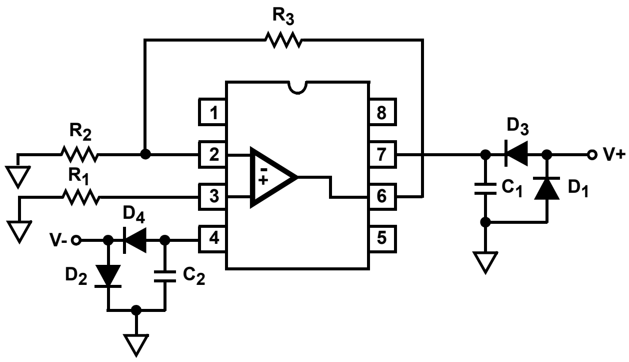
LARGE SIGNAL WAVEFORM



SMALL SIGNAL WAVEFORM

Burn-In Circuit

HS-1100RH CERDIP

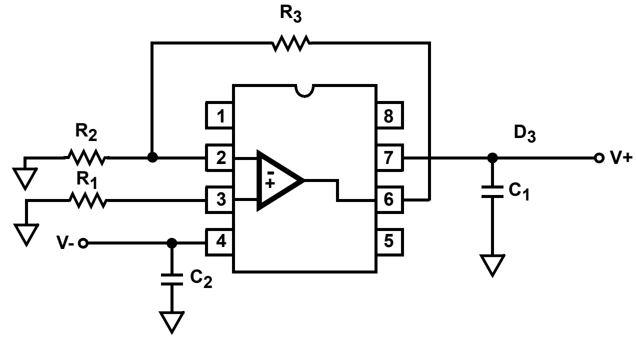


NOTES:

4. $R_1 = R_2 = 1k\Omega$, ±5% (Per Socket).
5. $R_3 = 10k\Omega$, ±5% (Per Socket).
6. $C_1 = C_2 = 0.01\mu F$ (Per Socket) or $0.1\mu F$ (Per Row) Min.
7. $D_1 = D_2$ = 1N4002 or Equivalent (Per Board).
8. $D_3 = D_4$ = 1N4002 or Equivalent (Per Socket).
9. V+ = +5.5V ±0.5V.
10. V- = -5.5V ±0.5V.

Irradiation Circuit

HS-1100RH CERDIP



NOTES:

11. $R_1 = R_2 = 1k\Omega$, ±5%.
12. $R_3 = 10k\Omega$, ±5%.
13. $C_1 = C_2 = 0.1\mu F$.
14. V+ = +5.5V ± 0.5V.
15. V- = -5.5V ± 0.5V.

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils ±1 mil
(1600μm x 1130μm x 483μm ±25.4μm)

INTERFACE MATERIALS:

Glassivation:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

Top Metallization:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

Substrate:

UHF-1, Bonded Wafer, DI

ASSEMBLY RELATED INFORMATION:

Substrate Potential (Powered Up):

Floating

ADDITIONAL INFORMATION:

Worst Case Current Density:

1.6×10^5 A/cm^2

Transistor Count:

52

Metallization Mask Layout

HS-1100RH