

Darlington Transistor

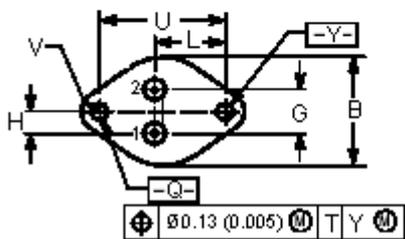
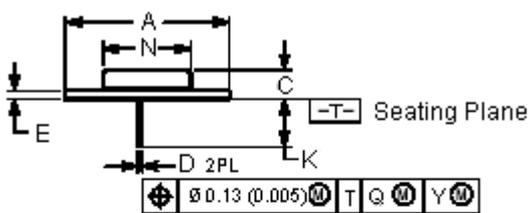


High - current complementary silicon transistors
For use output devices in complementary general purpose amplifier applications

Features:

- High DC current gain - $h_{FE} = 1,000$ (minimum) at $I_C - 20$ A dc
- Monolithic construction with built-in base emitter shunt resistor
- Junction temperature to $+200^\circ\text{C}$

(TO-3)

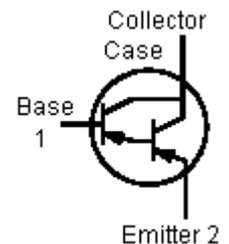


Style 1:
Pin 1. Base
2. Emitter
Collector (Case)

Dimensions	Minimum	Maximum
A	1.55 (39.37)	Reference
B	-	1.05 (26.67)
C	0.25 (6.35)	0.335 (8.51)
D	0.038 (0.97)	0.043 (1.09)
E	0.055 (1.4)	0.07 (1.77)
G	0.43 (10.92) BSC	
H	0.215 (5.46) BSC	
K	0.44 (11.18)	0.48 (12.19)
L	0.665 (16.89) BSC	
N	-	0.83 (21.08)
Q	0.151 (3.84)	0.165 (4.19)
U	1.187 (30.15) BSC	
V	0.131 (3.33)	0.188 (4.77)

Dimensions : Inches (Millimetres)

30 Amperes Darlington Power Transistors
Complementary Silicon
60 - 120 V, 200 W



(TO-3)
Case 1-07
Style 1

Maximum Ratings

Rating	Symbol	Value	Unit
Collector - Emitter Voltage	V_{CEO}	120	V dc
Collector - Base Voltage	V_{CB}		
Emitter - Base Voltage	V_{EB}		
Collector Current	I_C	30	A dc
Base Current	I_B	1	
Total Device Dissipation at $T_C = 25^\circ\text{C}$ Derate above 25°C at $T_C = 100^\circ\text{C}$	P_D	200 1.15	W W / $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200	$^\circ\text{C}$

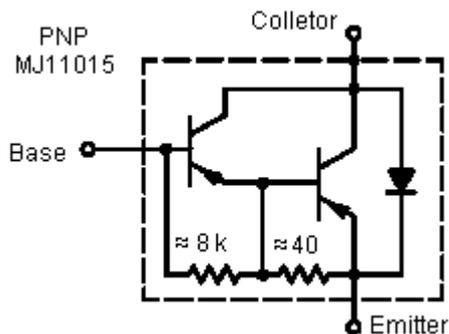
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Thermal Characteristics

Characteristics	Symbol	Maximum	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.17	$^{\circ}\text{C} / \text{W}$
Maximum Lead Temperature for Soldering Purposes for ≤ 10 Seconds	T_L	275	$^{\circ}\text{C}$

Stresses exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stresses above the recommended operating conditions may affect device reliability

Darlington Circuit Schematic



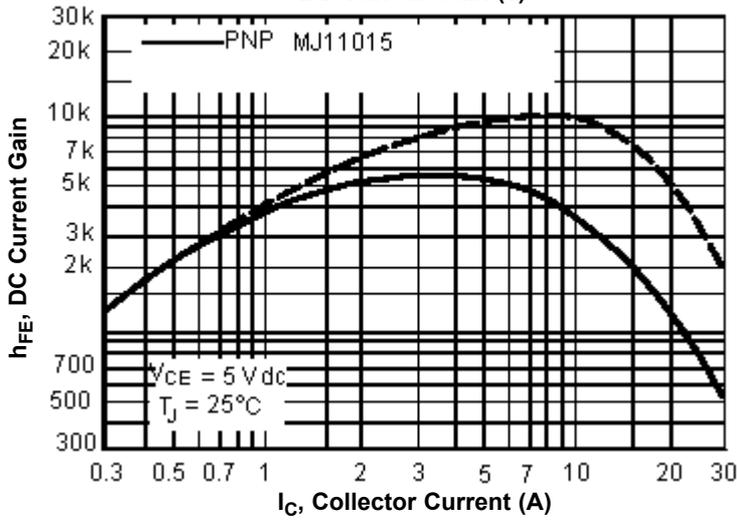
Electrical Characteristics ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Minimum	Maximum	Unit
Off Characteristics				
Collector - Emitter Breakdown Voltage (1) ($I_C = 100 \text{ mA dc}$, $I_B = 0$)	MJ11015 $V_{(BR)CEO}$	120	-	V dc
Collector - Emitter Leakage Current ($V_{CE} = 120 \text{ V dc}$, $R_{BE} = 1 \text{ k}\Omega$) ($V_{CE} = 120 \text{ V dc}$, $R_{BE} = 1 \text{ k}\Omega$, $T_C = 150^{\circ}\text{C}$)	MJ11015 I_{CER}	-	1 5	mA dc
Emitter Cut off Current ($V_{BE} = 5 \text{ V dc}$, $I_C = 0$)	I_{EBO}	-	5	
Collector - Emitter Leakage Current ($V_{CE} = 5 \text{ V dc}$, $I_B = 0$)	I_{CEO}	-	1	
On Characteristics (1)				
DC Current Gain ($I_C = 20 \text{ A dc}$, $V_{CE} = 5 \text{ V dc}$) ($I_C = 30 \text{ A dc}$, $V_{CE} = 5 \text{ V dc}$)	h_{FE}	1,000 200	- -	-
Collector - Emitter Saturation Voltage ($I_C = 20 \text{ A dc}$, $I_B = 200 \text{ mA dc}$) ($I_C = 30 \text{ A dc}$, $I_B = 300 \text{ mA dc}$)	$V_{CE(sat)}$	-	3 4	V dc
Base - Emitter Saturation Voltage ($I_C = 20 \text{ A dc}$, $I_B = 200 \text{ mA dc}$) ($I_C = 30 \text{ A dc}$, $I_B = 300 \text{ mA dc}$)	$V_{BE(sat)}$	-	3.5 5	
Dynamic Characteristics				
Current-Gain Bandwidth Product ($I_C = 10 \text{ A}$, $V_{CE} = 3 \text{ V dc}$, $f = 1 \text{ MHz}$)	h_{fe}	4	-	MHz

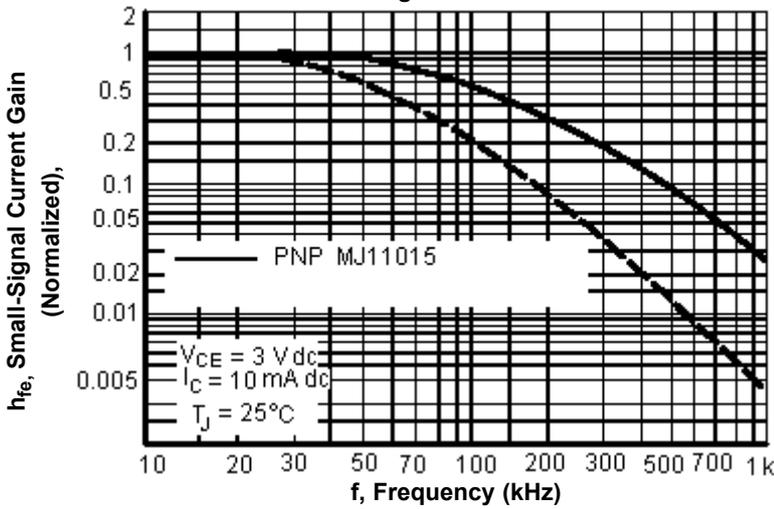
(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$

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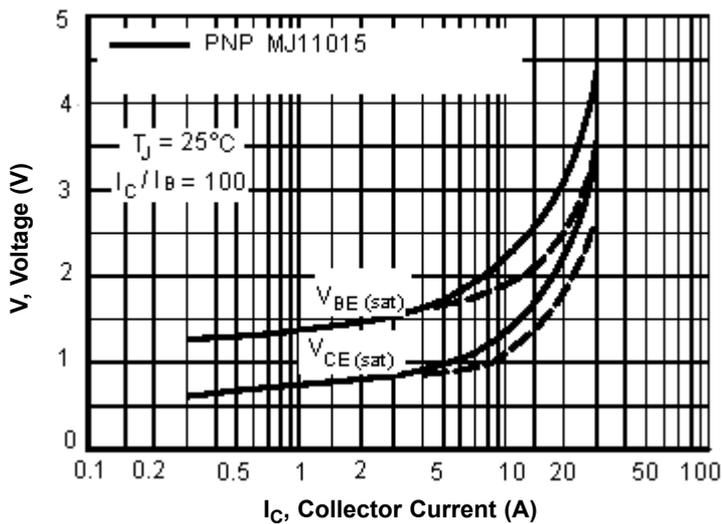
DC Current Gain (1)



Small-Signal Current Gain

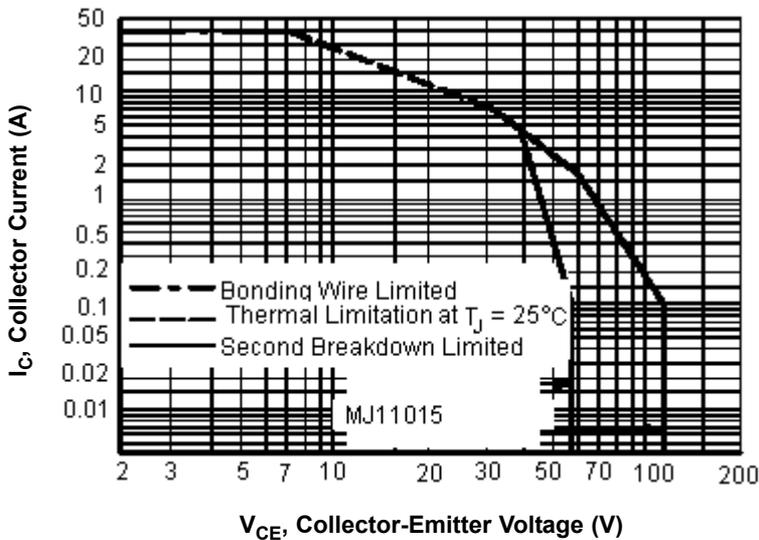


"On" Voltage (1)



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Active Region DC Safe Operating Area



There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operations e.g., the transistor must not be subjected to greater dissipation than the curves indicate. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown

Part Number Table

Description	Part Number
Darlington Transistor, TO-3	MJ11015

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