



APPLICATION NOTE

Estimated Junction Temperature Rise due to Power Dissipation during Operation

ATA6843/ATA6844

Introduction

This document helps to calculate the junction temperature based on the power dissipation to prevent temperature shut-down during normal operation.

Preface

Normal operation of the Atmel® ATA6843/ATA6844 may subject the devices power dissipation that is exceeding typical values. The devices incorporate an automatic shut-down feature to protect against excessive junction temperature rise which can in turn result in overheating and device failure. This application note explains how to calculate the power dissipated in the device during normal operation to maintain a safe power consumption margin that avoids device shut-down caused by temperature.

1. Basic Theory

1.1 Junction Temperature

The junction temperature can be calculated using the following formula.

$$1. \quad T_J = T_A + P_{TOT} R_{thja}$$

Where:

T_J [°C] = Junction temperature (see note 1)

T_A [°C] = Maximum ambient temperature

P_{TOT} [W] = The total dissipated device power

R_{thja} [K/W] = Thermal resistance from junction to ambient (see note 2)

- Notes:
1. To simplify the calculation it is assumed that the temperature is equally distributed on the chip. A more accurate model of the chip's temperature distribution including hot spots or temporary effects is beyond the scope of this note.
 2. Although, thermal resistance is specified in the datasheet as R_{thja} , it strongly depends on board design (layout, applied heat sinks, etc.) and might differ from the given value.

1.2 Total Dissipated Power (P_{TOT})

With this simplified equation (see note 1) P_{TOT} can be calculated as the sum of the average power dissipated in the power section, P_{PBAT} , and the average power dissipated in the low-power section, P_{VBAT} .

$$2. \quad P_{TOT} = P_{VBAT}(I_{VBAT}, I_{Load}, V_{VBAT}, V_{VCC}) + P_{PBAT}(\eta_{CP}, I_{HS}, I_{LS}, V_{PBAT})$$

1.2.1 Dissipated Power in Low-power Section (P_{VBAT})

P_{VBAT} consists of the power dissipated in the VCC regulator's passive device, P_{VCC} and the power consumed by the internal control circuitry, P_{CONTR} . P_{VCC} is a function of the voltage drop across the regulator's passive device and the average load current (I_{Load}) drawn from the VCC pin. P_{CONTR} depends on voltage VBAT and the average operating current of the control circuitry block, I_{VBAT} (see datasheet, parameter 1.1).

$$3. \quad P_{VBAT}(I_{VBAT}, I_{Load}, V_{VBAT}, V_{VCC}) = P_{VCC}(I_{Load}, V_{VBAT}, V_{VCC}) + P_{CONTR}(I_{VBAT}, V_{VBAT})$$

$$4. \quad P_{VCC}(I_{Load}, V_{VBAT}, V_{VCC}) = I_{Load}(V_{VBAT} - V_{VCC})$$

$$P_{CONTR}(I_{VBAT}, V_{VBAT}) = I_{VBAT} V_{VBAT}$$

1.2.2 Dissipated Power in Power Section (P_{PBAT})

P_{PBAT} mainly consists of the average power dissipated by the charge pump and the drivers, P_{CP} , and the used control circuitry, P_{PBAT_DC} . In equation 5, $P_{PBAT_DC} \ll P_{CP}$ and can be neglected. This simplifies to the following:

$$5. \quad P_{PBAT} = P_{CP} + P_{PBAT_DC} \approx P_{CP} = \frac{V_{PBAT}}{\eta_{CP}} (I_{HS} + I_{LS})$$

I_{HS} and I_{LS} = the average currents sourced by the high-side drivers and low-side drivers, respectively

$$6. \quad I_{HS} = f_0 n_{HS} Q_{HS}$$

$$I_{LS} = f_0 n_{LS} Q_{LS}$$

The high and low-side currents are functions of the switching frequency f_0 , the average gate charge to be transferred to switch the respective external NMOS transistor Q_{HS}, Q_{LS} , and the number of gates that are switched in each switch period (n_{HS}, n_{LS}). η_{CP} stands for charge pump efficiency and for Atmel® ATA6843/ATA6844 which includes a two-stage charge pump $\eta_{CP} \approx 0.3$.

While f_0 , n_{HS} and n_{LS} are application-specific, Q_{HS} and Q_{LS} are external NMOS transistor parameters. Combining equations 6 and 5 yields to:

$$7. \quad P_{PBAT} = V_{PBAT} \frac{f_0}{\eta_{CP}} (n_{HS} Q_{HS} + n_{LS} Q_{LS})$$

Thus, the total average power dissipation is:

$$8. \quad P_{\Sigma} = I_{\text{Load}} (V_{\text{VBAT}} - V_{\text{VCC}}) + I_{\text{VBAT}} V_{\text{VBAT}} + V_{\text{PBAT}} \frac{f_0}{\eta_{\text{CP}}} (n_{\text{HS}} Q_{\text{HS}} + n_{\text{LS}} Q_{\text{LS}})$$

Using equation 8 enables to calculate junction temperature and its shut-down margin.

2. Power Calculation Example

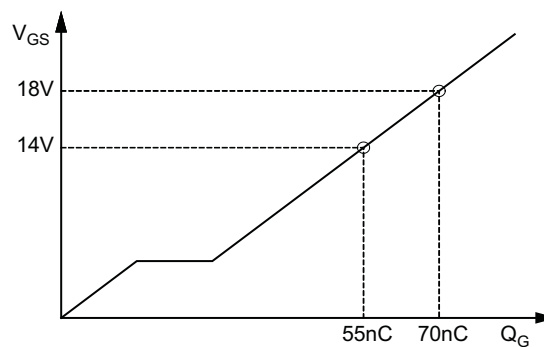
This chapter presents the power calculation for the ATA6843/ATA6844 when operating as a motor control gate driver in an H-bridge configuration. The entire power dissipation for the device is calculated with given operating conditions, which in turn results in the operating junction temperature. Device temperature shut-down can be calculated for a given device power vs. ambient operating temperature.

- $V_{\text{VCC}} = 5\text{V}$ and $I_{\text{Load}} = 40\text{mA}$
- $V_{\text{VBAT}} = V_{\text{PBAT}} = 18\text{V}$ (i.e., assuming that the maximum battery supply voltage is 18V)
- $f_0 = 20\text{kHz}$
- $n_{\text{HS}} = n_{\text{LS}} = 1$ (assuming one HS and one LS MOS transistor are switched per PWM period)

Although, all bridge transistors are congeneric, the transferred gate charges for the high and low-side MOS transistors are not equal. This is due to the different gate-source voltages being applied. The gate source voltage of the high-side devices is equal to $V_{\text{CPOUT}} - V_{\text{VBAT}}$ (datasheet parameter 6.1). The low-side gate-source voltage is set by the VG output (datasheet parameter 7.1). The actual gate charge can then be calculated as:

$Q_{\text{HS}} (V_{\text{CPOUT}} - V_{\text{PBAT}} = 18\text{V}) = 70\text{nC}$, and $Q_{\text{LS}} (V_{\text{VG}} = 14\text{V}) = 55\text{nC}$ (see Figure 2-1).

Figure 2-1. Gate-source Voltage versus Accumulated Gate Charge



Inserting the given values yields the following results:

$$P_{\text{VBAT}} = 646\text{mW}$$

$$P_{\text{PBAT}} = 150\text{mW}$$

$$P_{\Sigma} = 796\text{mW}$$

Assuming $R_{\text{thja}} = 25\text{K/W}$, the junction temperature increases to $\Delta T_J = P_{\Sigma} R_{\text{thja}} = 20\text{K}$.

Based on these assumptions ATA6843/ATA6844 would flag temperature prewarning (datasheet parameter 1.11) for $T_A \geq 150^\circ\text{C}$, and cause device shut-down for $T_A \geq 180^\circ\text{C}$ (datasheet parameter 1.14).

Further, the result shows that the total power dissipation and thus the self-heating is dominated by the load at the VCC output.

As shown in Figure 2-2, this example situation would neither change significantly if a different switching activity is required nor if VCC is set to 3.3V in conjunction with a smaller load current. In Figure 2-3 the power dissipation is plotted versus an accumulated gate charge that is needed to drive a HS NMOS transistor (gate charge for LS NMOS transistor is scaled accordingly). This figure clearly shows that the power dissipation in the power section begins to dominate only by applying very large external NMOS transistors.

Figure 2-2. Power Dissipation versus VCC Load Current

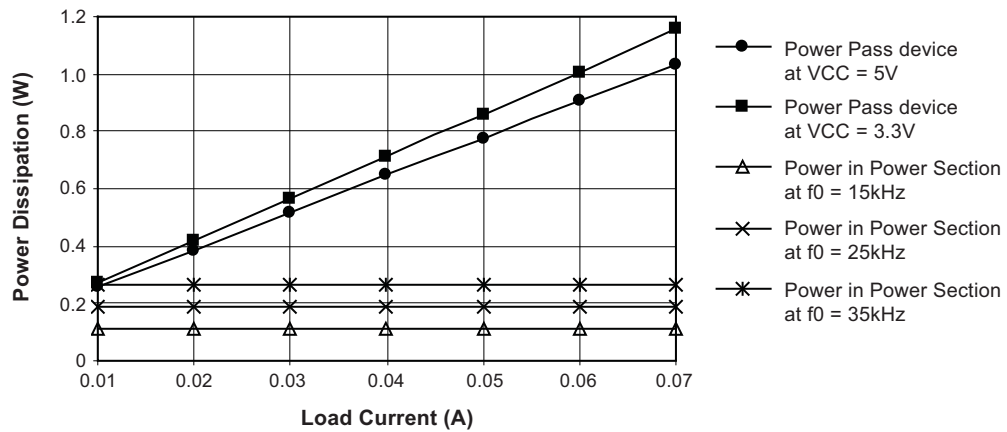
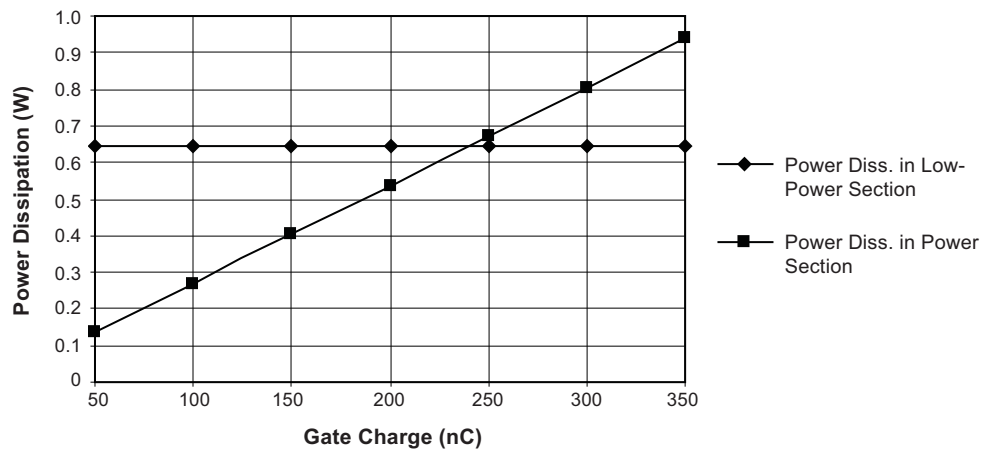


Figure 2-3. Power Dissipation versus Accumulated Gate Charge



3. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9181D-AUTO-04/15	• Put document in the latest template



Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA T: (+1)(408) 441.0311 F: (+1)(408) 436.4200 | www.atmel.com

© 2015 Atmel Corporation. / Rev.: 9181D-AUTO-04/15

Atmel®, Atmel logo and combinations thereof, Enabling Unlimited Possibilities®, and others are registered trademarks or trademarks of Atmel Corporation in U.S. and other countries. Other terms and product names may be trademarks of others.

DISCLAIMER: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. EXCEPT AS SET FORTH IN THE ATMEL TERMS AND CONDITIONS OF SALES LOCATED ON THE ATMEL WEBSITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS AND PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and products descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

SAFETY-CRITICAL, MILITARY, AND AUTOMOTIVE APPLICATIONS DISCLAIMER: Atmel products are not designed for and will not be used in connection with any applications where the failure of such products would reasonably be expected to result in significant personal injury or death ("Safety-Critical Applications") without an Atmel officer's specific written consent. Safety-Critical Applications include, without limitation, life support devices and systems, equipment or systems for the operation of nuclear facilities and weapons systems. Atmel products are not designed nor intended for use in military or aerospace applications or environments unless specifically designated by Atmel as military-grade. Atmel products are not designed nor intended for use in automotive applications unless specifically designated by Atmel as automotive-grade.