STEF05S

Datasheet

Electronic fuse for 5 V line

TSOT23-8L

Maturity status link
STEF05S

Features

- 5.7 V typical output overvoltage clamp
- Absolute maximum voltage of 25 V
- Adjustable current limit
- Thermal protection
- Input undervoltage lockout
- Low inrush current during startup
- Integrated 40 mΩ Power FET
- En/fault pin
- Adjustable slew rate for output voltage
- TSOT23-8L package
- Latch (STEF05S) or auto-retry (STEF05SA) versions

Applications

- Hard disk and SSD drives
- Hard disk array
- Hot-swap board
- Hot-plug protection

Description

The STEF05S is an integrated electronic fuse optimized for monitoring the 5 V DC power lines.

When connected in series to the main power rail, it is able to precisely detect and react to overcurrent and overvoltage conditions.

When an overload condition occurs, the device limits the output current to a safe value defined by the user. If the anomalous overload condition persists, the device goes into an open state, disconnecting the load from the power supply.

In case of overvoltage on the input, the device regulates the output to a preset safe value.

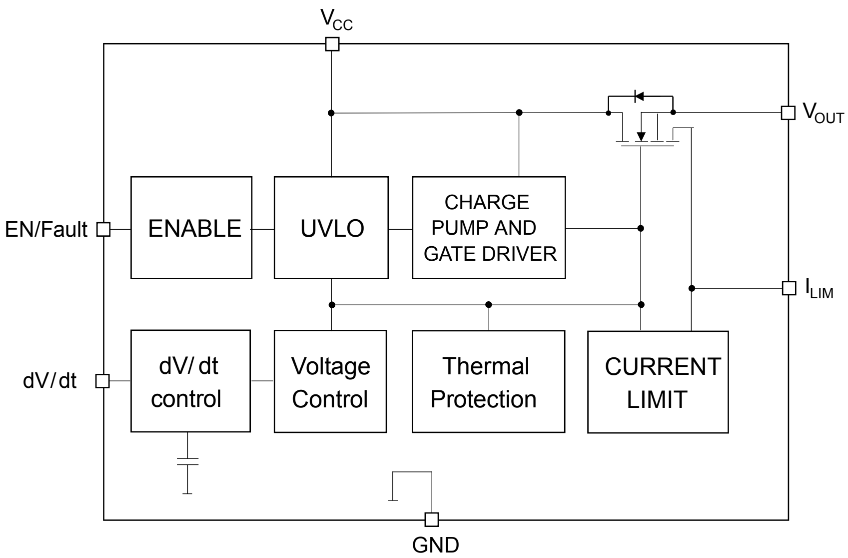
Undervoltage lockout prevents the load from malfunction, keeping the device off if the rail voltage is too low.

The STEF05S features the adjustable turn-on slew rate, which is useful to keep the inrush current under control during startup and hot-swap operations.

The STEF12S is a companion chip for the 12 V rails, useful to implement a complete power rail control in data-storage applications.

1 Diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connection (top view)

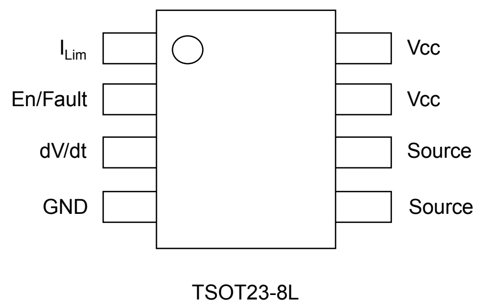


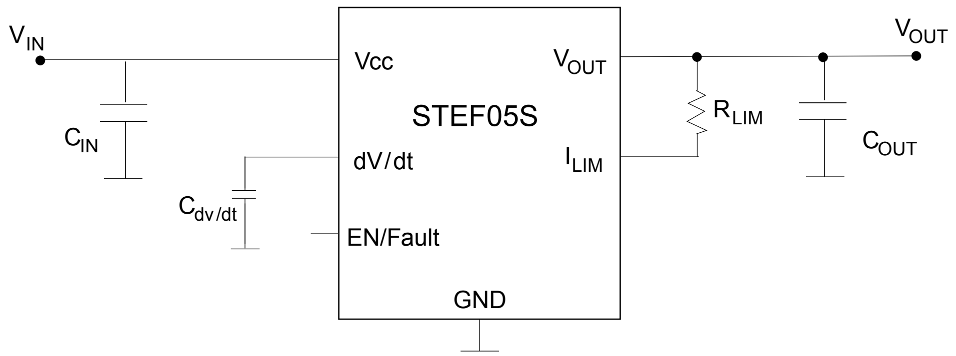
Table 1. Pin description

Pin #	Symbol	Function
1	I_{Lim} (1)	An R_{Lim} resistor between this pin and the Source pin sets the overload and short-circuit current limit levels.
2	En/Fault	The En/Fault pin is a tri-state, bi-directional interface. During normal operation the pin must be left floating, or it can be used to disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin goes into an intermediate state to signal a monitor circuit that the device is in thermal shutdown. It can be connected to another device of this family to cause a simultaneous shutdown during thermal events.
3	dV/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn-on. The internal capacitor allows a ramp-up time of around 1.35 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional capacitor is not required, this pin should be left open.
4	GND	Ground connection.
5 - 6	Source/V_{OUT}	Connected to the source of the internal power MOSFET and to the output terminal of the fuse.
7 - 8	V_{CC}	Positive input voltage of the eFuse.

1. *Important: missing or shorted R_{Lim} causes current limit circuit malfunction and may lead to device damage.*

3 Typical application

Figure 3. Typical application circuit



4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Positive power supply voltage	-0.3 to 25	V
V_{OUT}/source [(1)]	Output voltage	-0.3 to Vcc+0.3	V
I_{Lim}	Current limit resistor pin voltage	-0.3 to 25	V
En/fault	En/Fault pin voltage	-0.3 to 7	V
dv/dt	dv/dt pin voltage	-0.3 to 7	V
T_{op}	Operating junction temperature range	-40 to 125	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 s	260	°C
HBM	ESD protection - Human Body Model	2	kV
CDM	ESD protection - Charged device model (TSOT23-8L package)	500	V

1. *Fast V_{in} voltage dip due to input power removal may cause high reverse current flow through the internal body diode, that may damage the device.*
2. *The thermal limit is set above the maximum thermal rating. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	140	°C/W
R_{thJC}	Thermal resistance junction-case	35	°C/W

1. *Based on JESD51-7, 4-layer PCB.*

Table 4. Recommended operating condition

Symbol	Parameter	Value	Unit
V_{CC}	Operating power supply voltage	3.5 to 5.5	V
I_D	Maximum continuous current T_A = 25 °C	3.5	A
C_{IN}	Suggested input capacitor	1	µF
C_{OUT}	Minimum output capacitor	1	µF

1. *The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J(MAX)}$, the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A and can be estimated by: $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation produces overheating that may cause thermal shutdown.*

5 Electrical characteristics

Table 5. **Electrical characteristics V_{CC} = 5 V, $V_{En/Fault}$ = 5 V, C_I = 10 µF, C_O = 10 µF, T_J = 25 °C (unless otherwise specified).**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Under/Overvoltage protection						
V_{Clamp}	Output clamping voltage	V_{CC} = 8 V	5.5	5.7	5.9	V
V_{UVLO}	Undervoltage lockout	Turn-on, voltage rising	2.85	2.9	2.95	V
V_{Hyst}	UVLO hysteresis			0.15		V
Power MOSFET						
t_{dly}	Delay time	Enabling of chip to soft-start beginning (10% of V_{OUT}), no $C_{dv/dt}$		350		µs
R_{DSon}	On-resistance	T_J = 25 °C		40	50	mΩ
		T_J = 85 °C		48		
V_{OFF}	Off state output voltage	V_{CC} = 18 V, V_{GS} = 0, R_L = infinite		1	10	mV
Current Limit						
I_{Short}	Short-circuit current limit	R_{Lim} = 22 Ω		2		A
I_{Lim}	Overload current limit	R_{Lim} = 22 Ω		5.2		A
I_{Short}	Short-circuit current limit	R_{Lim} = 49.9 Ω		1.1		A
I_{Lim}	Overload current limit	R_{Lim} = 49.9 Ω		3.2		A
dv/dt circuit						
dv/dt	Output voltage ramp time	From 10% to 90% of V_{OUT}, no Cdv/dt		1.35		ms
En/Fault						
V_{IL}	Low level input voltage	Output disabled			0.5	V
$V_{I(INT)}$	Intermediate level input voltage	Thermal fault, output disabled	1.2	1.3	1.45	V
V_{IH}	High level input voltage	Output enabled	2.55			V
$V_{I(MAX)}$	High state maximum voltage			4.9		V
I_{IL}	Low level input current (sink)	$V_{En/Fault}$ = 0 V		-20	-50	µA
I_I	High level leakage current for external switch	$V_{En/Fault}$ = 5 V			1	µA
	Maximum fan-out for fault signal	Total numbers of chips that can be connected to this pin for simultaneous shutdown			3	Units
Current consumption						
I_{Bias}	Bias current	Device operational		0.37		mA
		Thermal shutdown		0.16		
		Off mode, $V_{En/Fault}$ = 0 V		0.12		
Thermal protection						
T_{SHDN}	Thermal shutdown			165		°C
	Hysteresis			20		

1. *Pulsed test.*
2. *Guaranteed by design and correlation but not tested in production.*

6 Application information

6.1 Turn-on and soft startup feature

When the input voltage is applied, the En/Fault pin goes up to the high state, and the internal control circuitry is enabled.

After an initial delay time of typically 350 µs, the output voltage is ramped up with a slope defined by the internal dv/dt circuitry. If no additional capacitor is connected to the dv/dt pin, the ramp-up time (V_{OUT} from 10% to 90%) is around 1.35 ms.

Connecting a capacitor between the $C_{dv/dt}$ pin and GND allows the modification of the output voltage ramp-up time. Given the desired time interval Δt during which the output voltage goes from zero to its maximum value, the capacitance to be added on the $C_{dv/dt}$ pin can be calculated using the following theoretical formula.

$$\Delta t\ [ms] = 1.35 + C_{dv/dt}\ [pF] \times 0.03 \quad (1)$$

Figure 4. Delay time and V_{OUT} ramp-up time

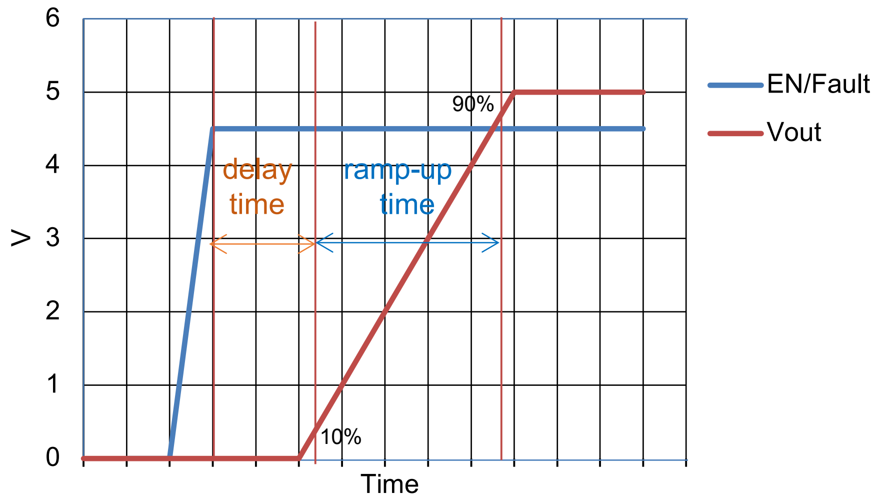


Table 6. Rise time vs. C_{dvdt}

C_{dvdt} (pF)	0	22	33	47	100	180	270	470	1000
Rise time (ms)	1.35	2	2.3	2.8	4.4	6.8	9.5	15.5	31.5

6.2 Maximum load at startup

Depending on supply voltage and load, it is possible that during startup the power dissipation is such that the maximum power protection is triggered and the output is shut down before the startup is complete. The EN/Fault signal is set according to Figure 5. En/Fault pin status.

In case of strong capacitive loads, the total start-up time may be longer than the programmed start-up time, since it is dependent also on the limitation current, the output load and the output capacitance value. In such a situation, the foldback current limit could activate, so that the startup is longer or eventually interrupted by the intervention of thermal protection. To avoid this occurrence, a longer start-up time should be set by the appropriate selection of the $C_{dv/dt}$ capacitor.

6.3 Normal operating conditions

The STEF05S behaves like a mechanical fuse, supplying the circuitry on its output with the same voltage shown at its input, with a small voltage fall due to the internal N-channel MOSFET R_{DSOn}.

6.4 Output voltage clamp

This internal protection circuit clamps the output voltage to a maximum safe value, typically 5.7 V, if the input voltage exceeds the V_{CLAMP} threshold. In this condition the device regulates the output voltage, therefore power dissipation increases. Thermal shutdown can occur if the overvoltage persists.

6.5 Current limiting

During operation, if the load current reaches the I_{LIM} overload threshold, an overload is detected. The current limiting circuit reduces the conductivity of the power MOSFET, in order to clamp the output current at the I_{SHORT} value. The overload threshold and current limit can be customized by means of the limiting resistor R_{Lim} Figure 3.

As shown in Figure 1, the device uses an internal N-channel sense FET with a fixed ratio, to monitor the output current and limit it at the level set by the user.

The R_{Lim} value for achieving the requested current limitation can be selected by using the following table, together with the graph in Figure 10 and Figure 11. Higher resistor values can be used, but due to the current limit trend shown in the graphs previously mentioned, the minimum values of I_{LIM} and I_{SHORT} are asymptotically limited.

Table 7. I_{Lim} / I_{Short} vs. R_{Lim}

R_{Lim} (Ω)	22	30	39	50	100	200	300
I_{Lim} (A)	5.2	4.2	3.55	3.2	2.1	1.6	1.4
I_{Short} (A)	2	1.6	1.3	1.1	0.55	0.3	0.2

Note: Missing or shorted R_{Lim} causes current limit circuit malfunction and may lead to device damage.

6.6 Thermal shutdown

If the device temperature exceeds the thermal shutdown threshold (T_{SHDN}), typically 165 °C, the power MOSFET is turned off and the load disconnected.

On the STEF05S latch version the EN/Fault pin of the device is automatically set to an intermediate voltage (typically 1.3 V), in order to signal the overtemperature event to the system controller.

The device can be reset from this condition either by cycling the supply voltage or by pulling down the EN pin below the V_{il} threshold and then releasing it.

On the auto-retry version (STEF05SA), the EN/Fault pin is set to a low logic level and the auto-retry circuit attempts to restart the device with soft-start once the die temperature is reduced to 145 °C typ. (165 °C minus the hysteresis value, 20 °C typ.).

6.7 En/Fault pin

The EN/Fault pin has the dual function of controlling the output of the device and providing information about the device status to the application. A simplified diagram of this circuit is depicted in Figure 6.

When it is used as a standard Enable pin, it can be connected to an external open-drain or open-collector device. In this case, when it is pulled at low logic level, it turns the output of the eFuse off.

If this pin is left floating, since it has internal pull-up circuitry, the eFuse is turned ON.

On the STEF05S (latch version), in case of thermal fault, the pin is pulled to an intermediate state (Figure 5). This signal can be provided to a monitor circuit, informing it that a thermal shutdown has occurred, or it can be directly connected to the EN/Fault pins of other eFuse devices on the same application in order to achieve a simultaneous enable/disable feature.

When a thermal fault occurs, the device can be reset either by cycling the supply voltage or by pulling down the Enable pin below the V_{il} threshold and then releasing it.

On the STEF05SA auto-retry version, once the thermal shutdown is triggered, the EN/Fault pin of the device is set to low state. It goes back to high level once the auto-retry occurs.

Figure 5. En/Fault pin status

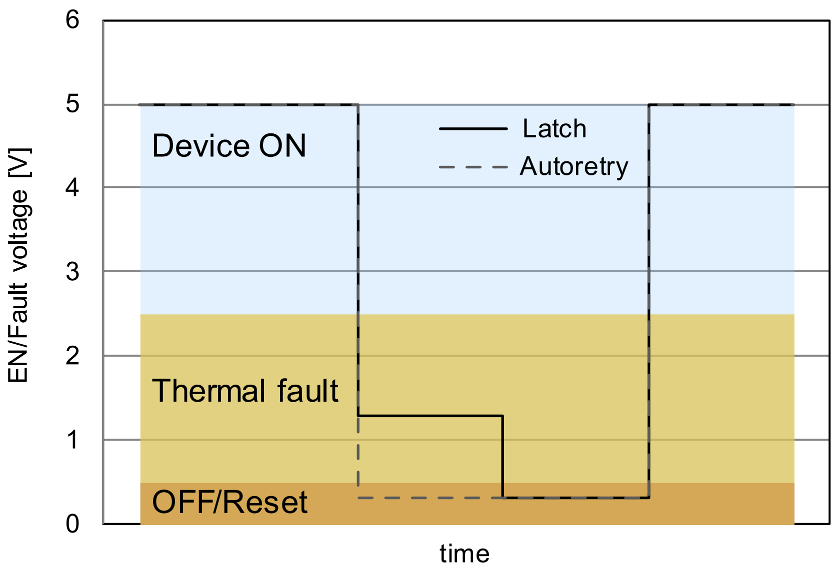
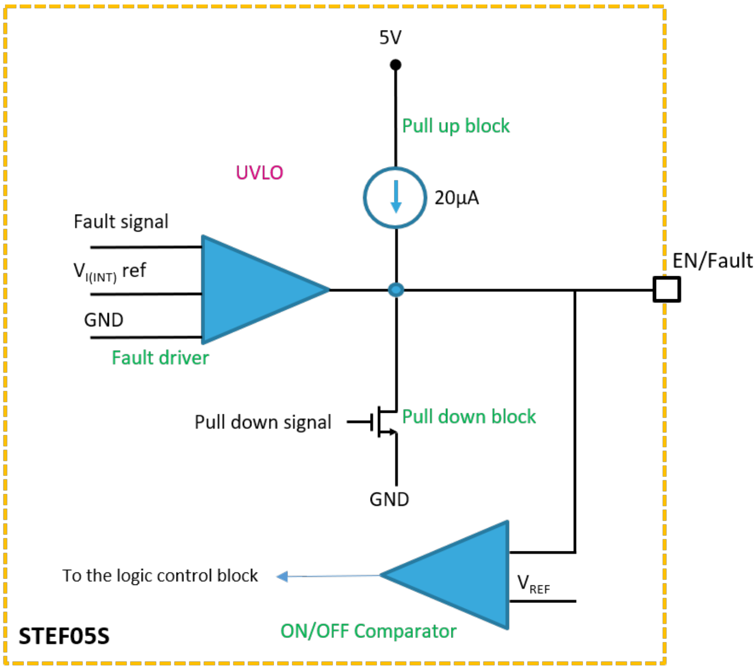


Figure 6. EN/Fault driver circuit



6.8 Application suggestions and PCB layout guidelines

Input and output capacitors are mandatory to guarantee device control loop stability and reduce the transient effects of stray inductances which may be present on the input and output power paths. In fact, when the STEF05S interrupts the current flow, input inductance generates a positive voltage spike on the input, and output inductance generates a negative voltage spike on the output.

To reduce the effects of such transients, a C_{IN} capacitor of at least 1 µF is recommended between the input pin and GND, and located as close as possible to the device.

For the same reason, a C_{OUT} capacitor of at least 1 µF must be connected at the output port.

When the device is powered by a power line made up of very long wires, the input inductance is higher than few µH, so the input capacitor should be increased in order to guarantee the proper operation of the device.

It is suggested to provide for additional protections and methods for addressing these transients, such as:

- Minimizing inductance of the input and output tracks
- TVS diodes on the input to absorb inductive spikes, see Figure 7
- Schottky diode on the output to absorb negative spikes, see Figure 7
- Combination of ceramic and electrolytic capacitors on the input and output

Fast input voltage dips due to input power removal may cause high reverse current flow through the internal body diode, that may lead to malfunction or damage the device.

In general, any application condition that may lead to an output voltage higher than input voltage, as per Table 2. Absolute maximum ratings, should be avoided.

In those applications where this kind of condition exists, it is recommended to protect the device by adding external circuits as:

- Schottky diode connected in anti-parallel configuration with the eFuse power switch to drive any reverse current outside the eFuse's intrinsic body diode (see Figure 8.).
- Diode in series to the power path.

Figure 7. **External protections against inductive voltage spikes**

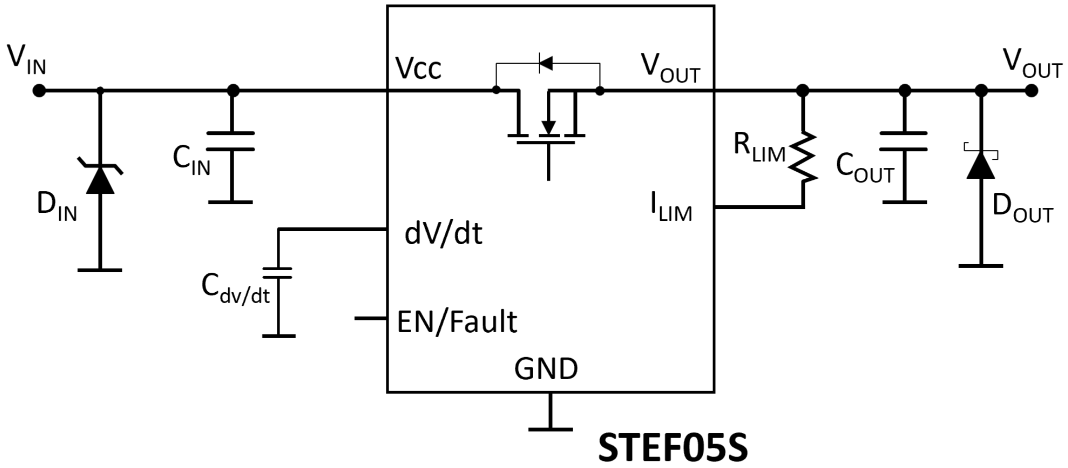
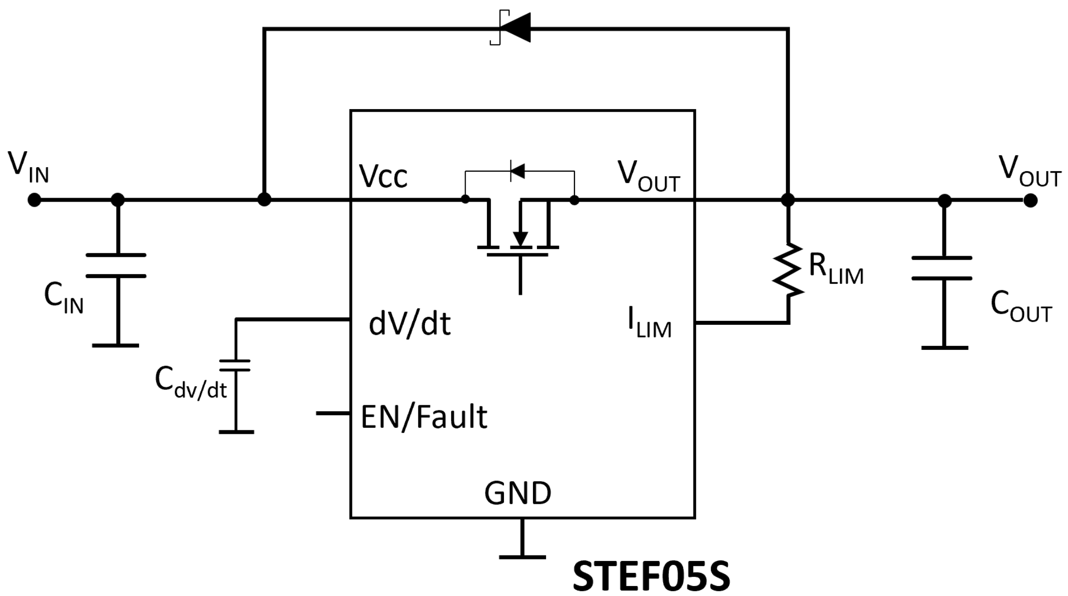


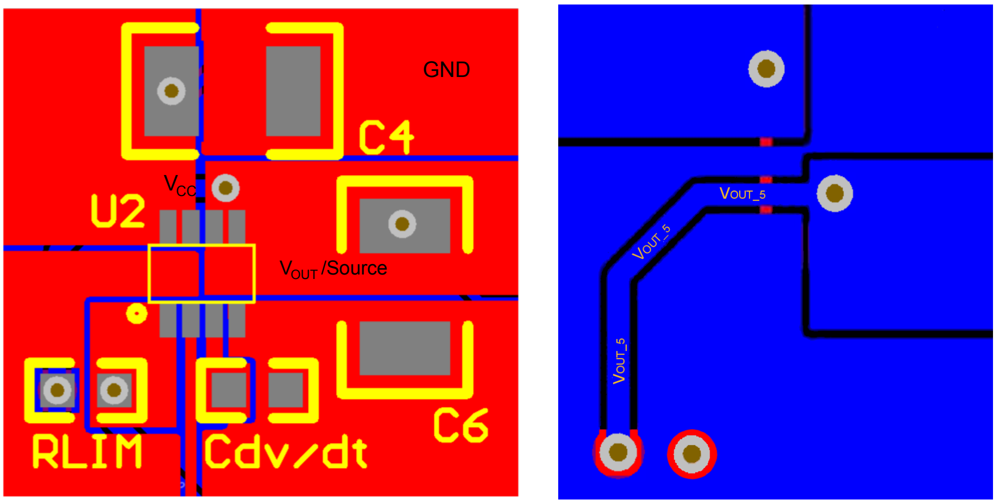
Figure 8. **External diode to address reverse current flow**



The PCB layout is critical for a stable and reliable operation. Refer to the typical PCB layout example shown in Figure 9 and to the following guidelines:

- Define the high current input and output copper traces as short as possible and adequately sized to sustain at least the overload current.
- Locate the R_{Lim} resistor close to the I_{Lim} pin and connect the other terminal of the component to V_{OUT} with the shortest possible trace. In fact, parasitic effects on the R_{Lim} connection trace can affect the current limit accuracy.
- Locate the Cdv/dt capacitor close to the dv/dt pin and connect the other terminal to GND with the shortest possible trace. Use low-leakage components for C_{dvdt}.
- The TSOT23-8L package dissipates thermal power mainly through the leads, so providing large enough copper areas around the PCB soldering pads is recommended.

Figure 9. **PCB layout example**



Top layer

Bottom layer

7 Typical characteristics

V_{CC} = 5 V, $V_{En/Fault}$ = floating, R_{Lim} = 22 Ω, C_{OUT} = 10 µF, $C_{dV/dt}$ = floating, T_A = 25 °C, unless otherwise specified.

Figure 10. I_{Lim} and I_{Short} vs. R_{Lim}

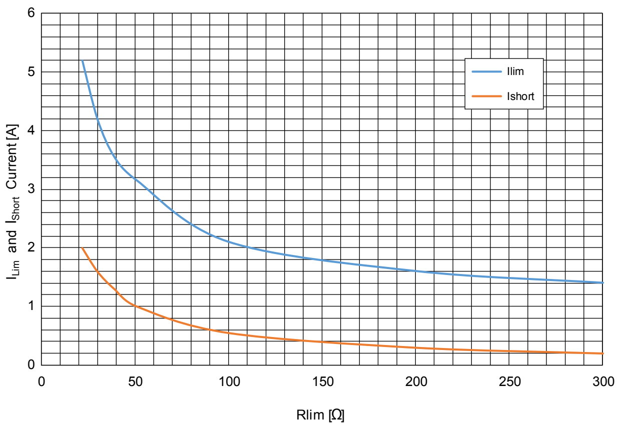


Figure 11. I_{Lim} and I_{Short} vs. R_{Lim} (magnification)

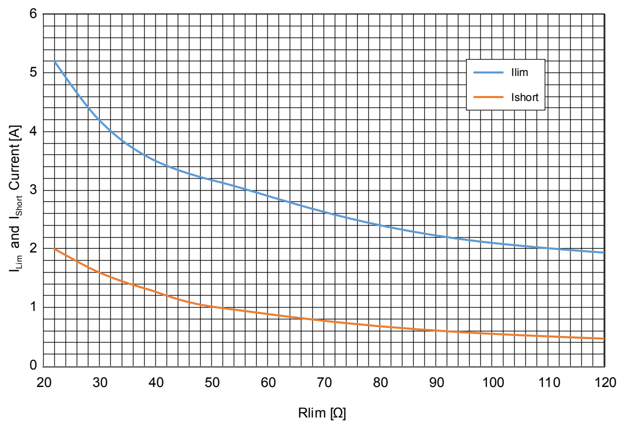


Figure 12. Bias current vs. temperature

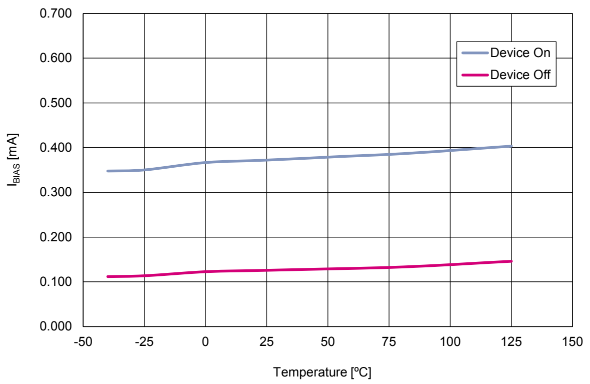


Figure 13. Bias current vs. temperature (thermal shutdown)

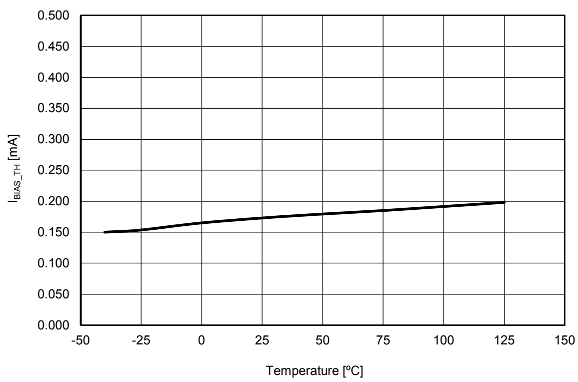


Figure 14. R_{DS_ON} vs. temperature

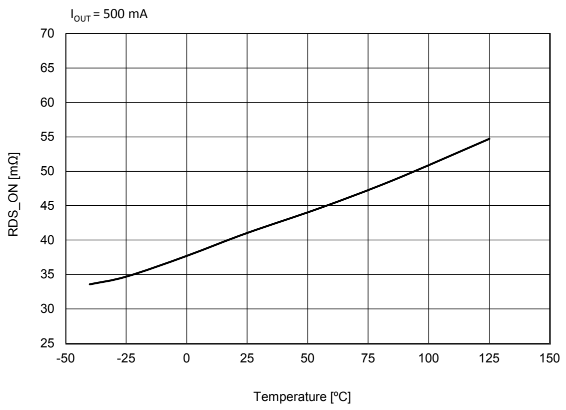


Figure 15. Clamping voltage vs. temperature

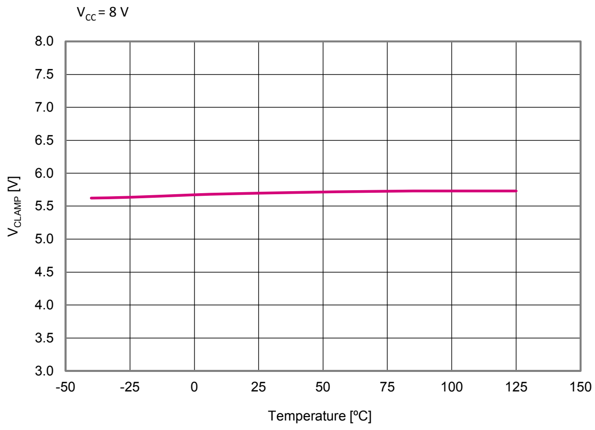


Figure 16. UVLO vs. temperature

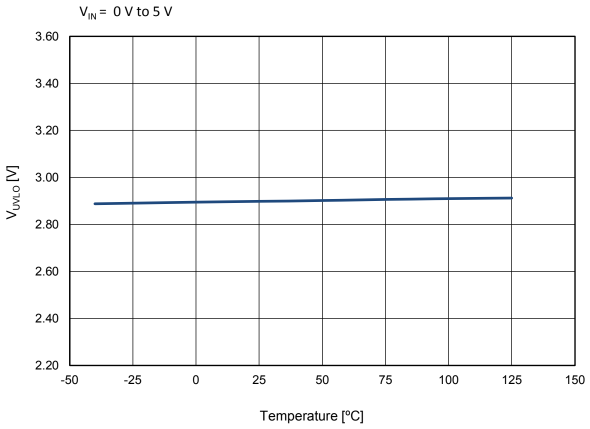


Figure 17. UVLO Hysteresis vs. temperature

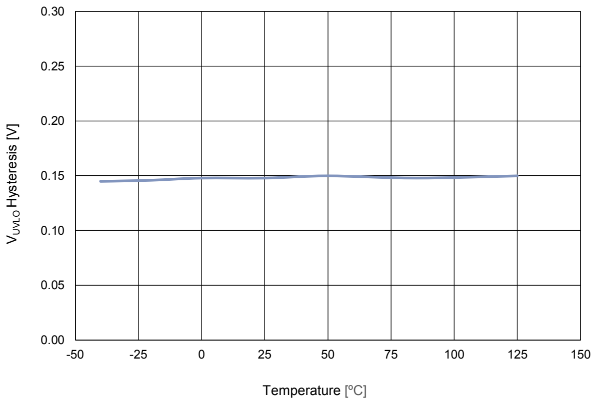


Figure 18. En/Fault pin thresholds vs. temperature

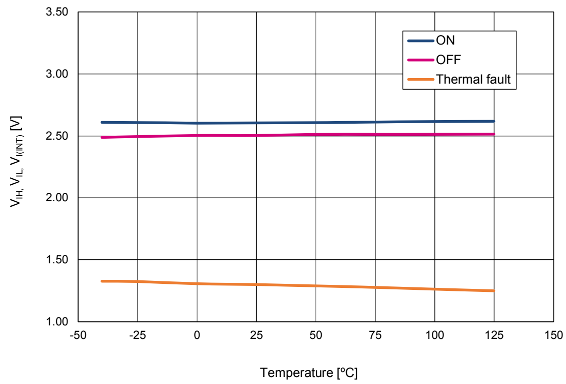


Figure 19. En/Fault pull-up voltage vs. temperature

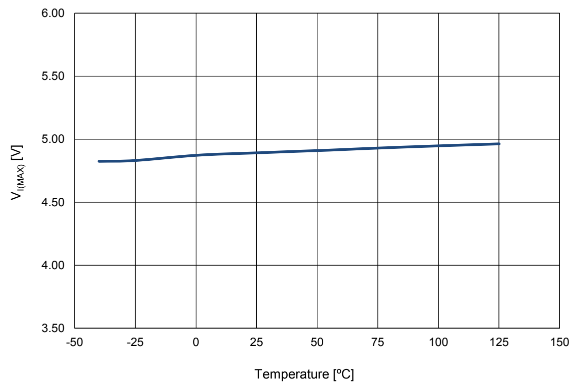


Figure 20. En/Fault pin current vs. temperature (En/Fault to GND)

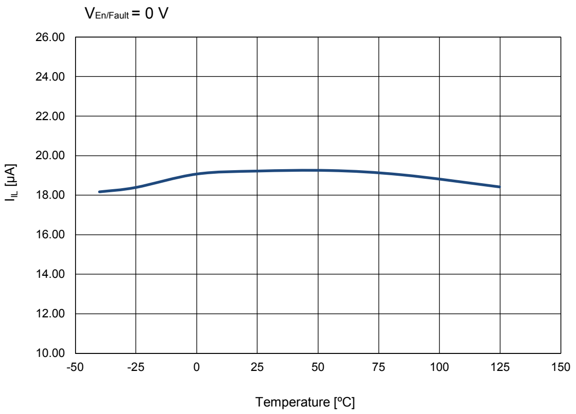


Figure 21. Soft-start time vs. temperature (no C_{dvdt})

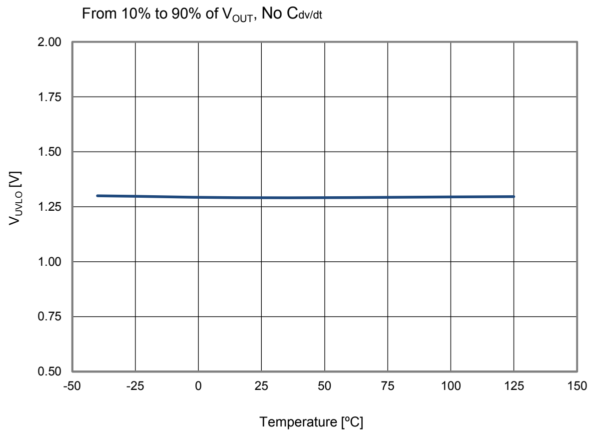
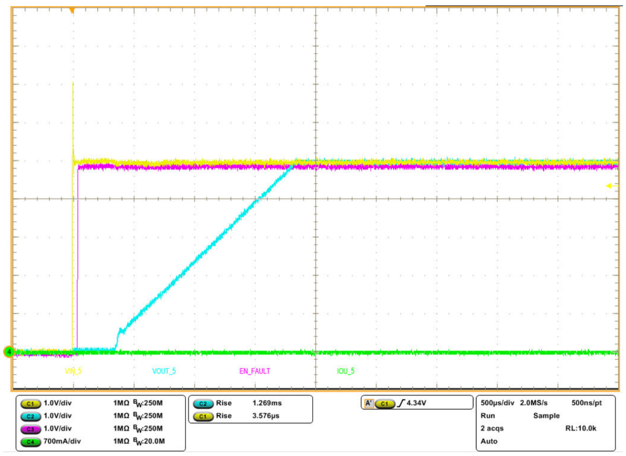
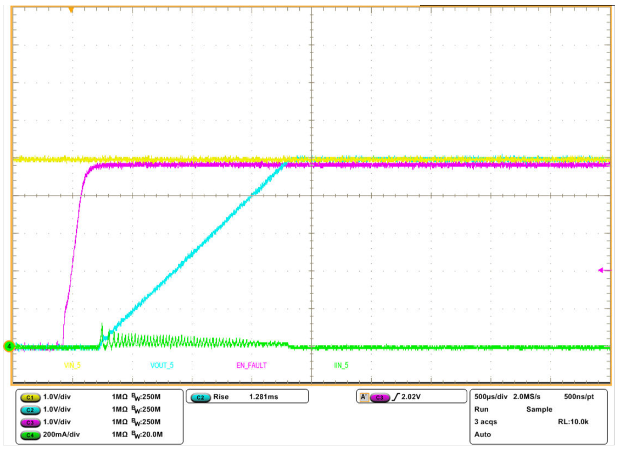


Figure 22. Startup via input voltage (No load)



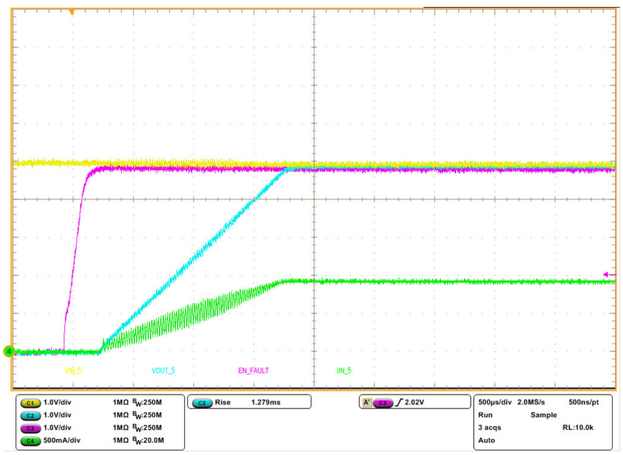
V_{IN} = from 0 V to 5 V, I_{OUT} = 0 mA , $C_{dV/dt}$ = floating, C_{IN} = 2.2 µF, C_{OUT} = 10 µF, R_{LIM} = 100 Ω

Figure 23. Startup via En/Fault pin (No load)



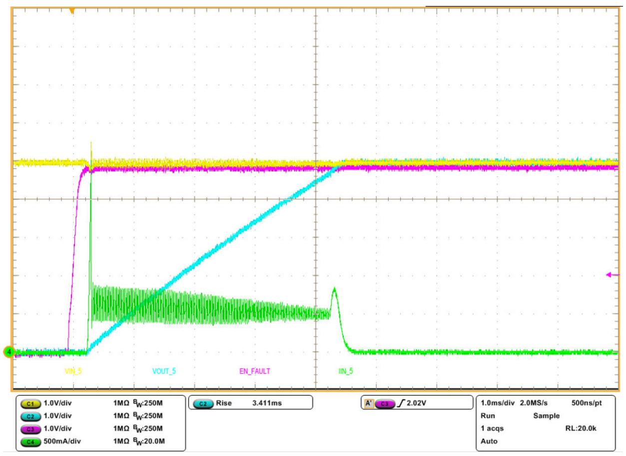
$V_{En/Fault}$ = from 0 V to floating, I_{OUT} = 0 mA , $C_{dV/dt}$ = floating, C_{IN} = 2.2 µF, C_{OUT} = 10 µF, R_{LIM} = 100 Ω

Figure 24. Startup via input voltage (5 Ω load)



V_{IN} = from 0 V to 5 V, R_{LOAD} = 5 Ω, $C_{dV/dt}$ = floating, C_{IN} = 2.2 µF, C_{OUT} = 10 µF, R_{LIM} = 100 Ω

Figure 25. Startup via En/Fault (C_{OUT} = 470 µF)

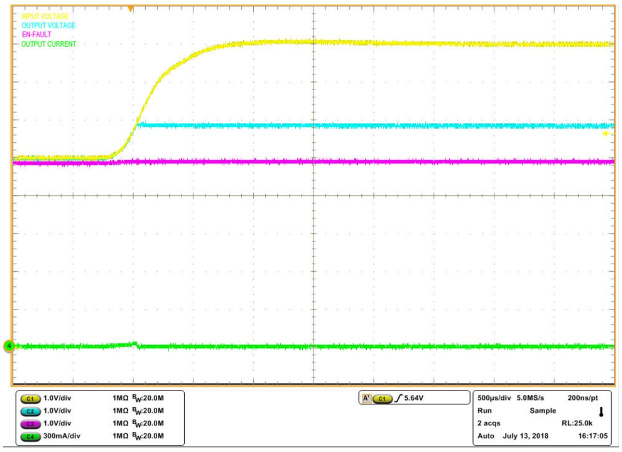


V_{IN} = from 0 V to 5 V, No load, $C_{dV/dt}$ = floating, C_{IN} = 2.2 µF, C_{OUT} = 470 µF, R_{LIM} = 100 Ω

Figure 26. Startup into voltage clamp

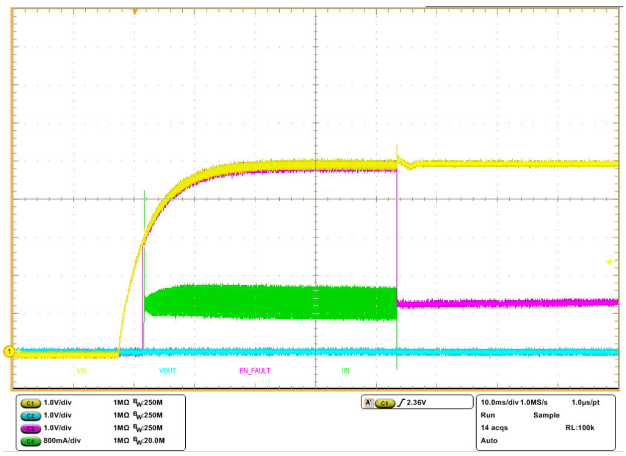
V_{IN} = from 0 V to 8 V, No load, $C_{dV/dt}$ = floating, C_{IN} = 2.2 µF, C_{OUT} = 10 µF, R_{LIM} = 100 Ω

Figure 27. Voltage clamp during operation



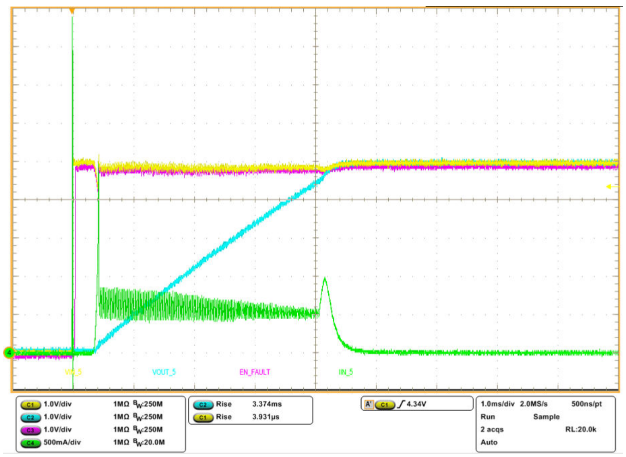
V_{IN} = from 5 V to 8 V, No load, $C_{dV/dt}$ = floating, C_{IN} = 2.2 µF, C_{OUT} = 10 µF, R_{LIM} = 100 Ω

Figure 28. Startup into output short-circuit



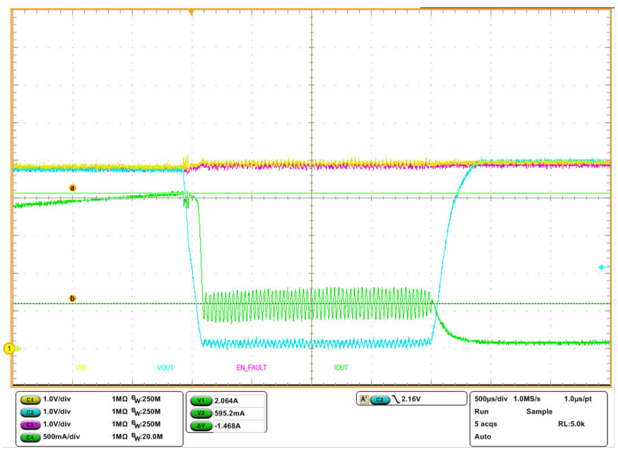
V_{IN} = 5 V, V_{OUT} shorted to GND, $C_{dV/dt}$ = floating, C_{IN} = 2.2 µF, C_{OUT} = 10 µF, R_{LIM} = 50 Ω

Figure 29. Hot-plug into overload



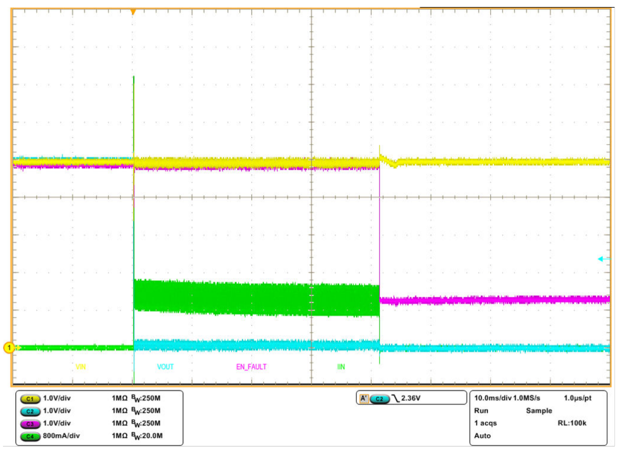
V_{IN} = 12 V, $C_{dV/dt}$ = floating, C_{IN} = 2.2 µF, C_{OUT} = 470 µF, R_{LIM} = 100 Ω

Figure 30. Overcurrent protection during operation



V_{IN} = 5 V, I_{OUT} = from 0 to current limit, $C_{dV/dt}$ = floating, C_{IN} = 2.2 µF, C_{OUT} = 10 µF, R_{LIM} = 100 Ω

Figure 31. Output short-circuit during operation



V_{IN} = 5 V, V_{OUT} = from 5 V to GND, $C_{dV/dt}$ = floating, C_{IN} = 2.2 µF, C_{OUT} = 10 µF, R_{LIM} = 50 Ω

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 TSOT23-8L package information

Figure 32. TSOT23-8L package outline

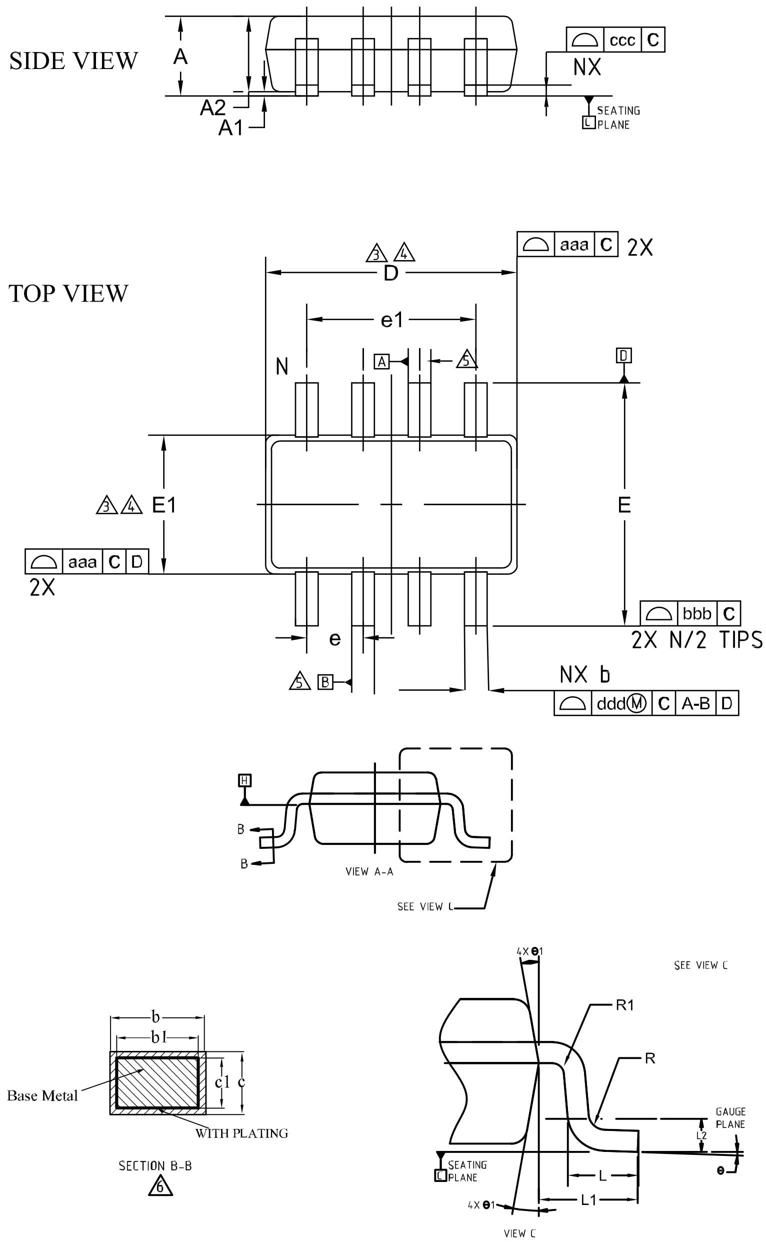
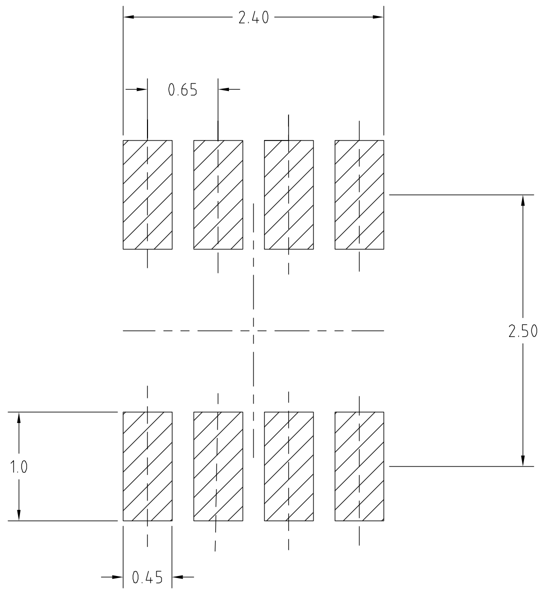


Table 8. **TSOT23-8L mechanical data**

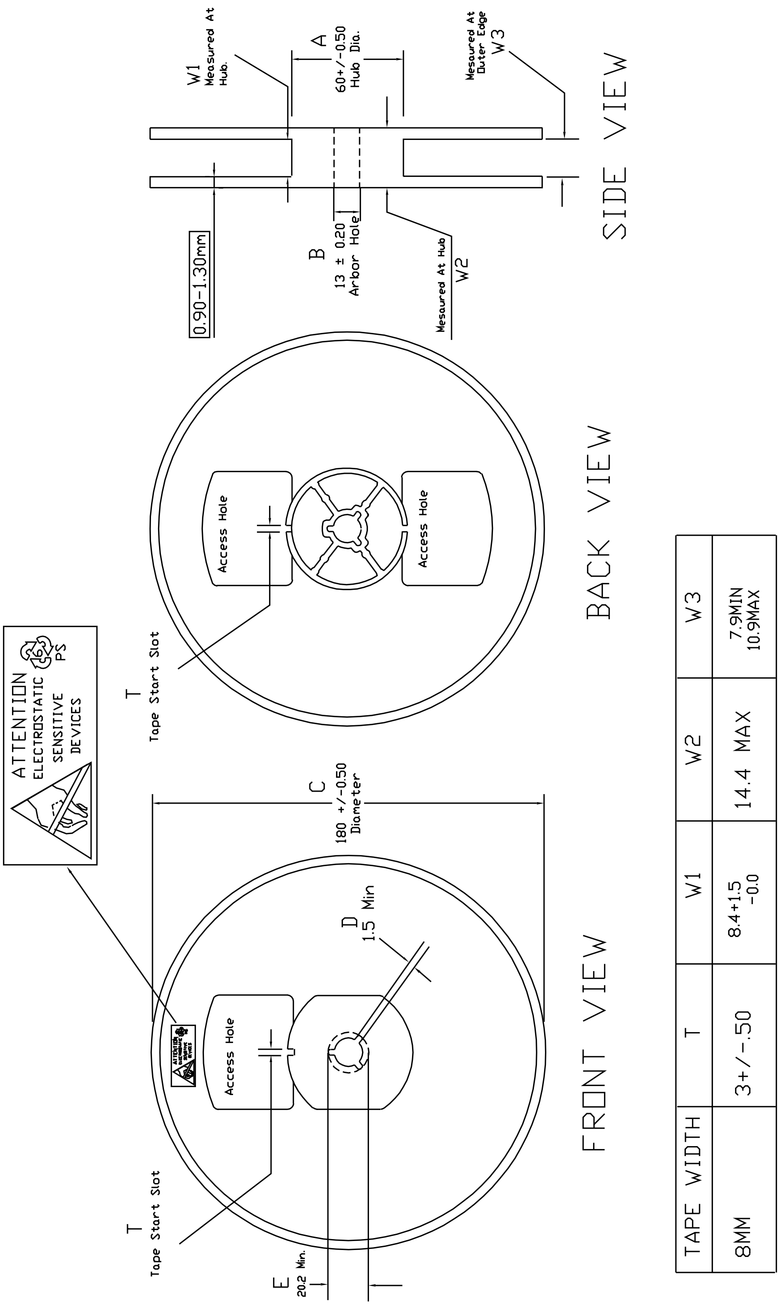
Dim.	mm		
	Min.	Typ.	Max.
A			1
A1	0.01	0.05	0.1
A2	0.84	0.87	0.9
b	0.22	-	0.36
b1	0.22	0.26	0.3
c	0.12	0.15	0.2
c1	0.08	0.13	0.16
D	-	2.90 BSC	-
E	-	2.80 BSC	-
E1	-	1.60 BSC	-
e	-	0.65 BSC	-
e1	-	1.95 BSC	-
L	0.3	0.4	0.5
L1	-	0.60 BSC	-
L2	-	0.25 BSC	-
R	0.1	-	-
R1	0.1	-	0.25
Θ	0	4°	8°
Θ1	4°	10°	12°
Tolerance of form and position			
aaa	0.15		
bbb	0.25		
ccc	0.1		
ddd	0.13		
N	8		
ND	4		

Figure 33. TSOT23-8L recommended footprint



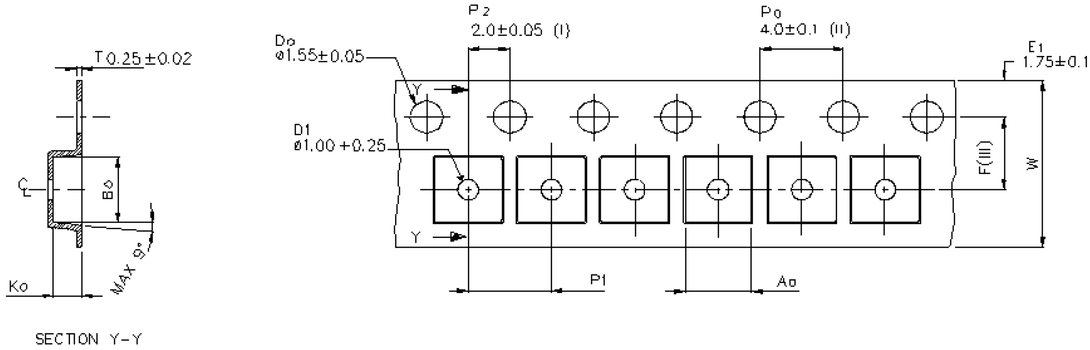
8.2 TSOT23-8L packing information

Figure 34. TSOT23-8L reel drawing outline



TAPE WIDTH	T	W1	W2	W3
8MM	3+/-.50	8.4+1.5 -0.0	14.4 MAX	7.9MIN 10.9MAX

Figure 35. **TSOT23-8L carrier tape**

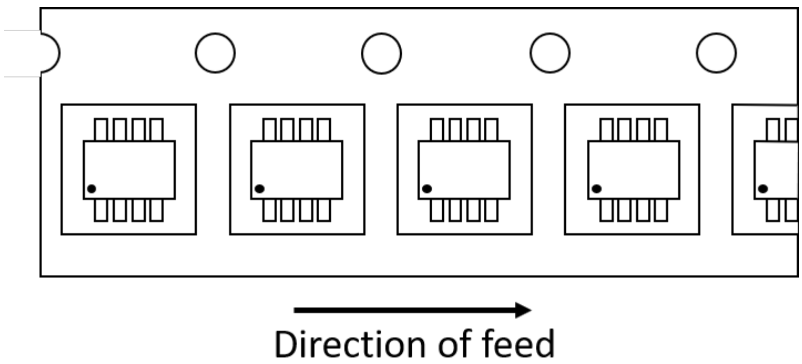


Ao	3.23 +/−0.10
Bo	3.17 +/−0.10
Ko	1.37 +/−0.10
F	3.50 +/−0.05
P1	4.00 +/−0.10
W	8.00 +0.3/−0.1

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape Max. 10^8 OHM/SR

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 36. **TSOT23-8L device orientation in tape**



9 Ordering information

Table 9. Order codes

Order code	Package	Packaging	Marking	Thermal protection
STEF05SGR	TSOT23-8	Tape and reel	05SL	Latch-off

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
27-Oct-2021	1	Initial release.
18-Dec-2023	2	Added footnote in Table 2, added Figure 7 and Figure 8.

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