

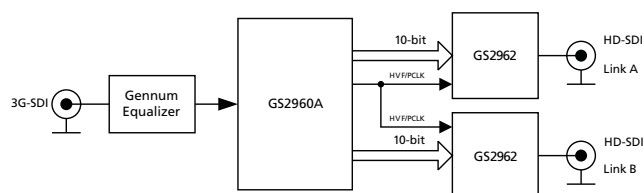
## 3Gb/s, HD, SD SDI Receiver Complete with SMPTE Video Processing

### Key Features

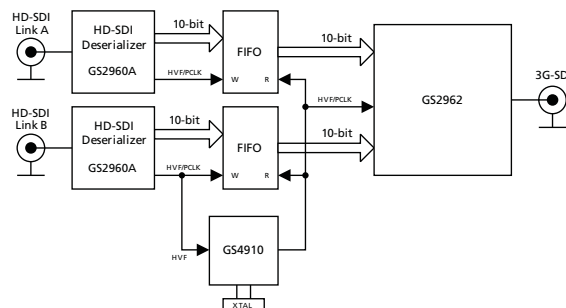
- Operation at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE 425M (Level A and Level B), SMPTE 424M, SMPTE 292, SMPTE 259M-C and DVB-ASI
- Integrated Reclocker
- Integrated low phase noise VCO
- Serial digital reclocked, or non-reclocked loop-through output
- Ancillary data extraction
- Optional conversion from SMPTE 425M Level B to Level A for 1080p 50/60 4:2:2 10-bit inputs
- Parallel data bus selectable as either 20-bit or 10-bit
- Comprehensive error detection and correction features
- Output H, V, F or CEA 861 Timing Signals
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- GSPI Host Interface
- Wide temperature range of -40°C to +85°C
- Low power operation (typically 350 mW)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and RoHS compliant

### Applications

Application: Single Link (3G-SDI) to Dual Link (HD-SDI) Converter



Application: Dual Link (HD-SDI) to Single Link (3G-SDI) Converter



### Description

The GS2960A is a multi-rate SDI Receiver which includes complete SMPTE processing, as per SMPTE 425M, 292 and SMPTE 259M-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The device features an integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The Serial Digital Output can be connected to an external Cable Driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode, the GS2960A performs SMPTE de-scrambling and NRZI to NRZ decoding and word alignment. Line-based CRC errors, line number errors, TRS errors and ancillary data check sum errors can all be detected. The GS2960A also provides ancillary data extraction. The entire ancillary data packet is extracted, and written to host-accessible registers. Other processing functions include H:V:F timing extraction, Luma and Chroma ancillary data indication, video standard detection, and SMPTE 352M packet detection and decoding. All of the processing features are optional and may be enabled or disabled via the Host Interface.

Parallel data outputs are provided in 20-bit or 10-bit multiplexed format for 3Gb/s, HD and SD video rates. For 1080p 50/60 4:2:2 10-bit, the parallel data is output on the

Note: for 3Gb/s 10-bit mode the device operates in Dual Data Rate (DDR) mode, where the data is sampled at both the rising and falling edges of the clock. This reduces the I/O speed requirements of the downstream devices.

# Contents

|                                                                             |    |
|-----------------------------------------------------------------------------|----|
| Key Features .....                                                          | 1  |
| Applications.....                                                           | 1  |
| Description.....                                                            | 1  |
| Functional Block Diagram .....                                              | 2  |
| 1. Pin Out.....                                                             | 7  |
| 1.1 Pin Assignment .....                                                    | 7  |
| 1.2 Pin Descriptions .....                                                  | 7  |
| 2. Electrical Characteristics .....                                         | 14 |
| 2.1 Absolute Maximum Ratings .....                                          | 14 |
| 2.2 Recommended Operating Conditions .....                                  | 14 |
| 2.3 DC Electrical Characteristics .....                                     | 15 |
| 2.4 AC Electrical Characteristics .....                                     | 17 |
| 3. Input/Output Circuits .....                                              | 22 |
| 4. Detailed Description.....                                                | 25 |
| 4.1 Functional Overview .....                                               | 25 |
| 4.2 SMPTE 425M Mapping - 3G Level A and Level B Formats .....               | 25 |
| 4.2.1 Level A Mapping .....                                                 | 25 |
| 4.2.2 Level B Mapping .....                                                 | 26 |
| 4.3 Serial Digital Input .....                                              | 26 |
| 4.4 Serial Digital Loop-Through Output .....                                | 26 |
| 4.5 Serial Digital Reclocker .....                                          | 27 |
| 4.5.1 PLL Loop Bandwidth .....                                              | 27 |
| 4.6 External Crystal/Reference Clock .....                                  | 28 |
| 4.7 Lock Detect .....                                                       | 29 |
| 4.7.1 Asynchronous Lock .....                                               | 30 |
| 4.7.2 Signal Interruption .....                                             | 31 |
| 4.8 SMPTE Functionality .....                                               | 31 |
| 4.8.1 Descrambling and Word Alignment .....                                 | 31 |
| 4.9 Parallel Data Outputs .....                                             | 32 |
| 4.9.1 Parallel Data Bus Buffers.....                                        | 32 |
| 4.9.2 Parallel Output in SMPTE Mode .....                                   | 35 |
| 4.9.3 Output Data Format in DVB-ASI Mode.....                               | 35 |
| 4.9.4 Parallel Output in Data-Through Mode .....                            | 36 |
| 4.9.5 Parallel Output Clock (PCLK).....                                     | 36 |
| 4.9.6 DDR Parallel Clock Timing .....                                       | 37 |
| 4.10 Timing Signal Generator .....                                          | 39 |
| 4.10.1 Manual Switch Line Lock Handling .....                               | 40 |
| 4.10.2 Automatic Switch Line Lock Handling .....                            | 41 |
| 4.10.3 Switch Line Lock Handling During Level B to Level A Conversion ..... | 41 |
| 4.11 Programmable Multi-function Outputs .....                              | 43 |
| 4.12 H:V:F Timing Signal Generation .....                                   | 44 |
| 4.12.1 CEA-861 Timing Generation .....                                      | 46 |
| 4.13 Automatic Video Standards Detection .....                              | 52 |
| 4.13.1 2K Support.....                                                      | 56 |

|                                                             |    |
|-------------------------------------------------------------|----|
| 4.14 Data Format Detection & Indication .....               | 56 |
| 4.15 EDH Detection .....                                    | 57 |
| 4.15.1 EDH Packet Detection .....                           | 57 |
| 4.15.2 EDH Flag Detection .....                             | 58 |
| 4.16 Video Signal Error Detection & Indication .....        | 58 |
| 4.16.1 TRS Error Detection .....                            | 60 |
| 4.16.2 Line Based CRC Error Detection .....                 | 60 |
| 4.16.3 EDH CRC Error Detection.....                         | 61 |
| 4.16.4 HD & 3G Line Number Error Detection .....            | 61 |
| 4.17 Ancillary Data Detection & Indication .....            | 61 |
| 4.17.1 Programmable Ancillary Data Detection.....           | 63 |
| 4.17.2 SMPTE 352M Payload Identifier .....                  | 64 |
| 4.17.3 Ancillary Data Checksum Error .....                  | 65 |
| 4.17.4 Video Standard Error .....                           | 66 |
| 4.18 Signal Processing .....                                | 66 |
| 4.18.1 TRS Correction & Insertion.....                      | 67 |
| 4.18.2 Line Based CRC Correction & Insertion .....          | 68 |
| 4.18.3 Line Number Error Correction & Insertion .....       | 68 |
| 4.18.4 ANC Data Checksum Error Correction & Insertion ..... | 68 |
| 4.18.5 EDH CRC Correction & Insertion .....                 | 68 |
| 4.18.6 Illegal Word Re-mapping .....                        | 69 |
| 4.18.7 TRS and Ancillary Data Preamble Remapping.....       | 69 |
| 4.18.8 Ancillary Data Extraction.....                       | 69 |
| 4.18.9 Level B to Level A Conversion .....                  | 73 |
| 4.19 GSPI - HOST Interface .....                            | 74 |
| 4.19.1 Command Word Description .....                       | 75 |
| 4.19.2 Data Read or Write Access.....                       | 75 |
| 4.19.3 GSPI Timing.....                                     | 76 |
| 4.20 Host Interface Register Maps .....                     | 78 |
| 4.21 JTAG Test Operation .....                              | 92 |
| 4.22 Device Power-up .....                                  | 93 |
| 4.23 Device Reset .....                                     | 93 |
| 4.24 Standby Mode .....                                     | 93 |
| 5. Application Reference Design .....                       | 94 |
| 5.1 Typical Application Circuit .....                       | 94 |
| 6. References & Relevant Standards .....                    | 95 |
| 7. Package & Ordering Information .....                     | 96 |
| 7.1 Package Dimensions .....                                | 96 |
| 7.2 Packaging Data .....                                    | 97 |
| 7.3 Marking Diagram .....                                   | 97 |
| 7.4 Solder Reflow Profiles .....                            | 98 |
| 7.5 Ordering Information .....                              | 98 |
| Revision History .....                                      | 98 |

## List of Figures

|                                                                                                                        |    |
|------------------------------------------------------------------------------------------------------------------------|----|
| Figure 3-1: Digital Input Pin with Schmitt Trigger .....                                                               | 22 |
| Figure 3-2: Bidirectional Digital Input/Output Pin.....                                                                | 22 |
| Figure 3-3: Bidirectional Digital Input/Output Pin with programmable drive strength.....                               | 23 |
| Figure 3-4: XTAL1/XTAL2/XTAL-OUT .....                                                                                 | 23 |
| Figure 3-5: VBG .....                                                                                                  | 23 |
| Figure 3-6: LB_CONT .....                                                                                              | 24 |
| Figure 3-7: Loop Filter .....                                                                                          | 24 |
| Figure 3-8: SDI/ $\overline{\text{SDI}}$ and TERM .....                                                                | 24 |
| Figure 3-9: SDO/ $\overline{\text{SDO}}$ .....                                                                         | 24 |
| Figure 4-1: Level A Mapping .....                                                                                      | 25 |
| Figure 4-2: Level B Mapping .....                                                                                      | 26 |
| Figure 4-3: 27MHz Clock Sources .....                                                                                  | 29 |
| Figure 4-4: PCLK to Data and Control Signal Output Timing - SDR Mode 1 .....                                           | 32 |
| Figure 4-5: PCLK to Data and Control Signal Output Timing - SDR Mode 2 .....                                           | 33 |
| Figure 4-6: PCLK to Data and Control Signal Output Timing - DDR Mode .....                                             | 34 |
| Figure 4-7: DDR Video Interface - 3G Level A .....                                                                     | 37 |
| Figure 4-8: DDR Video Interface - 3G Level B .....                                                                     | 38 |
| Figure 4-9: Delay Adjustment Ranges .....                                                                              | 39 |
| Figure 4-10: Switch Line Locking on a Non-Standard Switch Line .....                                                   | 40 |
| Figure 4-11: H:V:F Output Timing - 3G Level A and HDTV 20-bit Mode .....                                               | 44 |
| Figure 4-12: H:V:F Output Timing - 3G Level A and HDTV 10-bit Mode<br>3G Level B 20-bit Mode, each 10-bit stream ..... | 44 |
| Figure 4-13: H:V:F Output Timing - 3G Level B 10-bit Mode .....                                                        | 45 |
| Figure 4-14: H:V:F Output Timing - HD 20-bit Output Mode .....                                                         | 45 |
| Figure 4-15: H:V:F Output Timing - HD 10-bit Output Mode .....                                                         | 45 |
| Figure 4-16: H:V:F Output Timing - SD 20-bit Output Mode .....                                                         | 45 |
| Figure 4-17: H:V:F Output Timing - SD 10-bit Output Mode .....                                                         | 45 |
| Figure 4-18: H:V:DE Output Timing 1280 x 720p @ 59.94/60 (Format 4) .....                                              | 47 |
| Figure 4-19: H:V:DE Output Timing 1920 x 1080i @ 59.94/60 (Format 5) .....                                             | 47 |
| Figure 4-20: H:V:DE Output Timing 720 (1440) x 480i @ 59.94/60 (Format 6&7) .....                                      | 48 |
| Figure 4-21: H:V:DE Output Timing 1280 x 720p @ 50 (Format 19) .....                                                   | 48 |
| Figure 4-22: H:V:DE Output Timing 1920 x 1080i @ 50 (Format 20) .....                                                  | 49 |
| Figure 4-23: H:V:DE Output Timing 720 (1440) x 576 @ 50 (Format 21 & 22) .....                                         | 50 |
| Figure 4-24: H:V:DE Output Timing 1920 x 1080p @ 59.94/60 (Format 16) .....                                            | 50 |
| Figure 4-25: H:V:DE Output Timing 1920 x 1080p @ 50 (Format 31) .....                                                  | 51 |
| Figure 4-26: H:V:DE Output Timing 1920 x 1080p @ 23.94/24 (Format 32) .....                                            | 51 |
| Figure 4-27: H:V:DE Output Timing 1920 x 1080p @ 25 (Format 33) .....                                                  | 52 |
| Figure 4-28: H:V:DE Output Timing 1920 x 1080p @ 29.97/30 (Format 34) .....                                            | 52 |
| Figure 4-29: 2K Feature Enhancement .....                                                                              | 56 |
| Figure 4-30: Y/1ANC and C/2ANC Signal Timing .....                                                                     | 63 |
| Figure 4-31: Ancillary Data Extraction - Step A .....                                                                  | 70 |
| Figure 4-32: Ancillary Data Extraction - Step B .....                                                                  | 71 |
| Figure 4-33: Ancillary Data Extraction - Step C .....                                                                  | 71 |
| Figure 4-34: Ancillary Data Extraction - Step D .....                                                                  | 72 |
| Figure 4-35: GSPI Application Interface Connection .....                                                               | 74 |
| Figure 4-36: Command Word Format .....                                                                                 | 75 |
| Figure 4-37: Data Word Format .....                                                                                    | 76 |
| Figure 4-38: Write Mode .....                                                                                          | 76 |
| Figure 4-39: Read Mode .....                                                                                           | 76 |
| Figure 4-40: GSPI Time Delay .....                                                                                     | 76 |
| Figure 4-41: In-Circuit JTAG .....                                                                                     | 92 |
| Figure 4-42: System JTAG .....                                                                                         | 92 |
| Figure 4-43: Reset Pulse .....                                                                                         | 93 |
| Figure 7-1: Pb-free Solder Reflow Profile .....                                                                        | 98 |

# List of Tables

|                                                                               |    |
|-------------------------------------------------------------------------------|----|
| Table 1-1: Pin Descriptions .....                                             | 7  |
| Table 2-1: Absolute Maximum Ratings.....                                      | 14 |
| Table 2-2: Recommended Operating Conditions.....                              | 14 |
| Table 2-3: DC Electrical Characteristics .....                                | 15 |
| Table 2-4: AC Electrical Characteristics .....                                | 17 |
| Table 4-1: Serial Digital Output.....                                         | 27 |
| Table 4-2: PLL Loop Bandwidth .....                                           | 27 |
| Table 4-3: Input Clock Requirements.....                                      | 29 |
| Table 4-4: Lock Detect Conditions.....                                        | 30 |
| Table 4-5: GS2960A Output Video Data Format Selections .....                  | 34 |
| Table 4-6: GS2960A PCLK Output Rates .....                                    | 36 |
| Table 4-7: Switch Line Position for Digital Systems .....                     | 42 |
| Table 4-8: Output Signals Available on Programmable Multi-Function Pins ..... | 43 |
| Table 4-9: Supported CEA-861 Formats.....                                     | 46 |
| Table 4-10: Supported Video Standard Codes .....                              | 53 |
| Table 4-11: Data Format Register Codes .....                                  | 57 |
| Table 4-12: Error Status Register and Error Mask Register .....               | 59 |
| Table 4-13: SMPTE 352M Packet Data .....                                      | 65 |
| Table 4-14: IOPROC_DISABLE Register Bits .....                                | 67 |
| Table 4-15: GSPI Time Delay.....                                              | 76 |
| Table 4-16: GSPI Timing Parameters (50% levels; 3.3V or 1.8V operation) ..... | 77 |
| Table 4-17: Configuration and Status Registers.....                           | 78 |
| Table 4-18: ANC Extraction FIFO Access Registers.....                         | 91 |
| Table 7-1: Packaging Data.....                                                | 97 |

# 1. Pin Out

## 1.1 Pin Assignment

|   | 1                       | 2          | 3                           | 4        | 5        | 6        | 7                                 | 8             | 9      | 10     |
|---|-------------------------|------------|-----------------------------|----------|----------|----------|-----------------------------------|---------------|--------|--------|
| A | VBG                     | LF         | LB_CONT                     | VCO_VDD  | STAT0    | STAT1    | IO_VDD                            | PCLK          | DOUT18 | DOUT17 |
| B | A_VDD                   | PLL_VDD    | RSV                         | VCO_GND  | STAT2    | STAT3    | IO_GND                            | DOUT19        | DOUT16 | DOUT15 |
| C | SDI                     | A_GND      | PLL_VDD                     | PLL_VDD  | STAT4    | STAT5    | $\overline{\text{RESET\_TRST}}$   | DOUT12        | DOUT14 | DOUT13 |
| D | $\overline{\text{SDI}}$ | A_GND      | A_GND                       | PLL_GND  | CORE_GND | CORE_VDD | SW_EN                             | JTAG/HOST     | IO_GND | IO_VDD |
| E | SDI_VDD                 | SDI_GND    | A_GND                       | PLL_GND  | CORE_GND | CORE_VDD | SDOUT_TDO                         | SDIN_TDI      | DOUT10 | DOUT11 |
| F | TERM                    | RSV        | A_GND                       | PLL_GND  | CORE_GND | CORE_VDD | $\overline{\text{CS\_TMS}}$       | SCLK_TCK      | DOUT8  | DOUT9  |
| G | RSV                     | RSV        | $\overline{\text{RC\_BYP}}$ | CORE_GND | CORE_GND | CORE_VDD | $\overline{\text{SMPTE\_BYPASS}}$ | DVB_ASI       | IO_GND | IO_VDD |
| H | BUFF_VDD                | BUFF_GND   | RSV                         | RSV      | TIM_861  | XTAL_OUT | 20bit/10bit                       | IOPROC_EN/DIS | DOUT6  | DOUT7  |
| J | SDO                     | SDO_EN/DIS | RSV                         | RSV      | RSV      | XTAL2    | IO_GND                            | DOUT1         | DOUT4  | DOUT5  |
| K | $\overline{\text{SDO}}$ | STANDBY    | RSV                         | RSV      | RSV      | XTAL1    | IO_VDD                            | DOUT0         | DOUT2  | DOUT3  |

## 1.2 Pin Descriptions

Table 1-1: Pin Descriptions

| Pin Number | Name    | Timing | Type         | Description                                                                                                                                                                                                                    |
|------------|---------|--------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A1         | VBG     |        | Analog Input | Band Gap voltage filter connection.                                                                                                                                                                                            |
| A2         | LF      |        | Analog Input | Loop Filter component connection.                                                                                                                                                                                              |
| A3         | LB_CONT |        | Analog Input | Connection for loop bandwidth control resistor.                                                                                                                                                                                |
| A4         | VCO_VDD |        | Input Power  | POWER pin for the VCO. Connect to a 1.2V±5% analog supply followed by a RC filter (see <a href="#">5.1 Typical Application Circuit</a> ). A 105Ω 1% resistor must be used in the RC filter circuit. VCO_VDD is nominally 0.7V. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number               | Name                           | Timing | Type        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
|--------------------------|--------------------------------|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|--------------------------------|----------------|--------------------------------|----------------|--------------------------------|----------------|--------------|----------------|----------------|--------|-------|--------|---|------------|-------|-------------|---|--------------|---|----------------|---|-----------|---|-----------|---|
| A5, A6, B5, B6, C5, C6   | STAT[0:5]                      |        | Output      | <p>MULTI-FUNCTIONAL OUTPUT PORT.</p> <p>Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Each of the STAT [0:5] pins can be configured individually to output one of the following signals:</p> <table><tr><th>Signal</th><th>Default</th></tr><tr><td>H/HSYNC</td><td>STAT0</td></tr><tr><td>V/VSYNC</td><td>STAT1</td></tr><tr><td>F/DE</td><td>STAT2</td></tr><tr><td>LOCKED</td><td>STAT3</td></tr><tr><td>Y/1ANC</td><td>STAT4</td></tr><tr><td>C/2ANC</td><td>—</td></tr><tr><td>DATA ERROR</td><td>STAT5</td></tr><tr><td>VIDEO ERROR</td><td>—</td></tr><tr><td>EDH DETECTED</td><td>—</td></tr><tr><td>CARRIER DETECT</td><td>—</td></tr><tr><td>RATE_DET0</td><td>—</td></tr><tr><td>RATE_DET1</td><td>—</td></tr></table> | Signal                   | Default                        | H/HSYNC        | STAT0                          | V/VSYNC        | STAT1                          | F/DE           | STAT2        | LOCKED         | STAT3          | Y/1ANC | STAT4 | C/2ANC | — | DATA ERROR | STAT5 | VIDEO ERROR | — | EDH DETECTED | — | CARRIER DETECT | — | RATE_DET0 | — | RATE_DET1 | — |
| Signal                   | Default                        |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| H/HSYNC                  | STAT0                          |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| V/VSYNC                  | STAT1                          |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| F/DE                     | STAT2                          |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| LOCKED                   | STAT3                          |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| Y/1ANC                   | STAT4                          |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| C/2ANC                   | —                              |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| DATA ERROR               | STAT5                          |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| VIDEO ERROR              | —                              |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| EDH DETECTED             | —                              |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| CARRIER DETECT           | —                              |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| RATE_DET0                | —                              |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| RATE_DET1                | —                              |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| A7, D10, G10, K7         | IO_VDD                         |        | Input Power | POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| A8                       | PCLK                           |        | Output      | <p>PARALLEL DATA BUS CLOCK</p> <p>Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <table><tr><td>3G 10-bit or 20-bit mode</td><td>PCLK @ 148.5 or 148.5/1.001MHz</td></tr><tr><td>HD 10-bit mode</td><td>PCLK @ 148.5 or 148.5/1.001MHz</td></tr><tr><td>HD 20-bit mode</td><td>PCLK @ 74.25 or 74.25/1.001MHz</td></tr><tr><td>SD 10-bit mode</td><td>PCLK @ 27MHz</td></tr><tr><td>SD 20-bit mode</td><td>PCLK @ 13.5MHz</td></tr></table>                                                                                                                                                                                                                                                                                           | 3G 10-bit or 20-bit mode | PCLK @ 148.5 or 148.5/1.001MHz | HD 10-bit mode | PCLK @ 148.5 or 148.5/1.001MHz | HD 20-bit mode | PCLK @ 74.25 or 74.25/1.001MHz | SD 10-bit mode | PCLK @ 27MHz | SD 20-bit mode | PCLK @ 13.5MHz |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| 3G 10-bit or 20-bit mode | PCLK @ 148.5 or 148.5/1.001MHz |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| HD 10-bit mode           | PCLK @ 148.5 or 148.5/1.001MHz |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| HD 20-bit mode           | PCLK @ 74.25 or 74.25/1.001MHz |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| SD 10-bit mode           | PCLK @ 27MHz                   |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |
| SD 20-bit mode           | PCLK @ 13.5MHz                 |        |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                          |                                |                |                                |                |                                |                |              |                |                |        |       |        |   |            |       |             |   |              |   |                |   |           |   |           |   |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number                                 | Name                                       | Timing | Type         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------------------------------------------|--------------------------------------------|--------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A9, A10, B8, B9, B10, C8, C9, C10, E9, E10 | DOUT18, 17, 19, 16, 15, 12, 14, 13, 10, 11 |        | Output       | <p>PARALLEL DATA BUS</p> <p>Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <hr/> <p>20-bit mode<br/>20bit/10b<math>\overline{\text{it}}</math> = HIGH</p> <p>SMPTE mode (<math>\overline{\text{SMPTE\_BYPASS}}</math> = HIGH and DVB_ASI = LOW):<br/>Luma data output for SD and HD data rates; Data Stream 1 for 3G data rate<br/>DVB-ASI mode (<math>\overline{\text{SMPTE\_BYPASS}}</math> = LOW and DVB_ASI = HIGH):<br/>Not defined<br/>Data-Through mode (<math>\overline{\text{SMPTE\_BYPASS}}</math> = LOW and DVB_ASI = LOW):<br/>Data output</p> <hr/> <p>10-bit mode<br/>20bit/10b<math>\overline{\text{it}}</math> = LOW</p> <p>SMPTE mode (<math>\overline{\text{SMPTE\_BYPASS}}</math> = HIGH and DVB_ASI = LOW):<br/>Multiplexed Luma/Chroma data output for SD and HD data rates; Multiplexed Data Stream 1&amp;2 for 3G data rate<br/>DVB-ASI mode (<math>\overline{\text{SMPTE\_BYPASS}}</math> = LOW and DVB_ASI = HIGH):<br/>8b/10b decoded DVB-ASI data<br/>Data-Through mode (<math>\overline{\text{SMPTE\_BYPASS}}</math> = LOW and DVB_ASI = LOW):<br/>Data output</p> |
| B1                                         | A_VDD                                      |        | Input Power  | POWER pin for analog circuitry. Connect to 3.3V DC analog.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| B2, C3, C4                                 | PLL_VDD                                    |        | Input Power  | POWER pins for the Reclocker PLL. Connect to 1.2V DC analog.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| B3, F2, G1, G2                             | RSV                                        |        |              | These pins must be left unconnected.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| B4                                         | VCO_GND                                    |        | Input Power  | GND pin for the VCO. Connect to analog GND.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| B7, D9, G9, J7                             | IO_GND                                     |        | Input Power  | GND connection for digital I/O. Connect to digital GND.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| C1, D1                                     | SDI, $\overline{\text{SDI}}$               |        | Analog Input | Serial Digital Differential Input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| C2, D2, D3, E3, F3                         | A_GND                                      |        | Input Power  | GND pins for sensitive analog circuitry. Connect to analog GND.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number         | Name                                 | Timing | Type        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------|--------------------------------------|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C7                 | $\overline{\text{RESET\_TRST}}$      |        | Input       | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Used to reset the internal operating conditions to default settings and to reset the JTAG sequence.</p> <p>Normal mode (<math>\text{JTAG}/\overline{\text{HOST}} = \text{LOW}</math>):</p> <p>When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance.</p> <p>When HIGH, normal operation of the device resumes.</p> <p>JTAG test mode (<math>\text{JTAG}/\overline{\text{HOST}} = \text{HIGH}</math>):</p> <p>When LOW, all functional blocks are set to default and the JTAG test sequence is reset.</p> <p>When HIGH, normal operation of the JTAG test sequence resumes after <math>\overline{\text{RESET\_TRST}}</math> is de-asserted.</p> |
| D4, E4, F4         | PLL_GND                              |        | Input Power | GND pins for the Reclocker PLL. Connect to analog GND.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| D5, E5, F5, G4, G5 | CORE_GND                             |        | Input Power | GND connection for device core. Connect to digital GND.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| D6, E6, F6, G6     | CORE_VDD                             |        | Input Power | POWER connection for device core. Connect to 1.2V DC digital.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| D7                 | SW_EN                                |        | Input       | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Used to enable switch-line locking, as described in <a href="#">Section 4.10.1</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| D8                 | $\text{JTAG}/\overline{\text{HOST}}$ |        | Input       | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Used to select JTAG test mode or host interface mode.</p> <p>When <math>\text{JTAG}/\overline{\text{HOST}}</math> is HIGH, the host interface port is configured for JTAG test.</p> <p>When <math>\text{JTAG}/\overline{\text{HOST}}</math> is LOW, normal operation of the host interface port resumes.</p>                                                                                                                                                                                                                                                                                                                                                                                                |
| E1                 | SDI_VDD                              |        | Input Power | POWER pin for SDI buffer. Connect to 3.3V DC analog.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| E2                 | SDI_GND                              |        | Input Power | GND pin for SDI buffer. Connect to analog GND.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| E7                 | SDOUT_TDO                            |        | Output      | <p>COMMUNICATION SIGNAL OUTPUT</p> <p>Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>GSPI serial data output/test data out.</p> <p>In JTAG mode (<math>\text{JTAG}/\overline{\text{HOST}} = \text{HIGH}</math>), this pin is used to shift test results from the device.</p> <p>In host interface mode, this pin is used to read status and configuration data from the device.</p> <p><b>Note:</b> GSPI is slightly different than the SPI. For more details on GSPI, please refer to <a href="#">4.19 GSPI - HOST Interface</a>.</p>                                                                                                                                                                                                                                                   |

Table 1-1: Pin Descriptions (Continued)

| Pin Number                                 | Name                             | Timing | Type         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------------------------------------------|----------------------------------|--------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E8                                         | SDIN_TDI                         |        | Input        | COMMUNICATION SIGNAL INPUT<br>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.<br>GSPI serial data in/test data in.<br>In JTAG mode ( $JTAG/\overline{HOST}$ = HIGH), this pin is used to shift test data into the device.<br>In host interface mode, this pin is used to write address and configuration data words into the device.                                                                                 |
| F1                                         | TERM                             |        | Analog Input | Decoupling for internal SDI termination resistors.                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| F7                                         | $\overline{CS\_TMS}$             |        | Input        | COMMUNICATION SIGNAL INPUT<br>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.<br>Chip select / test mode start.<br>In JTAG mode ( $JTAG/\overline{HOST}$ = HIGH), this pin is Test Mode Start, used to control the operation of the JTAG test.<br>In host interface mode ( $JTAG/\overline{HOST}$ = LOW), this pin operates as the host interface chip select and is active LOW.                                     |
| F8                                         | SCLK_TCK                         |        | Input        | COMMUNICATION SIGNAL INPUT<br>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.<br>Serial data clock signal.<br>In JTAG mode ( $JTAG/\overline{HOST}$ = HIGH), this pin is the JTAG clock.<br>In host interface mode ( $JTAG/\overline{HOST}$ = LOW), this pin is the host interface serial bit clock.<br>All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock. |
| F9, F10, H9, H10, J8, J9, J10, K8, K9, K10 | DOUT8, 9, 6, 7, 1, 4, 5, 0, 2, 3 |        | Output       | PARALLEL DATA BUS<br>Please refer to the Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.                                                                                                                                                                                                                                                                                                                                                |
|                                            |                                  |        |              | 20-bit mode<br>20bit/ $\overline{10bit}$ = HIGH                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                                            |                                  |        |              | SMPTE mode ( $\overline{SMPTE\_BYPASS}$ = HIGH and DVB_ASI = LOW):<br>Chroma data output for SD and HD data rates; Data Stream 2 for 3G data rate<br>DVB-ASI mode ( $\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = HIGH):<br>Not defined<br>Data-Through mode ( $\overline{SMPTE\_BYPASS}$ = LOW and DVB_ASI = LOW):<br>Data output                                                                                                                                                                                     |
|                                            |                                  |        |              | 10-bit mode<br>20bit/ $\overline{10bit}$ = LOW                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|                                            |                                  |        |              | Forced LOW                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| G3                                         | $\overline{RC\_BYP}$             |        | Input        | CONTROL SIGNAL INPUT<br>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.<br>When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.                                                                                                                                     |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number                       | Name                              | Timing | Type           | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------------------------------|-----------------------------------|--------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| G7                               | $\overline{\text{SMPTE\_BYPASS}}$ |        | Input/Output   | <p>CONTROL SIGNAL INPUT/OUTPUT</p> <p>Please refer to the Input/Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Indicates the presence of valid SMPTE data.</p> <p>When the <math>\text{AUTO}/\overline{\text{MAN}}</math> bit in the host interface register is HIGH (Default), this pin is an OUTPUT. <math>\overline{\text{SMPTE\_BYPASS}}</math> is HIGH when the device locks to a SMPTE compliant input. <math>\overline{\text{SMPTE\_BYPASS}}</math> is LOW under all other conditions.</p> <p>When the <math>\text{AUTO}/\overline{\text{MAN}}</math> bit in the host interface register is LOW, this pin is an INPUT:</p> <p>No SMPTE scrambling takes place, and none of the I/O processing features of the device are available when <math>\overline{\text{SMPTE\_BYPASS}}</math> is set LOW.</p> <p>When <math>\overline{\text{SMPTE\_BYPASS}}</math> is set HIGH, the device carries out SMPTE scrambling and I/O processing.</p> <p>When <math>\overline{\text{SMPTE\_BYPASS}}</math> and <math>\text{DVB\_ASI}</math> are both set LOW, the device operates in Data-Through mode.</p> |
| G8                               | $\text{DVB\_ASI}$                 |        | Input/Output   | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input/Output Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Used to enable/disable DVB-ASI data extraction in manual mode.</p> <p>When the <math>\text{AUTO}/\overline{\text{MAN}}</math> bit in the host interface is LOW, this pin is an input and when the <math>\text{DVB\_ASI}</math> pin is set HIGH the device carries out <math>\text{DVB\_ASI}</math> data extraction and processing. The <math>\overline{\text{SMPTE\_BYPASS}}</math> pin must be set LOW. When <math>\overline{\text{SMPTE\_BYPASS}}</math> and <math>\text{DVB\_ASI}</math> are both set LOW, the device operates in Data-Through mode.</p> <p>When the <math>\text{AUTO}/\overline{\text{MAN}}</math> bit in the host interface is HIGH (Default), <math>\text{DVB\_ASI}</math> is configured as a status output (set LOW), and <math>\text{DVB\_ASI}</math> input streams are not supported or recognized.</p>                                                                                                                                                            |
| H1                               | $\text{BUFF\_VDD}$                |        | Input Power    | POWER pin for the serial digital output 50 $\Omega$ buffer. Connect to 3.3V DC analog.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| H2                               | $\text{BUFF\_GND}$                |        | Input Power    | GND pin for the cable driver buffer. Connect to analog GND.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| H3, H4, J3,<br>J4, J5, K3,<br>K5 | RSV                               |        |                | These pins must be connected to $\text{CORE\_GND}$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| H5                               | $\text{TIM\_861}$                 |        | Input          | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Used to select CEA-861 timing mode.</p> <p>When <math>\text{TIM\_861}</math> is HIGH, the device outputs CEA 861 timing signals (HSYNC/VSYNC/DE) instead of H:V:F digital timing signals.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| H6                               | $\text{XTAL\_OUT}$                |        | Digital Output | Buffered 27MHz crystal output. Can be used to cascade the crystal signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name                               | Timing | Type         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------------|------------------------------------|--------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| H7         | 20bit/ $\overline{10\text{bit}}$   |        | Input        | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Used to select the output bus width.</p> <p>HIGH = 20-bit, LOW = 10-bit.</p>                                                                                                                                                                                                                                                                                                              |
| H8         | IOPROC_EN/ $\overline{\text{DIS}}$ |        | Input        | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Used to enable or disable video processing features. When IOPROC_EN is HIGH, the video processing features of the device are enabled. When IOPROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode.</p>                                                                                                                   |
| J1, K1     | SDO, $\overline{\text{SDO}}$       |        | Output       | <p>Serial Data Output Signal.</p> <p>50Ω CML buffer for interfacing to an external cable driver.</p> <p>Serial digital output signal operating at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s.</p>                                                                                                                                                                                                                                                                                                                                                            |
| J2         | SDO_EN/ $\overline{\text{DIS}}$    |        | Input        | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>Used to enable/disable the serial digital output stage.</p> <p>When SDO_EN/<math>\overline{\text{DIS}}</math> is LOW, the serial digital output signals, SDO and <math>\overline{\text{SDO}}</math>, are both pulled HIGH.</p> <p>When SDO_EN/<math>\overline{\text{DIS}}</math> is HIGH, the serial digital output signals, SDO and <math>\overline{\text{SDO}}</math>, are enabled.</p> |
| J6, K6     | XTAL2, XTAL1                       |        | Analog Input | Input connection for 27MHz crystal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| K2         | STANDBY                            |        | Input        | <p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the <a href="#">DC Electrical Characteristics</a> table for logic level threshold and compatibility.</p> <p>When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down.</p> <p>In this mode, the serial digital output signals, SDO and <math>\overline{\text{SDO}}</math>, are both pulled HIGH.</p>                                                                                                                   |
| K4         | RSV                                |        |              | This pin must be left unconnected.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

## 2. Electrical Characteristics

### 2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

| Parameter                                              | Value/Units     |
|--------------------------------------------------------|-----------------|
| Supply Voltage, Digital Core (CORE_VDD)                | -0.3V to +1.5V  |
| Supply Voltage, Digital I/O (IO_VDD)                   | -0.3V to +4.0V  |
| Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD)          | -0.3V to +1.5V  |
| Supply Voltage, Analog 3.3V (SDI_VDD, BUFF_VDD, A_VDD) | -0.3V to +4.0V  |
| Input Voltage Range (digital inputs)                   | -2.0V to +5.25V |
| Operating Temperature Range                            | -20°C to +85°C  |
| Functional Temperature Range                           | -40°C to +85°C  |
| Storage Temperature Range                              | -50°C to +125°C |
| Peak Reflow Temperature (JEDEC J-STD-020C)             | 260°C           |
| ESD Sensitivity, HBM (JESD22-A114)                     | 2kV             |

**NOTES:**

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

### 2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

T<sub>A</sub> = -20°C to + 85°C, unless otherwise shown.

| Parameter                            | Symbol   | Conditions | Min  | Typ | Max  | Units | Notes |
|--------------------------------------|----------|------------|------|-----|------|-------|-------|
| Supply Voltage, Digital Core         | CORE_VDD | –          | 1.14 | 1.2 | 1.26 | V     | –     |
| Supply Voltage, Digital I/O          | IO_VDD   | 1.8V mode  | 1.71 | 1.8 | 1.89 | V     | –     |
|                                      |          | 3.3V mode  | 3.13 | 3.3 | 3.47 | V     | –     |
| Supply Voltage, PLL                  | PLL_VDD  | –          | 1.14 | 1.2 | 1.26 | V     | –     |
| Supply Voltage, Analog               | A_VDD    | –          | 3.13 | 3.3 | 3.47 | V     | 1     |
| Supply Voltage, Serial Digital Input | SDI_VDD  | –          | 3.13 | 3.3 | 3.47 | V     | 1     |
| Supply Voltage, CD Buffer            | BUFF_VDD | –          | 3.13 | 3.3 | 3.47 | V     | 1     |

**NOTES:**

1. The 3.3V supplies must track the 3.3V supply of an external EQ and external CD.

## 2.3 DC Electrical Characteristics

**Table 2-3: DC Electrical Characteristics**

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                             | Symbol           | Conditions             | Min             | Typ | Max             | Units | Notes |
|---------------------------------------|------------------|------------------------|-----------------|-----|-----------------|-------|-------|
| System                                |                  |                        |                 |     |                 |       |       |
| +1.2V Supply Current                  | I <sub>1V2</sub> | 10bit 3G               | –               | 200 | 235             | mA    | –     |
|                                       |                  | 20bit 3G               | –               | 195 | 235             | mA    | –     |
|                                       |                  | 10/20bit HD            | –               | 160 | 210             | mA    | –     |
|                                       |                  | 10/20bit SD            | –               | 135 | 165             | mA    | –     |
|                                       |                  | DVB_ASI                | –               | 135 | 165             | mA    | –     |
| +1.8V Supply Current                  | I <sub>1V8</sub> | 10bit 3G               | –               | 32  | 34              | mA    | –     |
|                                       |                  | 20bit 3G               | –               | 31  | 34              | mA    | –     |
|                                       |                  | 10/20bit HD            | –               | 20  | 21              | mA    | –     |
|                                       |                  | 10/20bit SD            | –               | 6   | 7               | mA    | –     |
|                                       |                  | DVB_ASI                | –               | 6   | 7               | mA    | –     |
| +3.3V Supply Current                  | I <sub>3V3</sub> | 10bit 3G               | –               | 95  | 105             | mA    | –     |
|                                       |                  | 20bit 3G               | –               | 95  | 105             | mA    | –     |
|                                       |                  | 10/20bit HD            | –               | 65  | 75              | mA    | –     |
|                                       |                  | 10/20bit SD            | –               | 35  | 45              | mA    | –     |
|                                       |                  | DVB_ASI                | –               | 35  | 45              | mA    | –     |
| Total Device Power<br>(IO_VDD = 1.8V) | P <sub>1D8</sub> | 10bit 3G               | –               | 350 | 430             | mW    | –     |
|                                       |                  | 20bit 3G               | –               | 320 | 400             | mW    | –     |
|                                       |                  | 10/20bit HD            | –               | 280 | 335             | mW    | –     |
|                                       |                  | 10/20bit SD            | –               | 240 | 305             | mW    | –     |
|                                       |                  | DVB_ASI                | –               | 240 | 305             | mW    | –     |
|                                       |                  | Reset                  | –               | 200 | –               | mW    | –     |
|                                       |                  | Standby                | –               | 16  | 44              | mW    | –     |
| Total Device Power<br>(IO_VDD = 3.3V) | P <sub>3D3</sub> | 10bit 3G               | –               | 550 | 665             | mW    | –     |
|                                       |                  | 20bit 3G               | –               | 520 | 665             | mW    | –     |
|                                       |                  | 10/20bit HD            | –               | 400 | 505             | mW    | –     |
|                                       |                  | 10/20bit SD            | –               | 280 | 370             | mW    | –     |
|                                       |                  | DVB_ASI                | –               | 280 | 370             | mW    | –     |
|                                       |                  | Reset                  | –               | 220 | –               | mW    | –     |
|                                       |                  | Standby                | –               | 16  | 44              | mW    | –     |
| Digital I/O                           |                  |                        |                 |     |                 |       |       |
| Input Logic LOW                       | V <sub>IL</sub>  | 3.3V or 1.8V operation | IO_VSS<br>-0.3  | –   | 0.3 x<br>IO_VDD | V     | –     |
| Input Logic HIGH                      | V <sub>IH</sub>  | 3.3V or 1.8V operation | 0.7 x<br>IO_VDD | –   | IO_VDD<br>+0.3  | V     | –     |

**Table 2-3: DC Electrical Characteristics (Continued)**

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                         | Symbol          | Conditions                | Min                  | Typ                   | Max                   | Units | Notes |
|-----------------------------------|-----------------|---------------------------|----------------------|-----------------------|-----------------------|-------|-------|
| Output Logic LOW                  | V <sub>OL</sub> | IOL = 5mA, 1.8V operation | –                    | –                     | 0.2                   | V     | –     |
|                                   |                 | IOL = 8mA, 3.3V operation | –                    | –                     | 0.4                   | V     | –     |
| Output Logic HIGH                 | V <sub>OH</sub> | IOH = 5mA, 1.8V operation | 1.4                  | –                     | –                     | V     | –     |
|                                   |                 | IOH = 8mA, 3.3V operation | 2.4                  | –                     | –                     | V     | –     |
| Serial Input                      |                 |                           |                      |                       |                       |       |       |
| Serial Input Common Mode Voltage  | –               | 50Ω load                  | 2.5                  | SDI_VDD<br>-(0.75/2)  | SDI_VDD<br>-(0.55/2)  | V     | –     |
| Serial Output                     |                 |                           |                      |                       |                       |       |       |
| Serial Output Common Mode Voltage | –               | 50Ω load                  | BUFF_VDD<br>-(0.6/2) | BUFF_VDD<br>-(0.45/2) | BUFF_VDD<br>-(0.35/2) | V     | –     |

**NOTES:**

1. The output drive strength of the digital outputs can be programmed through the host interface. Please see [Table 4-17: Configuration and Status Registers](#), register 06Dh for details.

## 2.4 AC Electrical Characteristics

**Table 2-4: AC Electrical Characteristics**

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                                         | Symbol             | Conditions             |      | Min  | Typ | Max   | Units | Notes |
|---------------------------------------------------|--------------------|------------------------|------|------|-----|-------|-------|-------|
| System                                            |                    |                        |      |      |     |       |       |       |
| Device Latency:<br>SMPTE mode,<br>IOPROC_EN = 1   | –                  | 3G (Level A)           |      | 44   | –   | 48    | PCLK  | –     |
|                                                   |                    | 3G (Level B)           |      | 108  | –   | 116   | PCLK  | –     |
|                                                   |                    | HD                     |      | 44   | –   | 48    | PCLK  | –     |
|                                                   |                    | SD                     |      | 44   | –   | 48    | PCLK  | –     |
| Device Latency:<br>SMPTE mode,<br>IOPROC_EN = 0   | –                  | 3G (Level A)           |      | 33   | –   | 36    | PCLK  | –     |
|                                                   |                    | HD                     |      | 33   | –   | 36    | PCLK  | –     |
|                                                   |                    | SD                     |      | 32   | –   | 35    | PCLK  | –     |
| Device Latency:<br>SMPTE bypass,<br>IOPROC_EN = 0 | –                  | 3G (Level A)           |      | 6    | –   | 9     | PCLK  | –     |
|                                                   |                    | HD                     |      | 6    | –   | 9     | PCLK  | –     |
|                                                   |                    | SD                     |      | 5    | –   | 9     | PCLK  | –     |
| Device Latency:<br>DVB-ASI                        | –                  | SD                     |      | 12   | –   | 16    | PCLK  | –     |
| Reset Pulse Width                                 | t <sub>reset</sub> | –                      |      | 1    | –   | –     | ms    | –     |
| Parallel Output                                   |                    |                        |      |      |     |       |       |       |
| Parallel Clock Frequency                          | f <sub>PCLK</sub>  | –                      |      | 13.5 | –   | 148.5 | MHz   | –     |
| Parallel Clock Duty Cycle                         | DC <sub>PCLK</sub> | –                      |      | 45   | –   | 55    | %     | –     |
| Output Data Hold Time (1.8V)                      | t <sub>oh</sub>    | 3G 10-bit<br>6pF Cload | SPI  | 1.5  | –   | –     | ns    | 1     |
|                                                   |                    |                        | DBUS | 0.3  | –   | –     | ns    | 1     |
|                                                   |                    |                        | STAT | 0.3  | –   | –     | ns    | 1     |
|                                                   |                    | 3G 20-bit<br>6pF Cload | DBUS | 1.0  | –   | –     | ns    | 1     |
|                                                   |                    |                        | STAT | 1.0  | –   | –     | ns    | 1     |
|                                                   |                    | HD 10-bit<br>6pF Cload | DBUS | 1.0  | –   | –     | ns    | 1     |
|                                                   |                    |                        | STAT | 1.0  | –   | –     | ns    | 1     |
|                                                   |                    | HD 20-bit<br>6pF Cload | DBUS | 1.0  | –   | –     | ns    | 1     |
|                                                   |                    |                        | STAT | 1.0  | –   | –     | ns    | 1     |
|                                                   |                    | SD 10-bit<br>6pF Cload | DBUS | 19.4 | –   | –     | ns    | 1     |
|                                                   |                    |                        | STAT | 19.4 | –   | –     | ns    | 1     |
|                                                   |                    | SD 20-bit<br>6pF Cload | DBUS | 38.0 | –   | –     | ns    | 1     |
|                                                   |                    |                        | STAT | 38.0 | –   | –     | ns    | 1     |

**Table 2-4: AC Electrical Characteristics (Continued)**

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                     | Symbol   | Conditions              |      | Min  | Typ | Max  | Units | Notes |
|-------------------------------|----------|-------------------------|------|------|-----|------|-------|-------|
| Output Data Hold Time (3.3V)  | $t_{oh}$ | 3G 10-bit<br>6pF Cload  | SPI  | 1.5  | –   | –    | ns    | 2     |
|                               |          |                         | DBUS | 0.3  | –   | –    | ns    | 2     |
|                               |          |                         | STAT | 0.3  | –   | –    | ns    | 2     |
|                               |          | 3G 20-bit<br>6pF Cload  | DBUS | 1.0  | –   | –    | ns    | 2     |
|                               |          |                         | STAT | 1.0  | –   | –    | ns    | 2     |
|                               |          | HD 10-bit<br>6pF Cload  | DBUS | 1.0  | –   | –    | ns    | 2     |
|                               |          |                         | STAT | 1.0  | –   | –    | ns    | 2     |
|                               |          | HD 20-bit<br>6pF Cload  | DBUS | 1.0  | –   | –    | ns    | 2     |
|                               |          |                         | STAT | 1.0  | –   | –    | ns    | 2     |
|                               |          | SD 10-bit<br>6pF Cload  | DBUS | 19.4 | –   | –    | ns    | 2     |
|                               |          |                         | STAT | 19.4 | –   | –    | ns    | 2     |
|                               |          | SD 20-bit<br>6pF Cload  | DBUS | 38.0 | –   | –    | ns    | 2     |
|                               |          |                         | STAT | 38.0 | –   | –    | ns    | 2     |
| Output Data Delay Time (1.8V) | $t_{od}$ | 3G 10-bit<br>15pF Cload | SPI  | –    | –   | 14.0 | ns    | 3     |
|                               |          |                         | DBUS | –    | –   | 1.8  | ns    | 3     |
|                               |          |                         | STAT | –    | –   | 2.5  | ns    | 3     |
|                               |          | 3G 20-bit<br>15pF Cload | DBUS | –    | –   | 3.7  | ns    | 3     |
|                               |          |                         | STAT | –    | –   | 4.4  | ns    | 3     |
|                               |          | HD 10-bit<br>15pF Cload | DBUS | –    | –   | 3.7  | ns    | 3     |
|                               |          |                         | STAT | –    | –   | 4.4  | ns    | 3     |
|                               |          | HD 20-bit<br>15pF Cload | DBUS | –    | –   | 3.7  | ns    | 3     |
|                               |          |                         | STAT | –    | –   | 4.4  | ns    | 3     |
|                               |          | SD 10-bit<br>15pF Cload | DBUS | –    | –   | 22.2 | ns    | 3     |
|                               |          |                         | STAT | –    | –   | 22.2 | ns    | 3     |
|                               |          | SD 20-bit<br>15pF Cload | DBUS | –    | –   | 41.0 | ns    | 3     |
|                               |          |                         | STAT | –    | –   | 41.0 | ns    | 3     |

**Table 2-4: AC Electrical Characteristics (Continued)**

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                         | Symbol                         | Conditions                       |      | Min  | Typ | Max  | Units | Notes |
|-----------------------------------|--------------------------------|----------------------------------|------|------|-----|------|-------|-------|
| Output Data Delay Time (3.3V)     | t <sub>od</sub>                | 3G 10-bit<br>15pF Cload          | SPI  | –    | –   | 14.0 | ns    | 4     |
|                                   |                                |                                  | DBUS | –    | –   | 1.9  | ns    | 4     |
|                                   |                                |                                  | STAT | –    | –   | 2.2  | ns    | 4     |
|                                   |                                | 3G 20-bit<br>15pF Cload          | DBUS | –    | –   | 3.7  | ns    | 4     |
|                                   |                                |                                  | STAT | –    | –   | 4.1  | ns    | 4     |
|                                   |                                | HD 10-bit<br>15pF Cload          | DBUS | –    | –   | 3.7  | ns    | 4     |
|                                   |                                |                                  | STAT | –    | –   | 4.1  | ns    | 4     |
|                                   |                                | HD 20-bit<br>15pF Cload          | DBUS | –    | –   | 3.7  | ns    | 4     |
|                                   |                                |                                  | STAT | –    | –   | 4.1  | ns    | 4     |
|                                   |                                | SD 10-bit<br>15pF Cload          | DBUS | –    | –   | 22.2 | ns    | 4     |
|                                   |                                |                                  | STAT | –    | –   | 22.2 | ns    | 4     |
|                                   |                                | SD 20-bit<br>15pF Cload          | DBUS | –    | –   | 41.0 | ns    | 4     |
|                                   |                                |                                  | STAT | –    | –   | 41.0 | ns    | 4     |
| Output Data Rise/Fall Time (1.8V) | t <sub>r</sub> /t <sub>f</sub> | 3G 10-bit<br>6pF Cload           | STAT | –    | –   | 0.4  | ns    | 1     |
|                                   |                                |                                  | DBUS | –    | –   | 0.3  | ns    | 1     |
|                                   |                                | All other<br>modes<br>6pF Cload  | STAT | –    | –   | 0.4  | ns    | 1     |
|                                   |                                |                                  | DBUS | –    | –   | 0.4  | ns    | 1     |
|                                   |                                | 3G 10-bit<br>15pF Cload          | STAT | –    | –   | 1.5  | ns    | 3     |
|                                   |                                |                                  | DBUS | –    | –   | 1.1  | ns    | 3     |
|                                   |                                | All other<br>modes<br>15pF Cload | STAT | –    | –   | 1.5  | ns    | 3     |
|                                   |                                |                                  | DBUS | –    | –   | 1.4  | ns    | 3     |
| Output Data Rise/Fall Time (3.3V) | t <sub>r</sub> /t <sub>f</sub> | 3G 10-bit<br>6pF Cload           | STAT | –    | –   | 0.5  | ns    | 2     |
|                                   |                                |                                  | DBUS | –    | –   | 0.4  | ns    | 2     |
|                                   |                                | All other<br>modes<br>6pF Cload  | STAT | –    | –   | 0.5  | ns    | 2     |
|                                   |                                |                                  | DBUS | –    | –   | 0.4  | ns    | 2     |
|                                   |                                | 3G 10-bit<br>15pF Cload          | STAT | –    | –   | 1.6  | ns    | 4     |
|                                   |                                |                                  | DBUS | –    | –   | 1.5  | ns    | 4     |
|                                   |                                | All other<br>modes<br>15pF Cload | STAT | –    | –   | 1.6  | ns    | 4     |
|                                   |                                |                                  | DBUS | –    | –   | 1.4  | ns    | 4     |
| Serial Digital Input              |                                |                                  |      |      |     |      |       |       |
| Serial Input Data Rate            | DR <sub>SDI</sub>              | –                                |      | 0.27 | –   | 2.97 | Gb/s  | –     |
| Serial Input Swing                | ΔV <sub>SDI</sub>              | Differential with 100Ω<br>load   |      | 500  | 800 | 1100 | mVp-p | –     |

**Table 2-4: AC Electrical Characteristics (Continued)**

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                            | Symbol             | Conditions                                 | Min  | Typ | Max  | Units   | Notes |
|--------------------------------------|--------------------|--------------------------------------------|------|-----|------|---------|-------|
| Serial Input Jitter Tolerance        | IJT                | Nominal loop bandwidth<br>Square wave mod. | 0.7  | 0.8 | –    | UI      | –     |
| <b>Serial Digital Output</b>         |                    |                                            |      |     |      |         |       |
| Serial Output Data Rate              | DR <sub>SDO</sub>  | –                                          | 0.27 | –   | 2.97 | Gb/s    | –     |
| Serial Output Swing                  | $\Delta V_{SDO}$   | Differential with 100 $\Omega$ load        | 350  | –   | 600  | mVp-p   | –     |
| Serial Output Rise Time<br>20% ~ 80% | tr <sub>SDO</sub>  | –                                          | –    | –   | 180  | ps      | –     |
| Serial Output Fall Time<br>20% ~ 80% | tf <sub>SDO</sub>  | –                                          | –    | –   | 180  | ps      | –     |
| Serial Output Intrinsic Jitter       | t <sub>OJ</sub>    | SMPTE colour bar 3G signal                 | –    | –   | 100  | ps      | –     |
|                                      |                    | SMPTE colour bar HD signal                 | –    | –   | 100  | ps      | –     |
|                                      |                    | SMPTE colour bar SD signal                 | –    | –   | 400  | ps      | –     |
| Serial Output Duty Cycle Distortion  | DCD <sub>SDO</sub> | 3G                                         | –    | 10  | –    | ps      | –     |
|                                      |                    | HD                                         | –    | 10  | –    | ps      | –     |
|                                      |                    | SD                                         | –    | 20  | –    | ps      | –     |
| Synchronous lock time                | –                  | –                                          | –    | –   | 25   | $\mu$ s | –     |
| Asynchronous lock time               | –                  | Manual mode, noise immunity disabled       | 100  | –   | 350  | $\mu$ s | –     |
|                                      |                    | Auto mode, noise immunity disabled         | 100  | –   | 600  | $\mu$ s | 5     |
|                                      |                    | Noise immunity enabled                     | 100  | –   | 1200 | $\mu$ s | 5     |
| Lock time from power-up              | –                  | After 20 minutes at -20°C                  | –    | 325 |      | ms      | –     |

**Table 2-4: AC Electrical Characteristics (Continued)**

Guaranteed over recommended operating conditions unless otherwise noted.

| Parameter                                                                                                                     | Symbol             | Conditions                           | Min   | Typ | Max | Units | Notes |
|-------------------------------------------------------------------------------------------------------------------------------|--------------------|--------------------------------------|-------|-----|-----|-------|-------|
| <b>GSPI</b>                                                                                                                   |                    |                                      |       |     |     |       |       |
| GSPI Input Clock Frequency                                                                                                    | $f_{\text{SCLK}}$  | 50% levels<br>3.3V or 1.8V operation | –     | –   | 60  | MHz   | 6     |
| GSPI Input Clock Duty Cycle                                                                                                   | $DC_{\text{SCLK}}$ |                                      | 40    | 50  | 60  | %     | 6     |
| GSPI Input Data Setup Time                                                                                                    | –                  |                                      | 1.5   | –   | –   | ns    | 6     |
| GSPI Input Data Hold Time                                                                                                     | –                  |                                      | 1.5   | –   | –   | ns    | 6     |
| GSPI Output Data Hold Time                                                                                                    | –                  |                                      | 1.5   | –   | –   | ns    | 6     |
| $\overline{\text{CS}}$ low before SCLK rising edge                                                                            | –                  |                                      | 1.5   | –   | –   | ns    | 6     |
| Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle | –                  |                                      | 37.1  | –   | –   | ns    | 6     |
| Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle  | –                  |                                      | 148.4 | –   | –   | ns    | 6     |
| $\overline{\text{CS}}$ high after SCLK falling edge                                                                           | –                  |                                      | 37.1  | –   | –   | ns    | 6     |

**NOTES:**

1. 1.89V and 0°C.
2. 3.47V and 0°C.
3. 1.71V and 85°C
4. 3.13V and 85°C
5. 720\_24p format requires a longer lock time
6. Timing parameters defined in [Section 4.19.3](#)

### 3. Input/Output Circuits

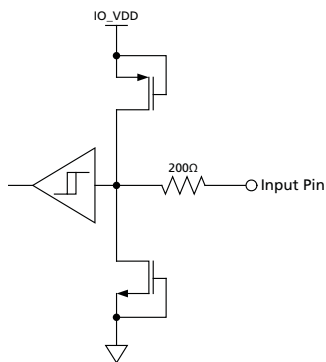


Figure 3-1: Digital Input Pin with Schmitt Trigger (20BIT/10BIT,  $\overline{CS\_TMS}$ , SW\_EN, IOPROC\_EN/ $\overline{DIS}$ , JTAG/HOST, RC\_BYP, RESET\_TRST, SCLK\_TCK, SDIN\_TDI, SDO\_EN/ $\overline{DIS}$ , STANDBY, TIM\_861)

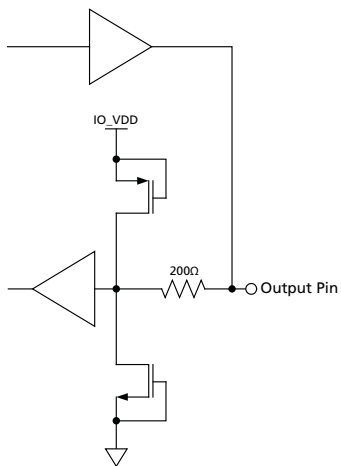


Figure 3-2: Bidirectional Digital Input/Output Pin - Configured to Output unless in Reset Mode. (DVB\_ASI, SMPTE\_BYPASS)

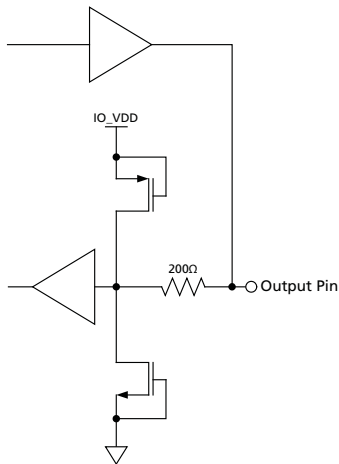


Figure 3-3: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to output unless in Reset Mode; in which case they are high-impedance. The drive strength can be set by writing to address 06Dh in the host interface register. (DOUT0, DOUT1, DOUT2, DOUT3, DOUT4, DOUT5, DOUT6, DOUT7, DOUT8, DOUT9, SDOUT\_TDO, STAT0, STAT1, STAT2, STAT3, STAT4, STAT5, XTAL\_OUT, DOUT10, DOUT11, DOUT12, DOUT13, DOUT14, DOUT15, DOUT16, DOUT17, DOUT18, DOUT19, PCLK)

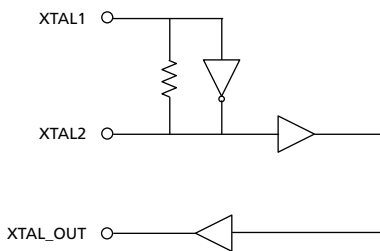


Figure 3-4: XTAL1/XTAL2/XTAL-OUT

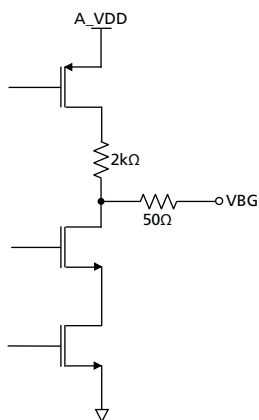


Figure 3-5: VBG

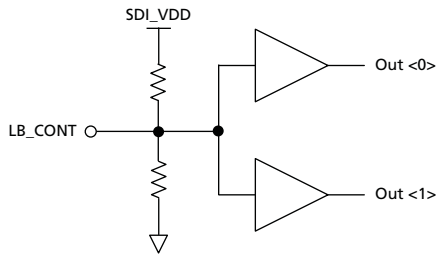


Figure 3-6: LB\_CONT

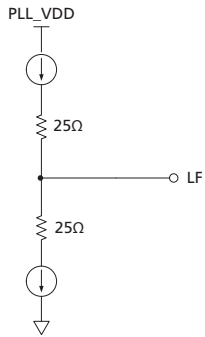


Figure 3-7: Loop Filter

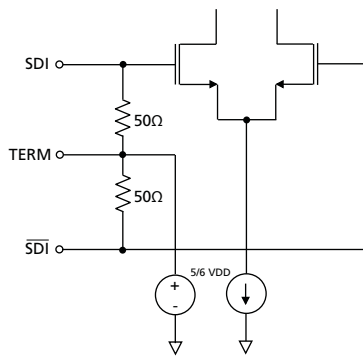


Figure 3-8: SDI/SDI and TERM

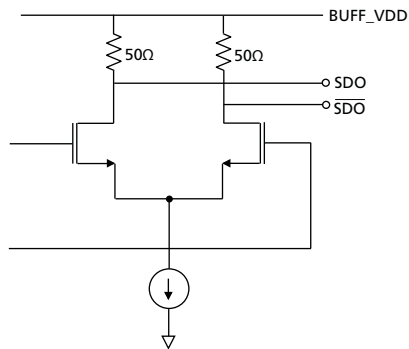


Figure 3-9: SDO/SDO



## 4.2.2 Level B Mapping

The 2 x 292 HD SDI interface - this can be two distinct links running at 1.5Gb/s or one 3Gb/s link formatted according to SMPTE 292 on two 10-bit links (Y/C interleaved). For 1080p/50/59.94/60 4:2:2 video formats, each link should be line-interleaved as per SMPTE 372M. See [Figure 4-2](#):

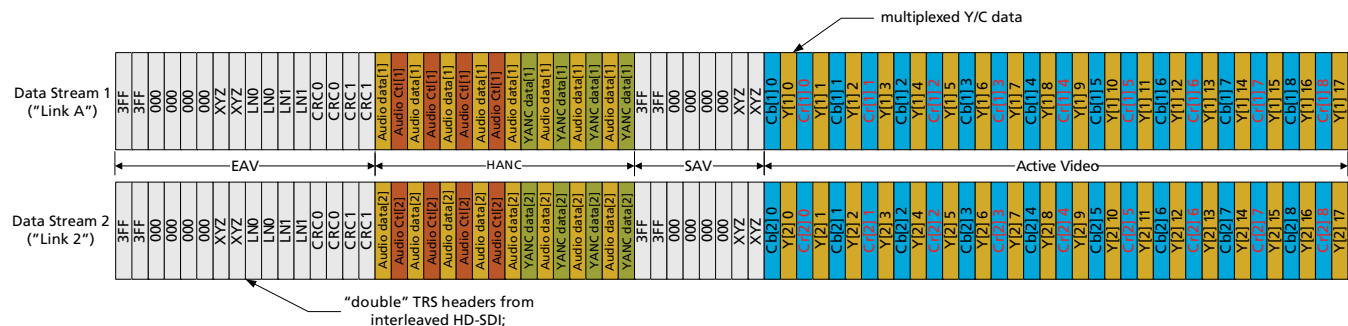


Figure 4-2: Level B Mapping

The GS2960A distinguishes between Level A and Level B mappings at 3Gb/s. When Level B data is detected, each 10-bit link is demultiplexed into its individual component streams, and most video processing features, including error detection and correction are enabled separately for Data Stream 1 and Data Stream 2 (Link A and Link B, respectively). Note that ancillary data extraction can only be enabled for one link for 3Gb/s Level B data. Data Stream 1 or Data Stream 2 can be selected via the host interface.

## 4.3 Serial Digital Input

The GS2960A can accept serial digital inputs compliant with SMPTE 424M, SMPTE 292 and SMPTE 259M-C. The serial digital input buffer features 50Ω input termination and can be DC-coupled to Gennum's 3Gb/s-capable equalizers.

## 4.4 Serial Digital Loop-Through Output

The GS2960A contains a 100Ω differential serial output buffer which can be configured to output either a retimed or a buffered version of the serial digital input. The SDO and  $\overline{\text{SDO}}$  outputs of this buffer can interface directly to a 3Gb/s-capable, SMPTE compliant Gennum cable driver. See [5.1 Typical Application Circuit](#) on [page 94](#).

When the  $\overline{\text{RC\_BYP}}$  pin is set HIGH, the serial digital output is the re-timed version of the serial input.

When the  $\overline{\text{RC\_BYP}}$  pin is set LOW, the serial digital output is simply the buffered version of the serial input, bypassing the internal reclocker.

The output can be disabled by setting the  $\text{SDO\_EN}/\overline{\text{DIS}}$  pin LOW. The output is also disabled when the STANDBY pin is asserted HIGH. When the output is disabled, both SDO and  $\overline{\text{SDO}}$  pins are set to VDD and remain static.

The SDO output is muted when the  $\overline{\text{RC\_BYP}}$  pin is set HIGH and the PLL is unlocked (LOCKED pin is LOW). When muted, the output is held static at logic '0' or logic '1'.

**Table 4-1: Serial Digital Output**

| SDO_EN/ $\overline{\text{DIS}}$ | $\overline{\text{RC\_BYP}}$ | SDO/ $\overline{\text{SDO}}$ |
|---------------------------------|-----------------------------|------------------------------|
| 0                               | X                           | Disabled                     |
| 1                               | 1                           | Re-timed                     |
| 1                               | 0                           | Buffered (not re-timed)      |

NOTE: The serial digital output is muted when the GS2960A is unlocked.

## 4.5 Serial Digital Reclocker

The GS2960A includes both a PLL stage and a sampling stage.

The PLL is comprised of two distinct loops:

- A coarse frequency acquisition loop sets the centre frequency of the integrated Voltage Controlled Oscillator (VCO) using an external 27MHz reference clock
- A fine frequency and phase locked loop aligns the VCO's phase and frequency to the input serial digital stream

The frequency lock loop results in a very fast lock time.

The sampling stage re-times the serial digital input with the locked VCO clock. This generates a clean serial digital stream, which may be output on the SDO/ $\overline{\text{SDO}}$  output pins and converted to parallel data for further processing. Parallel data is not affected by  $\overline{\text{RC\_BYP}}$ . Only the SDO is affected by this pin.

### 4.5.1 PLL Loop Bandwidth

The fine frequency and phase lock loop in the GS2960A reclocker is non-linear. The PLL loop bandwidth scales with the jitter amplitude of the input data stream; automatically reduces bandwidth in response to higher jitter. This allows the PLL to reject more of the jitter in the input data stream and produce a very clean reclocked output.

The loop bandwidth of the GS2960A PLL is defined with 0.2UI input jitter. The bandwidth is controlled by the LB\_CONT pin. Under nominal conditions, with the LB\_CONT pin floating and 0.2UI input jitter applied, the loop bandwidth is set to 1/1000 of the frequency of the input data stream. Connecting the LB\_CONT pin to 3.3V reduces the bandwidth to half of the nominal setting. Connecting the LB\_CONT pin to GND increases the bandwidth to double the nominal setting. [Table 4-2](#) below summarizes this information.

**Table 4-2: PLL Loop Bandwidth**

| Input Data Rate | LB_CONT Pin Connection | Loop Bandwidth (MHz) <sup>1</sup> |
|-----------------|------------------------|-----------------------------------|
| SD              | 3.3V                   | 0.135                             |
|                 | Floating               | 0.27                              |
|                 | 0V                     | 0.54                              |

**Table 4-2: PLL Loop Bandwidth (Continued)**

| Input Data Rate | LB_CONT Pin Connection | Loop Bandwidth (MHz) <sup>1</sup> |
|-----------------|------------------------|-----------------------------------|
| HD              | 3.3V                   | 0.75                              |
|                 | Floating               | 1.5                               |
|                 | 0V                     | 3.0                               |
| 3G              | 3.3V                   | 1.5                               |
|                 | Floating               | 3.0                               |
|                 | 0V                     | 6.0                               |

<sup>1</sup>Measured with 0.2UI input jitter applied

## 4.6 External Crystal/Reference Clock

The GS2960A requires an external 27MHz reference clock for correct operation. This reference clock is generated by connecting a crystal to the XTAL1 and XTAL2 pins of the device. See [Application Reference Design on page 94](#). [Table 4-3](#) shows XTAL characteristics.

Alternately, a 27MHz external clock source can be connected to the XTAL1 pin of the device, as shown in [Figure 4-3](#).

The frequency variation of the crystal including aging, supply and temperature variation should be less than +/-100ppm.

The equivalent series resistance (or motional resistance) should be a maximum of 50Ω.

The external crystal is used in the frequency acquisition process. It has no impact on the output jitter performance of the part when the part is locked to incoming data. Because of this, the only key parameter is the frequency variation of the crystal that is stated above.

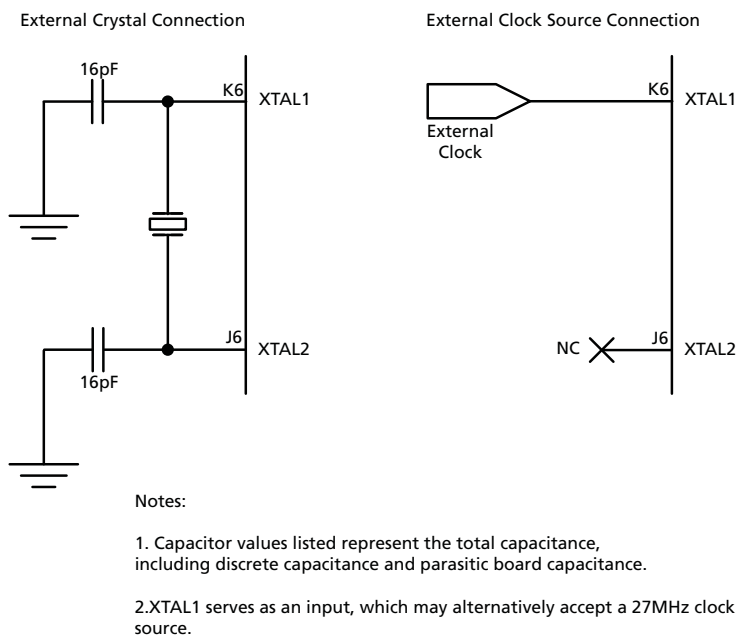


Figure 4-3: 27MHz Clock Sources

Table 4-3: Input Clock Requirements

| Parameter                                   | Min               | Typ | Max                 | UOM  | Notes |
|---------------------------------------------|-------------------|-----|---------------------|------|-------|
| XTAL1 Low Level Input Voltage ( $V_{il}$ )  | –                 | –   | 20% of $V_{DD\_IO}$ | V    | 3     |
| XTAL1 High Level Input Voltage ( $V_{ih}$ ) | 80% of $V_{DDIO}$ | –   | –                   | V    | 3     |
| XTAL1 Input Slew Rate                       | 2                 | –   | –                   | V/ns | 3     |
| XTAL1 to XOUT Prop. Delay (High to Low)     | 1.3               | 1.5 | 2.3                 | ns   | 3     |
| XTAL1 to XOUT Prop. Delay (Low to High)     | 1.3               | 1.6 | 2.3                 | ns   | 3     |

NOTES:

Valid when the cell is used to buffer an external clock source which is connected to the XTAL1 pin, then nothing should be connected to the XTAL2 pin.

4.7 Lock Detect

The LOCKED output signal is available by default on the STAT3 output pin, but may be programmed to be output through any one of the six programmable multi-functional pins of the device; STAT[5:0].

The LOCKED output signal is set HIGH by the Lock Detect block under the following conditions:

**Table 4-4: Lock Detect Conditions**

| Mode of Operation                           | Mode Setting                                                                                                                                                     | Condition for Locked                                                                                                                                                                                           |
|---------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Data-Through Mode                           | $\overline{\text{SMPTE\_BYPASS}} = \text{LOW}$<br>$\text{DVB\_ASI} = \text{LOW}$                                                                                 | Reclocker PLL is locked.                                                                                                                                                                                       |
| SMPTE Mode                                  | $\overline{\text{SMPTE\_BYPASS}} = \text{HIGH}$<br>$\text{DVB\_ASI} = \text{LOW}$                                                                                | Reclocker PLL is locked. Two consecutive TRS words are detected in a two-line window.                                                                                                                          |
| SMPTE Mode with Lock Noise-Immunity Enabled | $\overline{\text{SMPTE\_BYPASS}} = \text{HIGH}$<br>$\text{DVB\_ASI} = \text{LOW}$<br>Bit 0x085[10] set to 1<br>$\text{AUTO}/\overline{\text{MAN}} = \text{HIGH}$ | Reclocker PLL is locked. Two consecutive TRS words are detected in a two-line window. The last two detected TRS words must have the same alignment.<br><br>NOTE: Auto mode only. Not supported in Manual mode. |
| DVB_ASI Mode                                | $\overline{\text{SMPTE\_BYPASS}} = \text{LOW}$<br>$\text{DVB\_ASI} = \text{HIGH}$<br>Bit $\text{AUTO}/\overline{\text{MAN}} = \text{LOW}$                        | Reclocker PLL is locked. 32 consecutive DVB_ASI words with no errors are detected within a 128-word window.                                                                                                    |

**NOTE 1:** The part will lock to ASI Auto mode, but could falsely unlock for some ASI input patterns.

**NOTE 2:** In Standby mode, the reclocker PLL unlocks. However, the LOCKED signal retains whatever state it previously held. So, if before Standby assertion, the LOCKED signal is HIGH, then during standby, it remains HIGH regardless of the status of the PLL.

### 4.7.1 Asynchronous Lock

The lock detection algorithm is a continuous process, beginning at device power-up or after a system reset. It continues until the device is powered down or held in reset.

The device first determines if a valid serial digital input signal has been presented to the device. If no valid serial data stream has been detected, the serial data into the device is considered invalid, and the LOCKED signal is LOW.

Once a valid input signal has been detected, the asynchronous lock algorithm enters a “hunt” phase, in which the device attempts to detect the presence of either TRS words or DVB-ASI sync words.

By default, the device powers up in auto mode (the  $\text{AUTO}/\overline{\text{MAN}}$  bit in the host interface is set HIGH). In this mode, the device operating frequency toggles between 3G, HD and SD rates as it attempts to lock to the incoming data rate. The PCLK output continues to operate, and the frequency may switch between 148.5MHz, 74.25MHz, 27MHz and 13.5MHz.

When the device is operating in manual mode ( $\text{AUTO}/\overline{\text{MAN}}$  bit in the host interface is LOW), the operating frequency needs to be set through the host interface using the RATE\_DET[1:0] bits. In this mode, the asynchronous lock algorithm does not toggle the operating rate of the device and attempts to lock within a single standard. Lock is achieved within three lines of the selected standard.

## 4.7.2 Signal Interruption

The device tolerates a signal interruption of up to 10µs without unlocking, as long as no TRS words are deleted by this interruption. If a signal interruption of greater than 10µs is detected, the lock detection algorithm may lose the current data rate, and LOCKED will de-assert until the data rate is re-acquired by the lock detection block.

## 4.8 SMPTE Functionality

### 4.8.1 Descrambling and Word Alignment

The GS2960A performs NRZI to NRZ decoding and data descrambling according to SMPTE 424M/SMPTE 292/SMPTE 259M-C and word aligns the data to TRS sync words.

When operating in Manual mode (AUTO/ $\overline{\text{MAN}}$  bit in the host interface is set LOW), the device only carries out SMPTE decoding, descrambling and word alignment when the  $\overline{\text{SMPTE\_BYPASS}}$  pin is set HIGH and the DVB\_ASI pin is set LOW.

When operating in Auto mode (AUTO/ $\overline{\text{MAN}}$  bit in the host interface is set HIGH), the GS2960A carries out descrambling and word alignment to enable the detection of TRS sync words. When two consecutive valid TRS words (SAV and EAV), with the same bit alignment have been detected, the device word-aligns the data to the TRS ID words.

TRS ID word detection is a continuous process. The device remains in SMPTE mode until TRS ID words fail to be detected.

**NOTE 1:** Both 8-bit and 10-bit TRS headers are identified by the device.

**NOTE 2:** In 3G Level B mode, the device only supports Data Stream 1 and Data Stream 2 having the same bit width (example: both data streams contain 8-bit data, or both data streams contain 10-bit data). If the bit widths between the two data streams are different, the GS2960A cannot word align the input stream, and remains in Data-Through mode.

# 4.9 Parallel Data Outputs

The parallel data outputs are aligned to the rising edge of the PCLK.

## 4.9.1 Parallel Data Bus Buffers

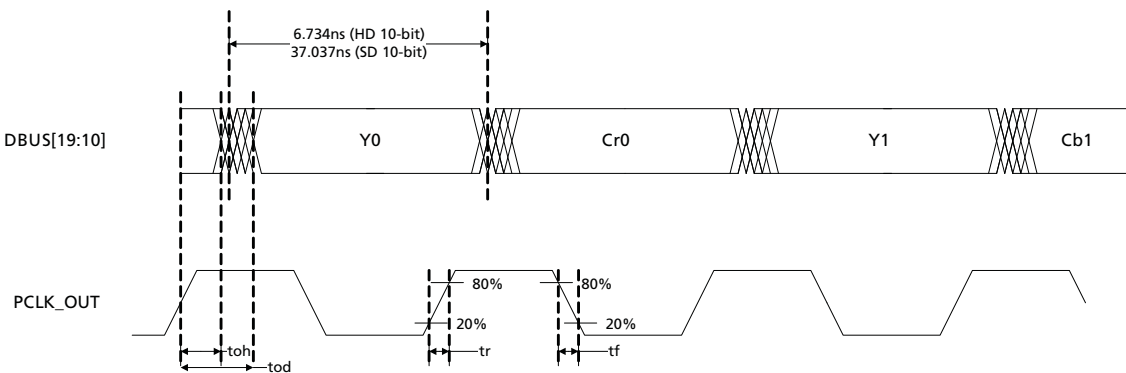
The parallel data bus, status signal outputs and control signal input pins are all connected to high-impedance buffers.

The device supports 1.8 or 3.3V (LVTTTL and LVCMOS levels) supplied at the IO\_VDD and IO\_GND pins.

All output buffers (including the PCLK output), are set to high-impedance in Reset mode ( $\overline{\text{RESET\_TRST}} = \text{LOW}$ ).

### I/O Timing Specs:

#### 10-bit SDR Mode:



| 10bHD Mode |         |             |       |         |             |       |         |             |       |         |             |       |
|------------|---------|-------------|-------|---------|-------------|-------|---------|-------------|-------|---------|-------------|-------|
|            | 3.3V    |             |       |         |             |       | 1.8V    |             |       |         |             |       |
|            | toh     | tr/tf (min) | Cload | tod     | tr/tf (max) | Cload | toh     | tr/tf (min) | Cload | tod     | tr/tf (max) | Cload |
| dbus       | 1.000ns | 0.400ns     | 6 pF  | 3.700ns | 1.400ns     | 15 pF | 1.000ns | 0.400ns     | 6 pF  | 3.700ns | 1.400ns     | 15 pF |
| stat       | 1.000ns | 0.500ns     |       | 4.100ns | 1.600ns     |       | 1.000ns | 0.400ns     |       | 4.400ns | 1.500ns     |       |

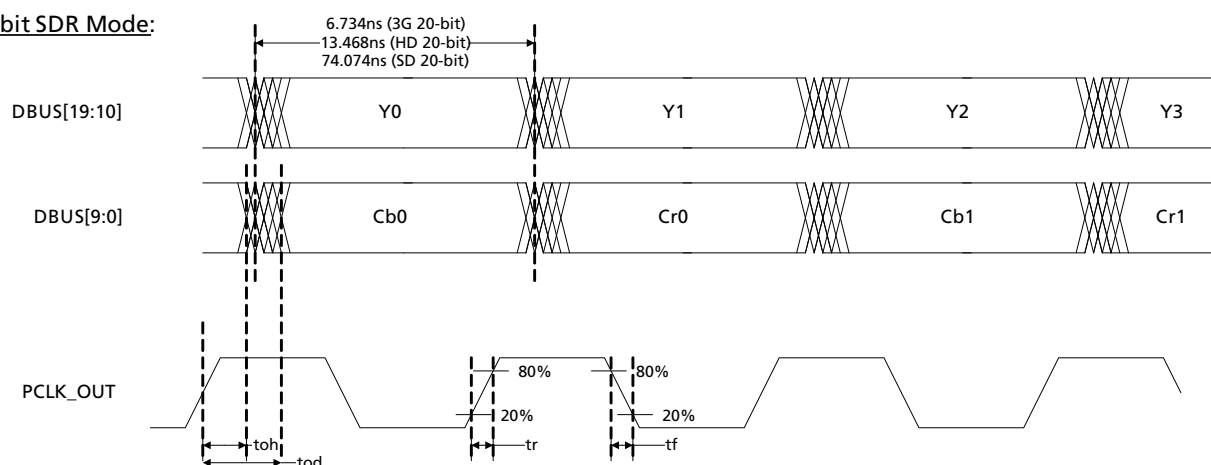
  

| 10bSD Mode |          |             |       |          |             |       |          |             |       |          |             |       |
|------------|----------|-------------|-------|----------|-------------|-------|----------|-------------|-------|----------|-------------|-------|
|            | 3.3V     |             |       |          |             |       | 1.8V     |             |       |          |             |       |
|            | toh      | tr/tf (min) | Cload | tod      | tr/tf (max) | Cload | toh      | tr/tf (min) | Cload | tod      | tr/tf (max) | Cload |
| dbus       | 19.400ns | 0.400ns     | 6 pF  | 22.200ns | 1.400ns     | 15 pF | 19.400ns | 0.400ns     | 6 pF  | 22.200ns | 1.400ns     | 15 pF |
| stat       | 19.400ns | 0.500ns     |       | 22.200ns | 1.600ns     |       | 19.400ns | 0.400ns     |       | 22.200ns | 1.500ns     |       |

Figure 4-4: PCLK to Data and Control Signal Output Timing - SDR Mode 1

## I/O Timing Specs:

### 20-bit SDR Mode:



| 20b3G and 20bHD Modes |                 |             |       |         |             |       |                 |             |       |         |             |       |
|-----------------------|-----------------|-------------|-------|---------|-------------|-------|-----------------|-------------|-------|---------|-------------|-------|
|                       | 3.3V            |             |       |         |             |       | 1.8V            |             |       |         |             |       |
|                       | to <sub>h</sub> | tr/tf (min) | Cload | tod     | tr/tf (max) | Cload | to <sub>h</sub> | tr/tf (min) | Cload | tod     | tr/tf (max) | Cload |
| dbus                  | 1.000ns         | 0.400ns     | 6 pF  | 3.700ns | 1.400ns     | 15 pF | 1.000ns         | 0.400ns     | 6 pF  | 3.700ns | 1.400ns     | 15 pF |
| stat                  | 1.000ns         | 0.500ns     |       | 4.100ns | 1.600ns     |       | 1.000ns         | 0.400ns     |       | 4.400ns | 1.500ns     |       |

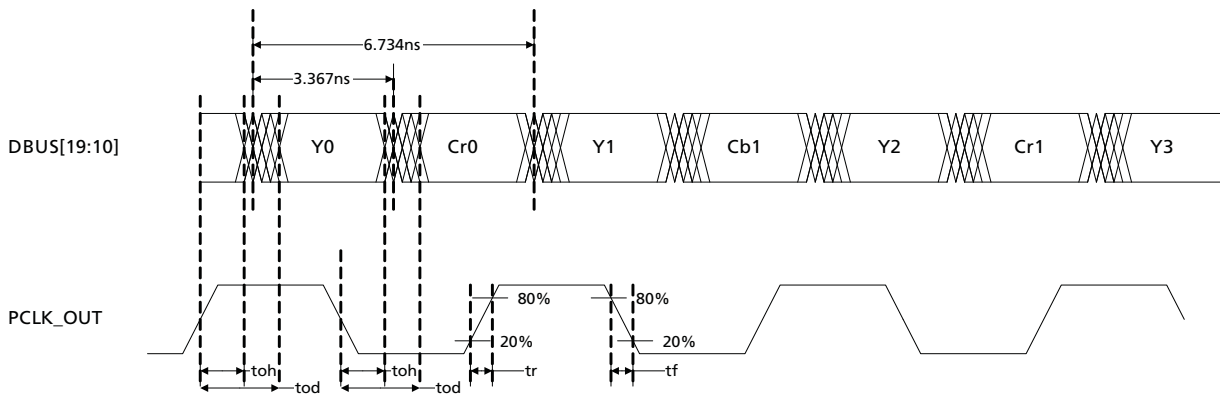
  

| 20bSD Mode |                 |             |       |          |             |       |                 |             |       |          |             |       |
|------------|-----------------|-------------|-------|----------|-------------|-------|-----------------|-------------|-------|----------|-------------|-------|
|            | 3.3V            |             |       |          |             |       | 1.8V            |             |       |          |             |       |
|            | to <sub>h</sub> | tr/tf (min) | Cload | tod      | tr/tf (max) | Cload | to <sub>h</sub> | tr/tf (min) | Cload | tod      | tr/tf (max) | Cload |
| dbus       | 38.000ns        | 0.400ns     | 6 pF  | 41.000ns | 1.400ns     | 15 pF | 38.000ns        | 0.400ns     | 6 pF  | 41.000ns | 1.400ns     | 15 pF |
| stat       | 38.000ns        | 0.500ns     |       | 41.000ns | 1.600ns     |       | 38.000ns        | 0.400ns     |       | 41.000ns | 1.500ns     |       |

Figure 4-5: PCLK to Data and Control Signal Output Timing - SDR Mode 2

## I/O Timing Specs:

### DDR Mode:



| 10b3G Mode |         |             |       |         |             |       |         |             |       |         |             |       |
|------------|---------|-------------|-------|---------|-------------|-------|---------|-------------|-------|---------|-------------|-------|
|            | 3.3V    |             |       |         |             |       | 1.8V    |             |       |         |             |       |
|            | toh     | tr/tf (min) | Cload | tod     | tr/tf (max) | Cload | toh     | tr/tf (min) | Cload | tod     | tr/tf (max) | Cload |
| dbus       | 0.450ns | 0.400ns     | 6 pF  | 1.900ns | 1.500ns     | 15 pF | 0.400ns | 0.300ns     | 6 pF  | 1.800ns | 1.100ns     | 15 pF |
| stat       | 0.450ns | 0.500ns     |       | 2.200ns | 1.600ns     |       | 0.450ns | 0.400ns     |       | 2.500ns | 1.500ns     |       |

Figure 4-6: PCLK to Data and Control Signal Output Timing - DDR Mode

The GS2960A has a 20-bit output parallel bus, which can be configured for different output formats as shown in [Table 4-5](#).

Table 4-5: GS2960A Output Video Data Format Selections

| Output Data Format               | Pin/Register Bit Settings |           |           |              |         | DOUT[9:0]  | DOUT[19:10]                          |
|----------------------------------|---------------------------|-----------|-----------|--------------|---------|------------|--------------------------------------|
|                                  | 20BIT /10BIT              | RATE_SELO | RATE_SEL1 | SMPTE_BYPASS | DVB-ASI |            |                                      |
| 20-bit demultiplexed HD format   | HIGH                      | LOW       | LOW       | HIGH         | LOW     | Chroma     | Luma                                 |
| 20-bit data output HD format     | HIGH                      | LOW       | LOW       | LOW          | LOW     | DATA       | DATA                                 |
| 20-bit demultiplexed SD format   | HIGH                      | HIGH      | X         | HIGH         | LOW     | Chroma     | Luma                                 |
| 20-bit data output SD format     | HIGH                      | HIGH      | X         | LOW          | LOW     | DATA       | DATA                                 |
| 10-bit multiplexed 3G DDR format | LOW                       | LOW       | HIGH      | HIGH         | LOW     | Driven LOW | Data Stream One/<br>Data Stream Two* |
| 10-bit multiplexed HD format     | LOW                       | LOW       | LOW       | HIGH         | LOW     | Driven LOW | Luma/Chroma                          |
| 10-bit data output HD format     | LOW                       | LOW       | LOW       | LOW          | LOW     | Driven LOW | DATA                                 |

**Table 4-5: GS2960A Output Video Data Format Selections (Continued)**

| Output Data Format             | Pin/Register Bit Settings |           |           |                            |         | DOUT[9:0]                                                                                                                                                                              | DOUT[19:10]      |
|--------------------------------|---------------------------|-----------|-----------|----------------------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
|                                | $\overline{20BIT/10BIT}$  | RATE_SELO | RATE_SEL1 | $\overline{SMPTE\_BYPASS}$ | DVB-ASI |                                                                                                                                                                                        |                  |
| 10-bit multiplexed SD format   | LOW                       | HIGH      | X         | HIGH                       | LOW     | Driven LOW                                                                                                                                                                             | Luma/Chroma      |
| 10-bit data output SD format   | LOW                       | HIGH      | X         | LOW                        | LOW     | Driven LOW                                                                                                                                                                             | DATA             |
| 20-bit demultiplexed 3G format | HIGH                      | LOW       | HIGH      | HIGH                       | LOW     | Data Stream Two*                                                                                                                                                                       | Data Stream One* |
| DVB-ASI format                 | LOW                       | HIGH      | X         | –                          | HIGH    | DOUT19 = WORD_ERR<br>DOUT18 = SYNC_OUT<br>DOUT17 = H_OUT<br>DOUT16 = G_OUT<br>DOUT15 = F_OUT<br>DOUT14 = E_OUT<br>DOUT13 = D_OUT<br>DOUT12 = C_OUT<br>DOUT11 = B_OUT<br>DOUT10 = A_OUT |                  |

\*In 3G mode, the data streams can be swapped at the output through the host interface.

NOTE: When in Auto Mode, swap RATE\_SEL with RATE\_DET.

## 4.9.2 Parallel Output in SMPTE Mode

When the device is operating in SMPTE mode ( $\overline{SMPTE\_BYPASS}$  = HIGH and DVB\_ASI = LOW), data is output in either Multiplexed or Demultiplexed form depending on the setting of the  $\overline{20bit/10bit}$  pin.

When operating in 20-bit mode ( $\overline{20bit/10bit}$  = HIGH), the output data is demultiplexed Luma and Chroma data for SD and HD data rates, and Data Stream 1 and Data Stream 2 for the 3G data.

When operating in 10-bit mode ( $\overline{20bit/10bit}$  = LOW), the output data is multiplexed Luma and Chroma data for SD and HD data rates, and multiplexed Data Stream 1 and Data Stream 2 for the 3G data. In this mode, the data is presented on the DOUT[19:10] pins, with DOUT[9:0] being forced LOW.

## 4.9.3 Output Data Format in DVB-ASI Mode

In DVB-ASI mode, the  $\overline{20bit/10bit}$  pin must be set LOW to configure the output parallel bus for 10-bit operation.

DVB-ASI mode is enabled when the AUTO/ $\overline{MAN}$  bit is LOW,  $\overline{SMPTE\_BYPASS}$  pin is LOW and the DVB\_ASI pin is HIGH.

The extracted 8-bit data is presented on DOUT[17:10] such that DOUT[17:10] = HOUT ~ AOUT, where AOUT is the least significant bit of the decoded transport stream data.

In addition, the DOUT19 and DOUT18 pins are configured as DVB-ASI status signals WORDERR and SYNCOUT respectively.

SYNCOUT is HIGH whenever a K28.5 sync character is output from the device.

WORDERR is HIGH whenever the device has detected a running disparity error or illegal code word.

#### 4.9.4 Parallel Output in Data-Through Mode

This mode is enabled when the  $\overline{\text{SMPTE\_BYPASS}}$  and DVB\_ASI pins are LOW.

In this mode, data is passed to the output bus without any decoding, descrambling or word-alignment.

The output data width (10-bit or 20-bit) is controlled by the setting of the 20bit/ $\overline{10\text{bit}}$  pin.

**NOTE:** In order to use Data-Through Mode, a 3G-B input signal must not be connected at the input of the device when the switch is made from Auto Mode to Data-Through Mode.

#### 4.9.5 Parallel Output Clock (PCLK)

The frequency of the PCLK output signal of the GS2960A is determined by the output data rate and the 20bit/ $\overline{10\text{bit}}$  pin setting. Table 4-6 lists the output signal formats according to the data format selected in Manual mode (AUTO/ $\overline{\text{MAN}}$  bit in the host interface is set LOW), or detected in Auto mode (AUTO/ $\overline{\text{MAN}}$  bit in the host interface is set HIGH).

**Table 4-6: GS2960A PCLK Output Rates**

| Output Data Format               | Pin/Control Bit Settings         |           |           |                                   |         | PCLK Rate               |
|----------------------------------|----------------------------------|-----------|-----------|-----------------------------------|---------|-------------------------|
|                                  | 20bit/ $\overline{10\text{bit}}$ | RATE_DET0 | RATE_DET1 | $\overline{\text{SMPTE\_BYPASS}}$ | DVB-ASI |                         |
| 20-bit demultiplexed HD format   | HIGH                             | LOW       | LOW       | HIGH                              | –       | 74.25 or 74.25/1.001MHz |
| 20-bit data output HD format     | HIGH                             | LOW       | LOW       | LOW                               | –       | 74.25 or 74.25/1.001MHz |
| 20-bit demultiplexed SD format   | HIGH                             | HIGH      | –         | HIGH                              | LOW     | 13.5MHz                 |
| 20-bit data output SD format     | HIGH                             | HIGH      | –         | LOW                               | LOW     | 13.5MHz                 |
| 20-bit demultiplexed 3G format   | HIGH                             | LOW       | HIGH      | HIGH                              | –       | 148.5 or 148.5/1.001MHz |
| 10-bit multiplexed 3G DDR format | LOW                              | LOW       | HIGH      | HIGH                              | LOW     | 148.5 or 148.5/1.001MHz |
| 10-bit multiplexed HD format     | LOW                              | LOW       | LOW       | HIGH                              | –       | 148.5 or 148.5/1.001MHz |
| 10-bit data output HD format     | LOW                              | LOW       | LOW       | LOW                               | –       | 148.5 or 148.5/1.001MHz |
| 10-bit multiplexed SD format     | LOW                              | HIGH      | –         | HIGH                              | LOW     | 27MHz                   |

**Table 4-6: GS2960A PCLK Output Rates (Continued)**

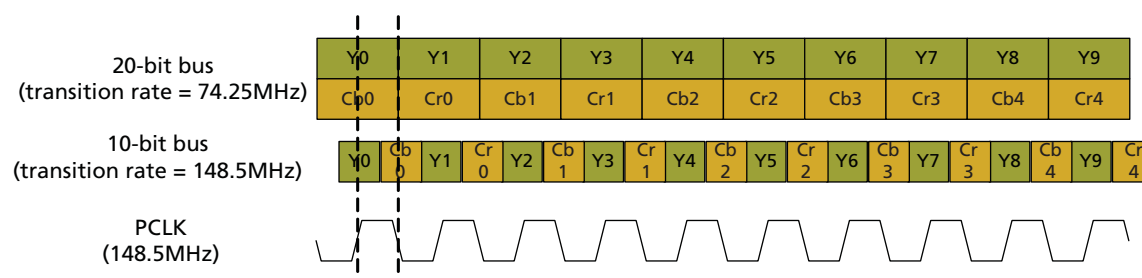
| Output Data Format              | Pin/Control Bit Settings |           |           |                               |         | PCLK Rate |
|---------------------------------|--------------------------|-----------|-----------|-------------------------------|---------|-----------|
|                                 | 20bit/<br>10bit          | RATE_DET0 | RATE_DET1 | <u>SMPTE</u><br><u>BYPASS</u> | DVB-ASI |           |
| 10-bit data output<br>SD format | LOW                      | HIGH      | –         | LOW                           | LOW     | 27MHz     |
| 10-bit ASI output<br>SD format  | LOW                      | HIGH      | –         | LOW                           | HIGH    | 27MHz     |

## 4.9.6 DDR Parallel Clock Timing

The GS2960A has the ability to transmit 10-bit parallel video data with a DDR (Dual Data Rate) pixel clock over a single-ended interface. DDR Mode can be enabled when the SDI data bandwidth is 3Gb/s. In this case, the 10-bit parallel data rate is 297Mb/s, and the frequency of the DDR clock is 148.5MHz (10-bit output in 3G mode).

The DDR pixel clock avoids the need to operate a high-drive pixel clock at 297MHz. This reduces power consumption, clock drive strength, and noise generation. It also enables easier board routing and avoids the need to use the higher-speed I/Os on FPGAs, which may require more expensive speed grades.

Figure 4-7 and Figure 4-8 show how the DDR interface operates. The pixel clock is transmitted at half the data rate, and the interleaved data is sampled at the receiver on both clock edges.



**Figure 4-7: DDR Video Interface - 3G Level A**

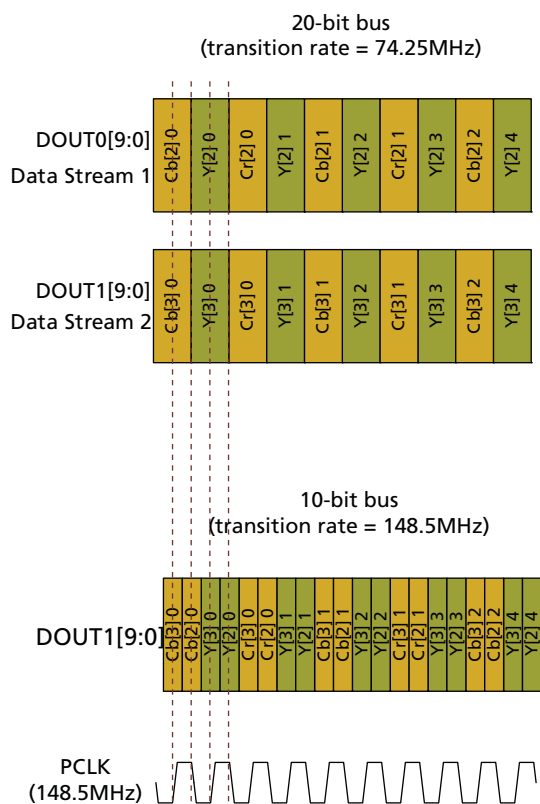


Figure 4-8: DDR Video Interface - 3G Level B

The GS2960A has the ability to shift the Setup/Hold window on the receive interface, by using an on-chip delay line to shift the phase of PCLK with respect to the data bus.

The timing of the PCLK output, relative to the data, can be adjusted through the host interface registers. Address 06Ch contains the delay line controls:

Bit[5] (DEL\_LINE\_CLK\_SEL) is a coarse delay adjustment that selects between the default (nominal) PCLK phase and a quadrature phase, for a 90° phase shift.

Bits[4:0] (DEL\_LINE\_OFFSET) comprise a fine delay adjustment to shift the PCLK in 40ps increments (typical conditions). The maximum fine delay adjustment is approximately 1.2ns under nominal conditions.

An example delay adjustment over min/typ/max conditions is illustrated in [Figure 4-9](#). The target delay is 0.84ns under typical conditions (approximately 45° PCLK phase shift), and requires a control word setting of 0x0014 for address 0x006C.

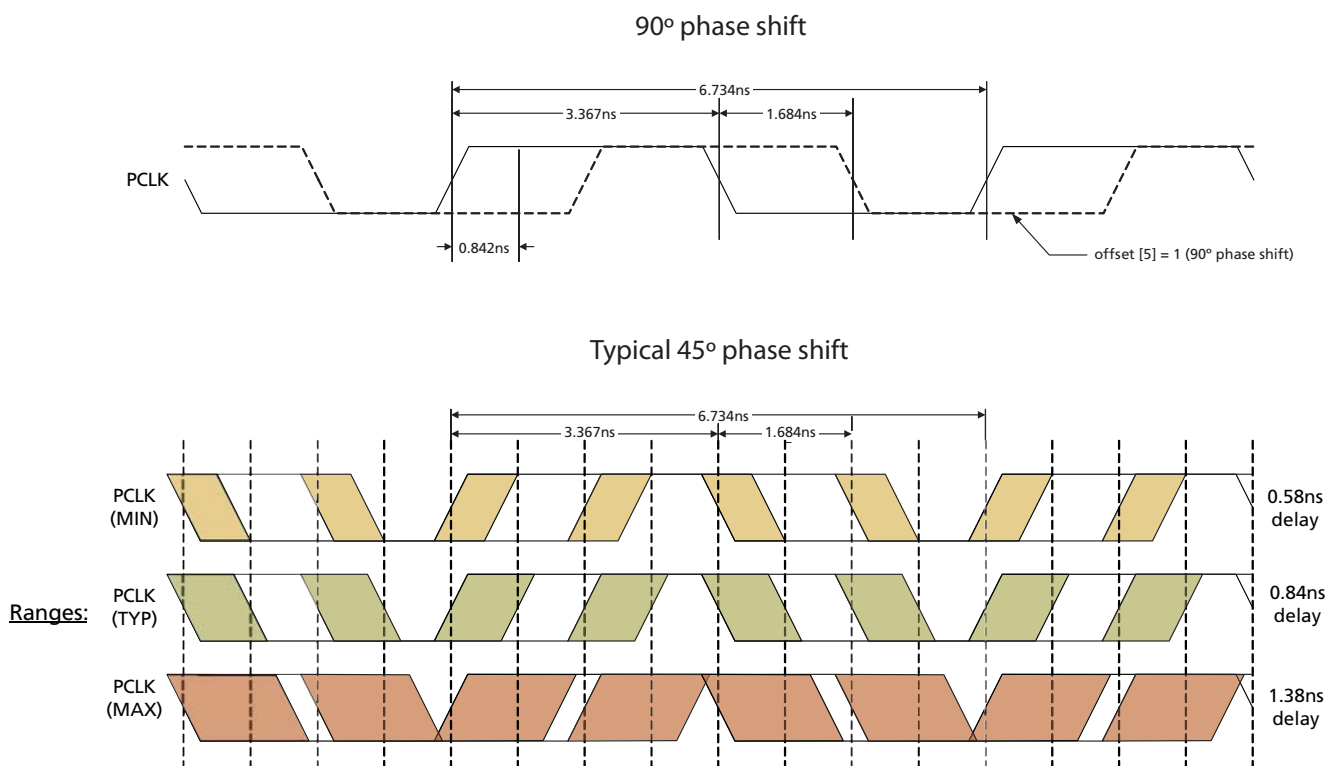


Figure 4-9: Delay Adjustment Ranges

## 4.10 Timing Signal Generator

The GS2960A has an internal timing signal generator which is used to generate digital FVH timing reference signals, to detect and correct certain error conditions and automatic video standard detection.

The timing signal generator is only operational in SMPTE mode ( $\overline{\text{SMPTE\_BYPASS}} = \text{HIGH}$ ).

The timing signal generator consists of a number of counters and comparators operating at video pixel and video line rates. These counters maintain information about the total line length, active line length, total number of lines per field/frame and total active lines per field/frame for the received video standard.

It takes one video frame to obtain full synchronization to the received video standard.

**NOTE:** Both 8-bit and 10-bit TRS words are identified by the device. Once synchronization has been achieved, the timing signal generator continues to monitor the received TRS timing information to maintain synchronization.

The timing signal generator re-synchronizes all pixel and line based counters on every received TRS ID. Note that for correct operation of the timing signal generator, the SW\_EN input pin must be set LOW, unless manual synchronous switching is enabled (Section 4.10.1).

## 4.10.1 Manual Switch Line Lock Handling

The principle of switch line lock handling is that the switching of synchronous video sources will only disturb the horizontal timing and alignment, whereas the vertical timing remains in synchronization - i.e. switching between video sources of the same format.

To account for the horizontal disturbance caused by a synchronous switch, the word alignment block and timing signal generator automatically re-synchronizes to the new timing immediately if the synchronous switch happens during the designated switch line, as defined in SMPTE recommended practice RP168-2002.

The device samples the SW\_EN pin on every PCLK cycle. When a Logic LOW to HIGH transition on this pin is detected anywhere within the active line, the word alignment block and timing signal generator re-synchronizes immediately to the next TRS word.

This allows the system to force immediate lock on any line, if the switch point is non-standard.

To ensure proper switch line lock handling, the SW\_EN signal should be asserted HIGH anywhere within the active portion of the line on which the switch has taken place, and should be held HIGH for approximately one video line. After this time period, SW\_EN should be de-asserted. SW\_EN should be held LOW during normal device operation.

**NOTE:** It is the rising edge of the SW\_EN signal, which generates the switch line lock re-synchronization. This edge must be in the active portion of the line containing the video switch point.

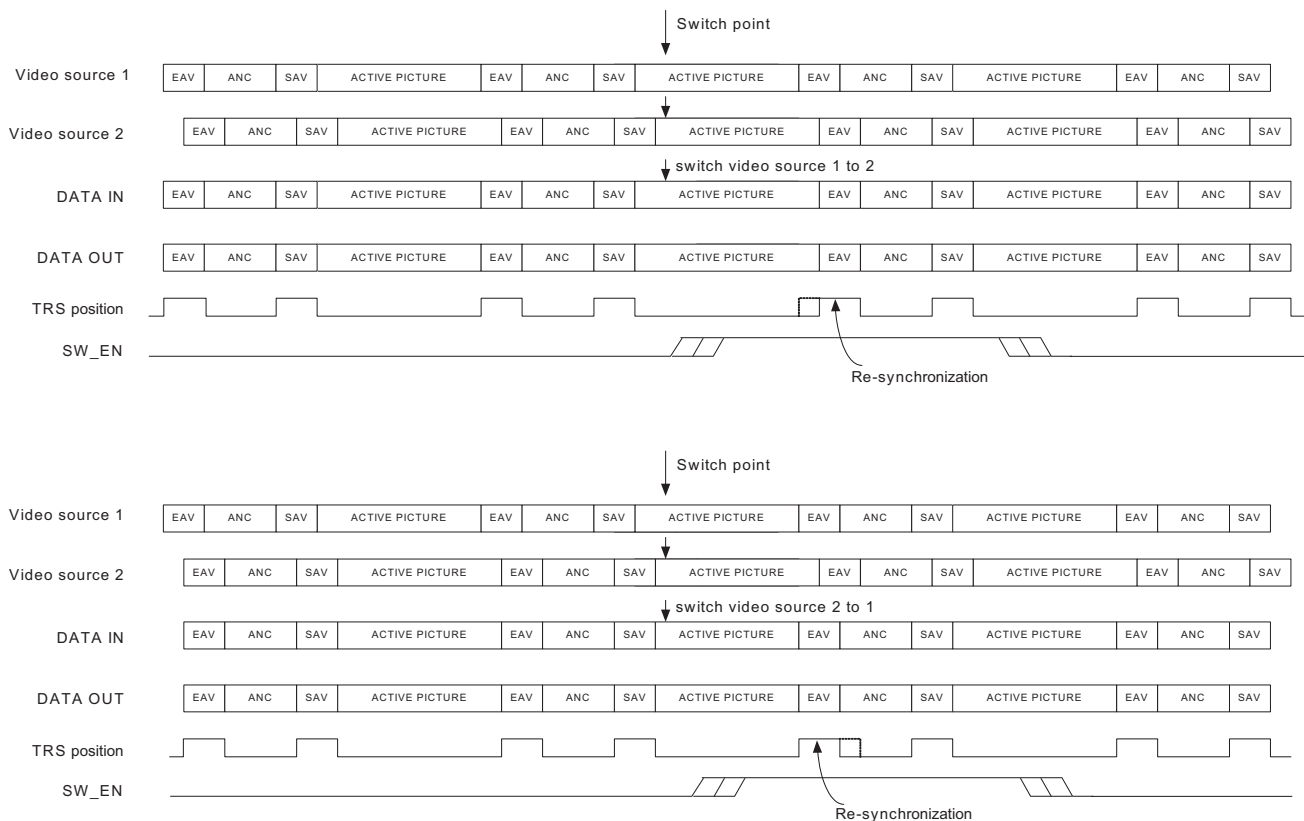


Figure 4-10: Switch Line Locking on a Non-Standard Switch Line

## 4.10.2 Automatic Switch Line Lock Handling

The synchronous switch point is defined for all major video standards in SMPTE RP168-2002. The device automatically re-synchronizes the word alignment block and timing signal generator at the switch point, based on the detected video standard.

The device, as described in [Section 4.10.1](#) and [Figure 4-10](#) above, implements the re-synchronization process automatically, every field/frame. The switch line is defined as follows:

- For 525 line interlaced systems: resynchronization takes place at then end of lines 10 & 273
- For 525 line progressive systems: resynchronization takes place at then end of line 10
- For 625 line interlaced systems: resynchronization takes place at then end of lines 6 & 319
- For 625 line progressive systems: resynchronization takes place at then end of line 6
- For 750 line progressive systems: resynchronization takes place at then end of line 7
- For 1125 line interlaced systems: resynchronization takes place at then end of lines 7 & 568
- For 1125 line progressive systems: resynchronization takes place at then end of line 7

**NOTE:** Unless indicated by SMPTE 352M payload identifier packets, the GS2960A does not distinguish between 1125-line progressive segmented-frame (PsF) video and 1125-line interlaced video operating at 25 or 30fps. However, PsF video operating at 24fps is detected by the device.

A full list of all major video standards and switching lines is shown in [Table 4-7](#).

## 4.10.3 Switch Line Lock Handling During Level B to Level A Conversion

When 3G data is detected by the GS2960A, and Level B to Level A conversion is enabled, the device only supports a limited phase offset between two synchronous video sources if a synchronous switch is implemented.

If the synchronous switch point results in an “extended” active video period, the GS2960A only re-synchronizes to the following TRS ID if the phase difference between the two sources is less than or equal to 10 $\mu$ s. If the phase difference is greater than 10 $\mu$ s, the GS2960A takes one additional line to re-synchronize. In this case, the user may observe a missing H pulse on the line following the switch line, on the H timing output.

Note that this 10 $\mu$ s constraint is only valid when Level B to Level A conversion is enabled, and only when the synchronous switch point results in an extended active video area.

**Table 4-7: Switch Line Position for Digital Systems**

| System | Frame Rate & Structure | Pixel Structure |         | Signal Standard | Parallel Interface | Serial Interface | Line No. |      |  |     |   |
|--------|------------------------|-----------------|---------|-----------------|--------------------|------------------|----------|------|--|-----|---|
| 1125   | 60/P                   | 1920x1080       | 4:2:2   | 274M + RP211    |                    | 292              | 7        |      |  |     |   |
|        | 50/P                   |                 |         | 274M + RP211    |                    |                  | 7/569    |      |  |     |   |
|        | 60/I                   |                 |         | 274M + RP211    |                    |                  |          |      |  |     |   |
|        | 50/I                   |                 |         | 274M + RP211    |                    |                  |          |      |  |     |   |
|        | 30/P                   |                 |         | 274M + RP211    |                    |                  |          |      |  |     |   |
|        | 25/P                   |                 |         | 274M + RP211    |                    |                  |          |      |  |     |   |
|        | 24/P                   |                 |         | 274M + RP211    |                    |                  |          |      |  |     |   |
|        | 30/PsF                 |                 |         | 274M + RP211    |                    |                  |          |      |  |     |   |
|        | 25/PsF                 |                 |         | 274M + RP211    |                    |                  |          |      |  |     |   |
|        | 24/PsF                 |                 |         | 274M + RP211    |                    |                  |          |      |  |     |   |
|        | 750                    |                 |         | 60/P            | 1280x720           |                  | 4:2:2    | 296M |  | 292 | 7 |
|        |                        |                 |         | 50/P            |                    |                  |          | 296M |  |     |   |
| 30/P   |                        | 296M            |         |                 |                    |                  |          |      |  |     |   |
| 25/P   |                        | 296M            |         |                 |                    |                  |          |      |  |     |   |
| 24/P   |                        | 296M            |         |                 |                    |                  |          |      |  |     |   |
|        |                        |                 |         |                 |                    |                  |          |      |  |     |   |
| 625    | 50/P                   | 720x576         | 4:2:2   | BT.1358         | 349M               | 292              | 6        |      |  |     |   |
|        |                        |                 |         | BT.1358         | 347M               | 344M             |          |      |  |     |   |
|        |                        |                 |         | BT.1358         | BT.1358            | BT.1362          |          |      |  |     |   |
|        |                        |                 | 4:2:0   | BT.1358         | 349M               | 292              |          |      |  |     |   |
|        |                        |                 |         | BT.1358         | BT.1358            | BT.1362          |          |      |  |     |   |
|        |                        |                 |         |                 |                    |                  |          |      |  |     |   |
|        | 50/I                   | 960x576         | 4:2:2   | BT.601          | 349M               | 292              | 6/319    |      |  |     |   |
|        |                        |                 |         | BT.601          | BT.656             | 259M             |          |      |  |     |   |
|        |                        | 720x576         | 4:4:4:4 | BT.799          | 349M               | 292              |          |      |  |     |   |
|        |                        |                 |         | BT.799          | 347M               | 344M             |          |      |  |     |   |
|        |                        |                 |         | BT.799          | BT.799             | 344M             |          |      |  |     |   |
|        |                        |                 |         | BT.799          | BT.799             | —                |          |      |  |     |   |
|        |                        |                 |         | 4:2:2           | BT.601             | 349M             |          | 292  |  |     |   |
|        |                        |                 | BT.601  |                 | 125M               | 259M             |          |      |  |     |   |

**Table 4-7: Switch Line Position for Digital Systems (Continued)**

| System  | Frame Rate & Structure | Pixel Structure |       | Signal Standard | Parallel Interface | Serial Interface | Line No. |
|---------|------------------------|-----------------|-------|-----------------|--------------------|------------------|----------|
| 525     | 59.94/P                | 720x483         | 4:2:2 | 293M            | 349M               | 292              | 10       |
|         |                        |                 |       | 293M            | 347M               | 344M             |          |
|         |                        |                 |       | 293M            | 293M               | 294M             |          |
|         |                        | 4:2:0           | 293M  | 349M            | 292                |                  |          |
|         |                        |                 | 293M  | 293M            | 294M               |                  |          |
|         | 59.94/I                | 960x483         | 4:2:2 | 267M            | 349M               | 292              | 10/273   |
|         |                        |                 |       | 267M            | 267M               | 259M             |          |
|         |                        | 720x483         | 4:4:4 | 267M            | 349M               | 292              |          |
|         |                        |                 |       | 267M            | 347M               | 344M             |          |
|         |                        |                 |       | 267M            | RP174              | 344M             |          |
|         |                        |                 |       | 267M            | RP175              | RP175            |          |
|         |                        |                 | 4:2:2 | 125M            | 349M               | 292              |          |
|         |                        |                 |       | 125M            | 125M               | 259M             |          |
| HD-SDTI | P or PsF structure     | 1920x1080       | 4:2:2 | 274M            | 274M + 348M        | 292              | 7        |
|         | I structure            |                 |       | 274M            |                    |                  | 7/569    |
|         | P structure            | 1280x720        |       | 296M            | 296M + 348M        |                  | 7        |
| SDTI    | 50/I                   | 720x576         | 4:2:2 | BT.656          | BT.656 + 305M      | 259M             | 6/319    |
|         | 59.94/I                | 720x483         |       | 125M            | 125M + 305M        |                  | 10/273   |

## 4.11 Programmable Multi-function Outputs

The GS2960A has 6 multi-function output pins, STAT [5:0], which are programmable via the host interface to output one of the following signals:

**Table 4-8: Output Signals Available on Programmable Multi-Function Pins**

| Status Signal                                                   | Selection Code | Default Output Pin |
|-----------------------------------------------------------------|----------------|--------------------|
| H/HSYNC (according to TIM_861 Pin) <a href="#">Section 4.12</a> | 0000           | STAT 0             |
| V/VSYSN (according to TIM_861 Pin) <a href="#">Section 4.12</a> | 0001           | STAT 1             |
| F/DE (according to TIM_861 Pin) <a href="#">Section 4.12</a>    | 0010           | STAT 2             |
| LOCKED <a href="#">Section 4.7</a>                              | 0011           | STAT 3             |
| Y/1ANC <a href="#">Section 4.17</a>                             | 0100           | STAT 4             |
| C/2ANC <a href="#">Section 4.17</a>                             | 0101           | –                  |
| DATA ERROR <a href="#">Section 4.16</a>                         | 0110           | STAT 5             |

**Table 4-8: Output Signals Available on Programmable Multi-Function Pins (Continued)**

| Status Signal  | Selection Code | Default Output Pin |
|----------------|----------------|--------------------|
| VIDEO ERROR    | 0111           | —                  |
| EDH DETECTED   | 1001           | —                  |
| CARRIER DETECT | 1010           | —                  |
| RATE_DET0      | 1011           | —                  |
| RATE_DET1      | 1100           | —                  |

NOTE:

Each of the STAT[5:0] pins are configurable individually using the register bits in the host interface; STAT[5:0]\_CONFIG (008h/009h).

## 4.12 H:V:F Timing Signal Generation

The GS2960A extracts critical timing parameters from the received TRS words.

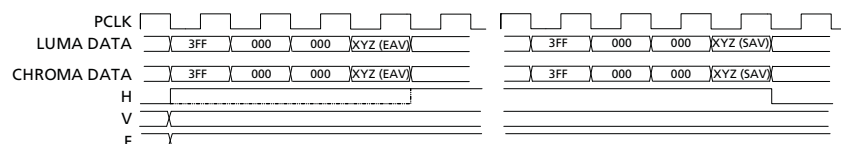
Horizontal blanking (H), Vertical blanking (V), and Field odd/even (F) timing are output on the STAT[2:0] pins by default.

Using the H\_CONFIG bit in the host interface, the H signal timing can be selected as one of the following:

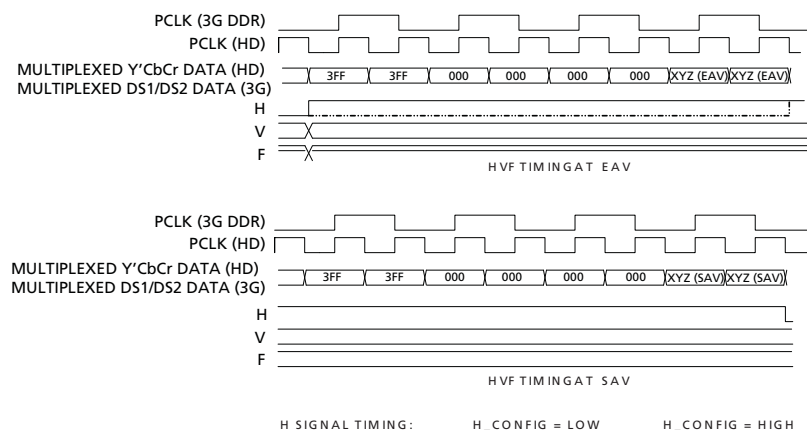
1. Active line blanking (H\_CONFIG = LOW) - the H output is HIGH for the horizontal blanking period, including the EAV TRS words.
2. TRS based blanking (H\_CONFIG = HIGH) - the H output is set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS signals.

The timing of these signals is shown in the figures below.

**NOTE:** Both 8-bit and 10-bit TRS words are identified by the device.



**Figure 4-11: H:V:F Output Timing - 3G Level A and HDTV 20-bit Mode**



**Figure 4-12: H:V:F Output Timing - 3G Level A and HDTV 10-bit Mode  
3G Level B 20-bit Mode, each 10-bit stream**



## 4.12.1 CEA-861 Timing Generation

The GS2960A is capable of generating CEA 861 timing instead of SMPTE HVF timing for all of the supported video formats.

This mode is selected when the TIM\_861 pin is HIGH.

Horizontal sync (HSYNC), Vertical sync (VSYNC), and Data Enable (DE) timing are output on the STAT[2:0] pins by default.

Table 4-9 shows the CEA-861 formats supported by the GS2960A:

**Table 4-9: Supported CEA-861 Formats**

| Format                        | CEA-861 Format  | VD_STD[5:0]        |
|-------------------------------|-----------------|--------------------|
| 720(1440) x 480i @ 59.94/60Hz | 6 & 7           | 16h, 17h, 19h, 1Bh |
| 720(1440) x 576i @ 50Hz       | 21 & 22         | 18h, 1Ah           |
| 1280 x 720p @ 59.94/60Hz      | 4               | 20h, 00h           |
| 1280 x 720p @ 50Hz            | 19              | 24h, 04h           |
| 1920 x 1080i @ 59.94/60Hz     | 5               | 2Ah, 0Ah           |
| 1920 x 1080i @ 50Hz           | 20              | 2Ch, 0Ch           |
| 1920 x 1080p @ 29.97/30Hz     | 34 <sup>1</sup> | 2Bh, 0Bh           |
| 1920 x 1080p @ 25Hz           | 33 <sup>2</sup> | 2Dh, 0Dh           |
| 1920 x 1080p @ 23.98/24Hz     | 32              | 30h, 10h           |
| 1920 x 1080p @ 59.94/60Hz     | 16 <sup>1</sup> | 2Bh                |
| 1920 x 1080p @ 50Hz           | 31 <sup>2</sup> | 2Dh                |

NOTES:

1,2: Timing is identical for the corresponding formats.

### 4.12.1.1 Vertical Timing

When CEA861 timing is selected, the device will output standards compliant CEA861 timing signals as shown in the figures below; for example 240 active lines per field for SMPTE 125M.

The register bit TRS\_861 is used to select DFP timing generator mode which follows the vertical blanking timing as defined by the embedded TRS code words.

The timing of the CEA 861 timing reference signals can be found in the CEA 861 specifications. For information, they are included in the following diagrams. These diagrams may not be comprehensive.

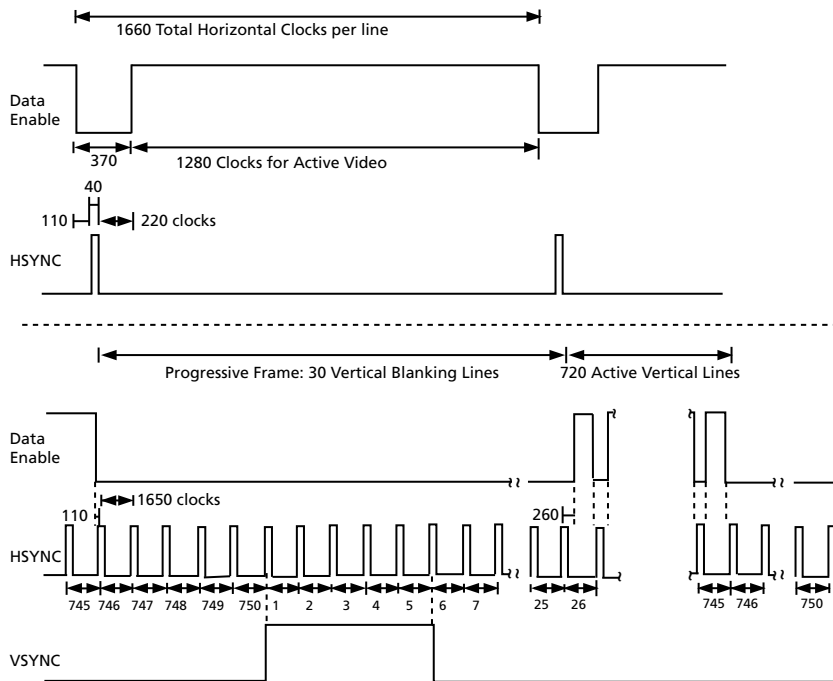


Figure 4-18: H:V:DE Output Timing 1280 x 720p @ 59.94/60 (Format 4)

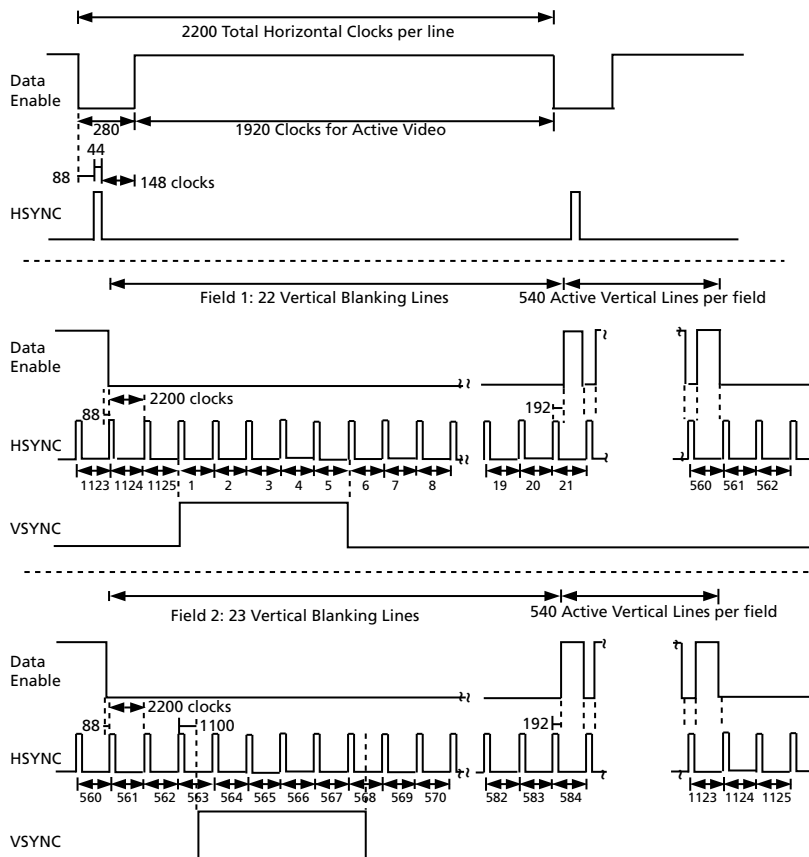


Figure 4-19: H:V:DE Output Timing 1920 x 1080i @ 59.94/60 (Format 5)

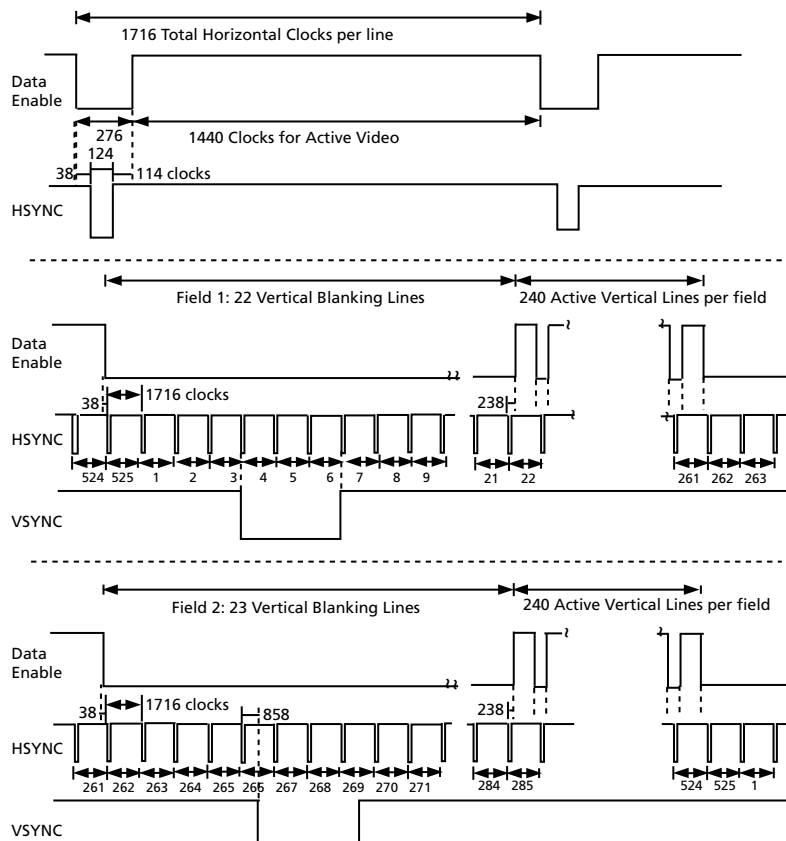


Figure 4-20: H:V:DE Output Timing 720 (1440) x 480i @ 59.94/60 (Format 6&7)

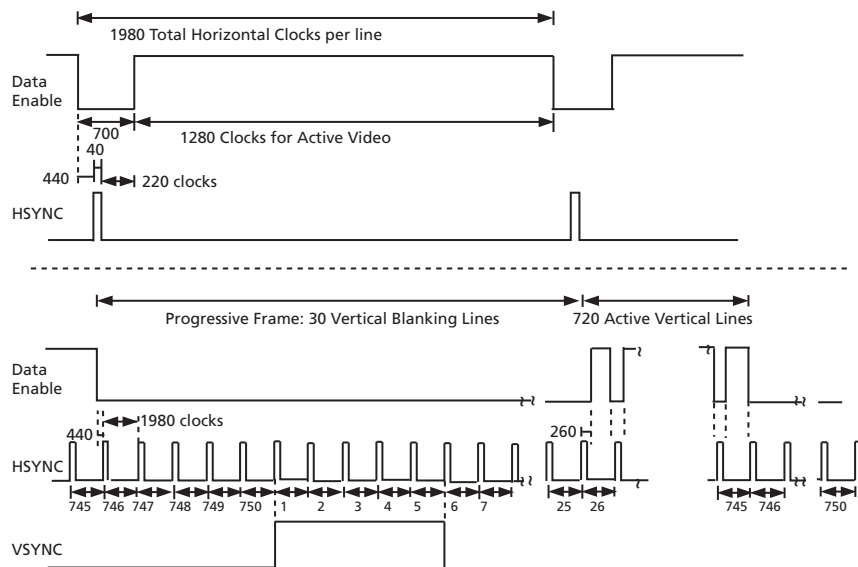


Figure 4-21: H:V:DE Output Timing 1280 x 720p @ 50 (Format 19)

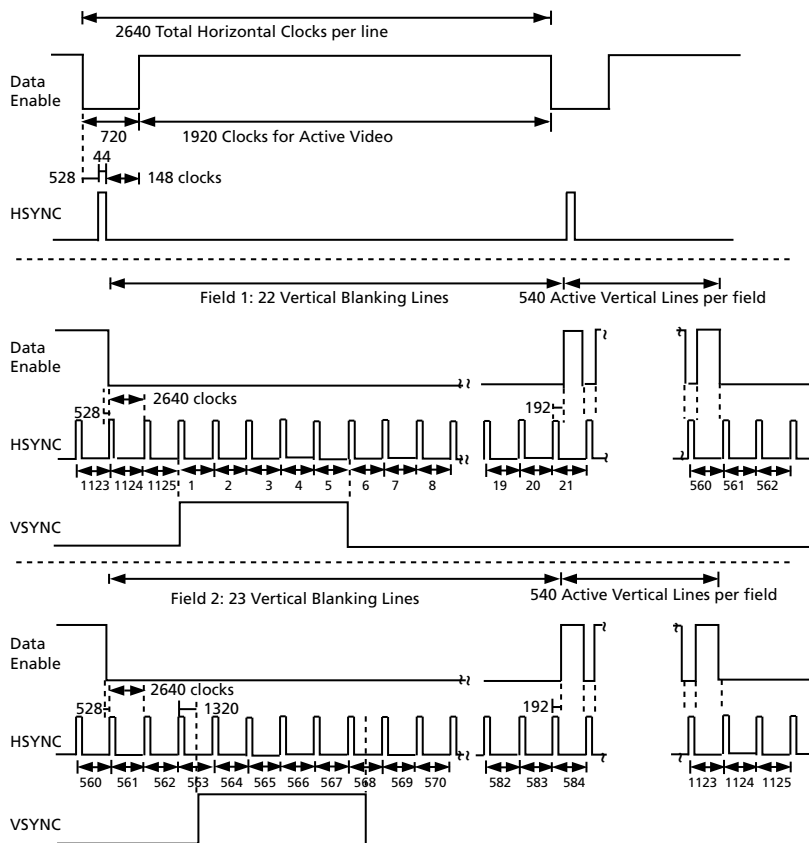


Figure 4-22: H:V:DE Output Timing 1920 x 1080i @ 50 (Format 20)

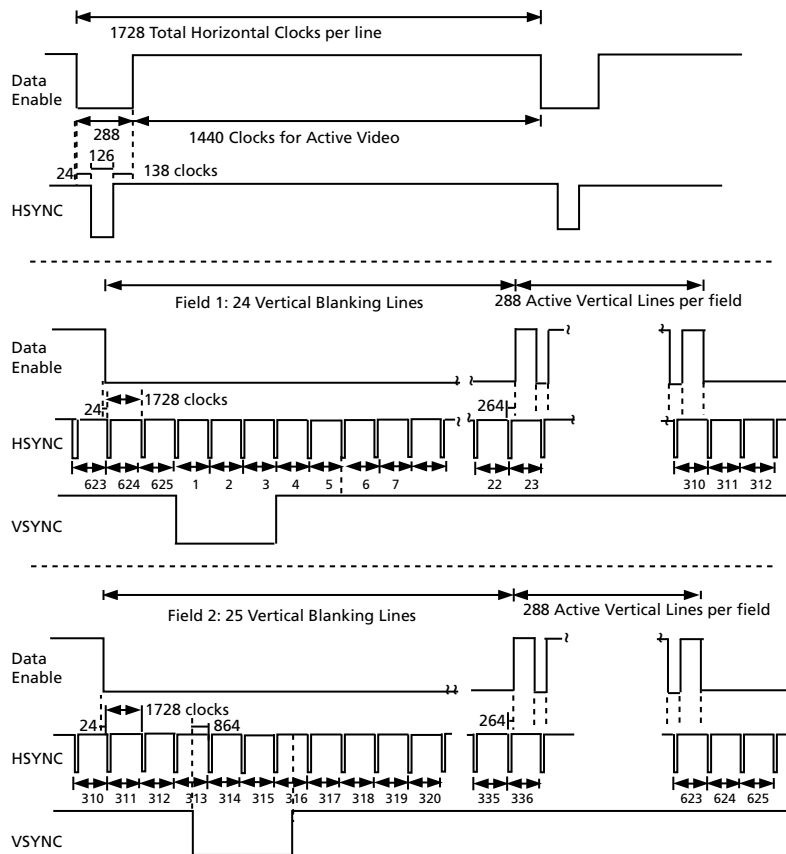


Figure 4-23: H:V:DE Output Timing 720 (1440) x 576 @ 50 (Format 21 & 22)

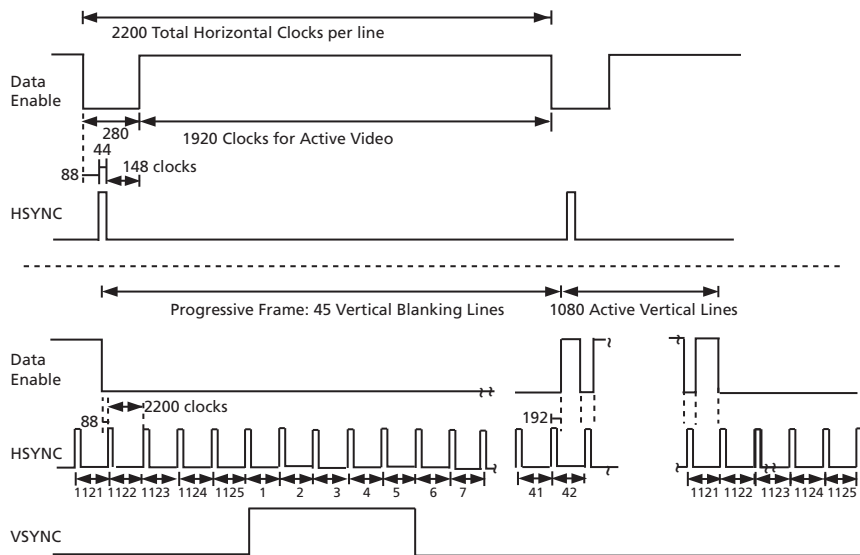


Figure 4-24: H:V:DE Output Timing 1920 x 1080p @ 59.94/60 (Format 16)

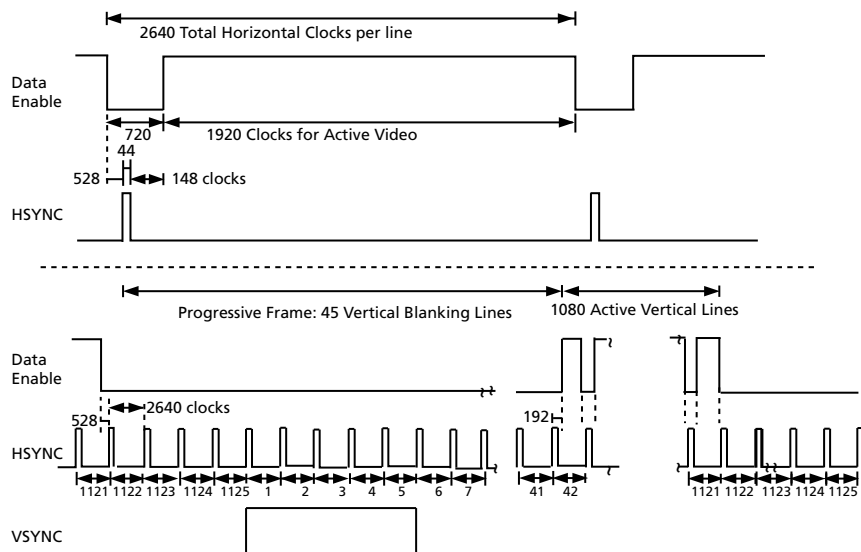


Figure 4-25: H:V:DE Output Timing 1920 x 1080p @ 50 (Format 31)

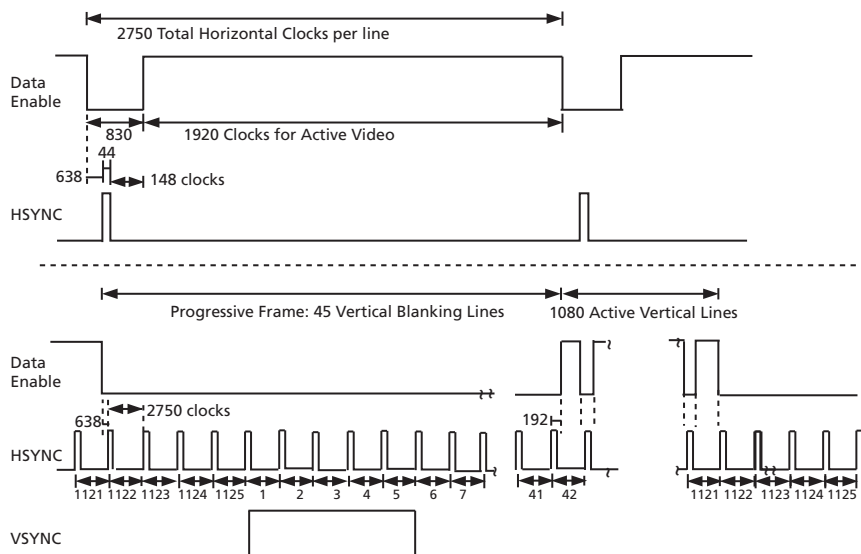


Figure 4-26: H:V:DE Output Timing 1920 x 1080p @ 23.94/24 (Format 32)

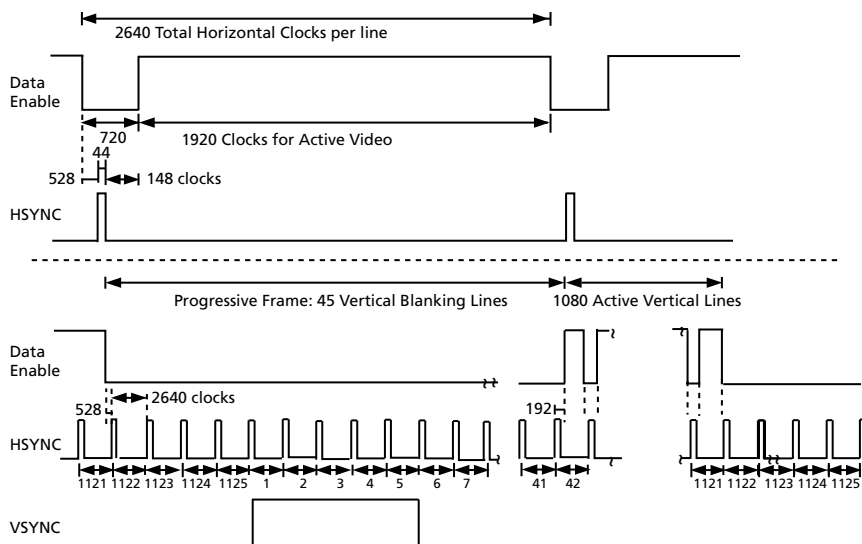


Figure 4-27: H:V:DE Output Timing 1920 x 1080p @ 25 (Format 33)

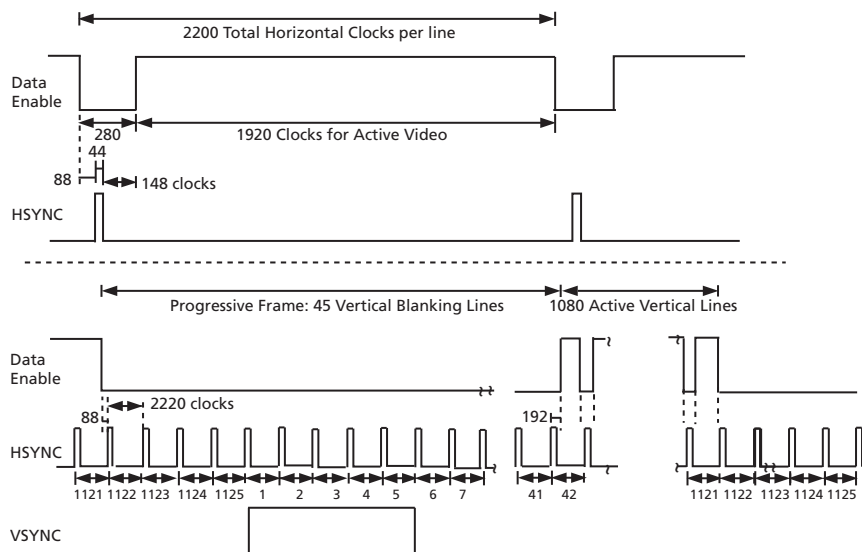


Figure 4-28: H:V:DE Output Timing 1920 x 1080p @ 29.97/30 (Format 34)

## 4.13 Automatic Video Standards Detection

Using the timing extracted from the received TRS signals, the GS2960A is able to identify the received video standard.

In 3G input mode, the GS2960A measures the timing parameters of one of the two identical data streams. The Rate Selection/Indication bits and the VD\_STD code may be used in combination to determine the video standard.

The total samples per line, active samples per line, total lines per field/frame and active lines per field/frame are all measured.

Four registers are provided to allow the system to read the video standard information from the device. These raster structure registers are provided in addition to the

VIDEO\_FORMAT\_352\_A\_X and VIDEO\_FORMAT\_352\_B\_X registers, and are updated once per frame at the end of line 12.

The raster structure registers also contain three status bits: STD\_LOCK, INT/ $\overline{\text{PROG}}$  and M. The STD\_LOCK bit is set HIGH whenever the timing signal generator is fully synchronized to the incoming standard, and detects it as one of the supported formats. The INT/ $\overline{\text{PROG}}$  bit is set HIGH if the detected video standard is interlaced and LOW if the detected video standard is progressive. M is set HIGH if the clock frequency includes the “1000/1001” factor denoting a 23.98, 29.97 or 59.94Hz frame rate.

The video standard code is reported in the VD\_STD bits of the host interface register.

Table 4-10 describes the 5-bit codes for the recognized video standards.

**Table 4-10: Supported Video Standard Codes**

| SMPTE<br>Standard                            | Active Video Area                           | RATE_<br>DET[1]<br>HD/3G | RATE_<br>DET[0]<br>SD/HD | Lines<br>per<br>Frame | Active<br>Lines per<br>Frame | Words<br>per<br>Active<br>Line | Words<br>per Line | VD_STD<br>[5:0] |
|----------------------------------------------|---------------------------------------------|--------------------------|--------------------------|-----------------------|------------------------------|--------------------------------|-------------------|-----------------|
| 425M (3G<br>Level A)<br>4:2:2                | 1920x1080/60 (1:1)                          | 1                        | 0                        | 1125                  | 1080                         | 1920                           | 2200              | 2Bh             |
|                                              | 1920x1080/50 (1:1)                          | 1                        | 0                        | 1125                  | 1080                         | 1920                           | 2640              | 2Dh             |
| 425M (3G<br>Level B<br>DS1 and<br>DS2) 4:2:2 | 1920x1080/60 (2:1)                          | 1                        | 0                        | 1125                  | 540                          | 1920                           | 2200              | 0Ah             |
|                                              | 1920x1080/50 (2:1)                          | 1                        | 0                        | 1125                  | 540                          | 1920                           | 2640              | 0Ch             |
| 425M (3G)<br>4:4:4                           | 1920x1080/60 (2:1) or<br>1920x1080/30 (PsF) | 1                        | 0                        | 1125                  | 1080                         | 3840                           | 4400              | 2Ah             |
|                                              | 1920x1080/50 (2:1) or<br>1920x1080/25 (PsF) | 1                        | 0                        | 1125                  | 1080                         | 3840                           | 5280              | 2Ch             |
|                                              | 1280x720/60 (1:1)                           | 1                        | 0                        | 750                   | 720                          | 2560                           | 3300              | 20h             |
|                                              | 1280x720/50 (1:1)                           | 1                        | 0                        | 750                   | 720                          | 2560                           | 3960              | 24h             |
|                                              | 1920x1080/30 (1:1)                          | 1                        | 0                        | 1125                  | 1080                         | 3840                           | 4400              | 2Bh             |
|                                              | 1920x1080/25 (1:1)                          | 1                        | 0                        | 1125                  | 1080                         | 3840                           | 5280              | 2Dh             |
|                                              | 1280x720/25 (1:1)                           | 1                        | 0                        | 750                   | 720                          | 2560                           | 7920              | 26h             |
|                                              | 1920x1080/24 (1:1)                          | 1                        | 0                        | 1125                  | 1080                         | 3840                           | 5500              | 30h             |
|                                              | 1280x720/24 (1:1)                           | 1                        | 0                        | 750                   | 720                          | 2560                           | 8250              | 28h             |
| 260M (HD)                                    | 1920x1035/60 (2:1)                          | 0                        | 0                        | 1125                  | 1035                         | 1920                           | 2200              | 15h             |
| 259M (HD)                                    | 1920x1080/50 (2:1)                          | 0                        | 0                        | 1250                  | 1080                         | 1920                           | 2376              | 14h             |

**Table 4-10: Supported Video Standard Codes (Continued)**

| SMPTE Standard          | Active Video Area                              | RATE_<br>DET[1]<br>HD/3G | RATE_<br>DET[0]<br>SD/HD | Lines<br>per<br>Frame | Active<br>Lines per<br>Frame | Words<br>per<br>Active<br>Line | Words<br>per Line | VD_STD<br>[5:0] |
|-------------------------|------------------------------------------------|--------------------------|--------------------------|-----------------------|------------------------------|--------------------------------|-------------------|-----------------|
| 274M (HD)               | 1920x1080/60 (2:1) or<br>1920x1080/30 (PsF)    | 0                        | 0                        | 1125                  | 1080                         | 1920                           | 2200              | 0Ah             |
|                         | 1920x1080/50 (2:1) or<br>1920x1080/25 (PsF)    | 0                        | 0                        | 1125                  | 1080                         | 1920                           | 2640              | 0Ch             |
|                         | 1920x1080/30 (1:1)                             | 0                        | 0                        | 1125                  | 1080                         | 1920                           | 2200              | 0Bh             |
|                         | 1920x1080/25 (1:1)                             | 0                        | 0                        | 1125                  | 1080                         | 1920                           | 2640              | 0Dh             |
|                         | 1920x1080/24 (1:1)                             | 0                        | 0                        | 1125                  | 1080                         | 1920                           | 2750              | 10h             |
|                         | 1920x1080/24 (PsF)                             | 0                        | 0                        | 1125                  | 1080                         | 1920                           | 2750              | 11h             |
|                         | 1920x1080/25 (1:1) –<br>EM                     | 0                        | 0                        | 1125                  | 1080                         | 2304                           | 2640              | 0Eh             |
|                         | 1920x1080/25 (PsF) –<br>EM                     | 0                        | 0                        | 1125                  | 1080                         | 2304                           | 2640              | 0Fh             |
|                         | 1920x1080/24 (1:1) –<br>EM                     | 0                        | 0                        | 1125                  | 1080                         | 2400                           | 2750              | 12h             |
|                         | 1920x1080/24 (PsF) –<br>EM                     | 0                        | 0                        | 1125                  | 1080                         | 2400                           | 2750              | 13h             |
| 296M (HD)               | 1280x720/30 (1:1)                              | 0                        | 0                        | 750                   | 720                          | 1280                           | 3300              | 02h             |
|                         | 1280x720/30 (1:1) –<br>EM                      | 0                        | 0                        | 750                   | 720                          | 2880                           | 3300              | 03h             |
|                         | 1280x720/50 (1:1)                              | 0                        | 0                        | 750                   | 720                          | 1280                           | 1980              | 04h             |
| 296M (HD)               | 1280x720/50 (1:1) –<br>EM                      | 0                        | 0                        | 750                   | 720                          | 1728                           | 1980              | 05h             |
|                         | 1280x720/25 (1:1)                              | 0                        | 0                        | 750                   | 720                          | 1280                           | 3960              | 06h             |
|                         | 1280x720/25 (1:1) –<br>EM                      | 0                        | 0                        | 750                   | 720                          | 3456                           | 3960              | 07h             |
|                         | 1280x720/24 (1:1)                              | 0                        | 0                        | 750                   | 720                          | 1280                           | 4125              | 08h             |
|                         | 1280x720/24 (1:1) –<br>EM                      | 0                        | 0                        | 750                   | 720                          | 3600                           | 4125              | 09h             |
|                         | 1280x720/60 (1:1)                              | 0                        | 0                        | 750                   | 720                          | 1280                           | 1650              | 00h             |
|                         | 1280x720/60 (1:1) –<br>EM                      | 0                        | 0                        | 750                   | 720                          | 1440                           | 1650              | 01h             |
| 125M (SD)               | 1440x487/60 (2:1)                              | x                        | 1                        | 525                   | 244 or 243                   | 1440                           | 1716              | 16h             |
|                         | 1440x507/60                                    | x                        | 1                        | 525                   | 254 or 253                   | 1440                           | 1716              | 17h             |
|                         | 525-line 487 generic                           | x                        | 1                        | 525                   | –                            | –                              | 1716              | 19h             |
|                         | 525-line 507 generic                           | x                        | 1                        | 525                   | –                            | –                              | 1716              | 18h             |
| ITU-R<br>BT.656<br>(SD) | 1440x576/50 (2:1) Or<br>dual link progressive) | x                        | 1                        | 625                   | –                            | 1440                           | 1728              | 18h             |
|                         | 625-line generic                               | x                        | 1                        | 625                   | –                            | –                              | 1728              | 1Ah             |

**Table 4-10: Supported Video Standard Codes (Continued)**

| SMPTE Standard                                           | Active Video Area      | RATE_DET[1]<br>HD/3G | RATE_DET[0]<br>SD/HD | Lines per Frame | Active Lines per Frame | Words per Active Line | Words per Line | VD_STD [5:0] |
|----------------------------------------------------------|------------------------|----------------------|----------------------|-----------------|------------------------|-----------------------|----------------|--------------|
| Unknown HD                                               | $SD/\overline{HD} = 0$ | 0                    | 0                    | –               | –                      | –                     | –              | 1Dh          |
| Unknown SD                                               | $SD/\overline{HD} = 1$ | x                    | 1                    | –               | –                      | –                     | –              | 1Eh          |
| Unknown 3G                                               | $SD/\overline{HD} = 0$ | 1                    | 0                    | –               | –                      | –                     | –              | 3Ch          |
| <b>2K Standards (see 4.13.1 2K Support)</b>              |                        |                      |                      |                 |                        |                       |                |              |
| 2048-2-200xX<br>(4:2:2)                                  | 2048x1080/30 (1:1)     | 0                    | 0                    | 1125            | 1080                   | 2048                  | 2200           | 31h          |
|                                                          | 2048x1080/25 (1:1)     | 0                    | 0                    | 1125            | 1080                   | 2048                  | 2640           | 32h          |
|                                                          | 2048x1080/24 (1:1)     | 0                    | 0                    | 1125            | 1080                   | 2048                  | 2750           | 33h          |
|                                                          | 2048x1080/60 (1:1)     | 1                    | 0                    | 1125            | 1080                   | 2048                  | 2200           | 37h          |
|                                                          | 2048x1080/50 (1:1)     | 1                    | 0                    | 1125            | 1080                   | 2048                  | 2640           | 38h          |
|                                                          | 2048x1080/48 (1:1)     | 1                    | 0                    | 1125            | 1080                   | 2048                  | 2750           | 39h          |
| 2048-2-200X<br>(4:4:4)                                   | 2048x1080/30 (1:1)     | 1                    | 0                    | 1125            | 1080                   | 2048                  | 2200           | 34h          |
|                                                          | 2048x1080/25 (1:1)     | 1                    | 0                    | 1125            | 1080                   | 2048                  | 2640           | 35h          |
|                                                          | 2048x1080/24 (1:1)     | 1                    | 0                    | 1125            | 1080                   | 2048                  | 2750           | 36h          |
| Non SMPTE or 2048-2-200xX<br>(4:2:2) Level B DS1 and DS2 | 2048x1080/60 (2:1)     | 0 (1)                | 0                    | 1125            | 540                    | 2048                  | 2200           | 3Dh          |
|                                                          | 2048x1080/50 (2:1)     | 0 (1)                | 0                    | 1125            | 540                    | 2048                  | 2640           | 3Eh          |
|                                                          | 2048x1080/48 (2:1)     | 0 (1)                | 0                    | 1125            | 540                    | 2048                  | 2750           | 3Fh          |
| Non SMPTE                                                | Unknown 2K             | x                    | 0                    | –               | –                      | 2048                  | –              | 3Ah          |

**NOTES:**

1. The Line Numbers in brackets refer to version zero SMPTE 352M packet locations, if they are different from version 1.
2. The part may provide full or limited functionality with standards that are not included in this table. Please consult a Semtech technical representative.
3. For SD-SDI streams, the device can report an incorrect M value when SMPTE-352M packets are present.

**NOTE:** In certain systems, due to greater ppm offsets in the crystal, the 'M' bit may not assert properly. In such cases, bits 3:0 in Register 06Fh can be increased to a maximum value of 4.

By default (after power up or after systems reset), the four RASTER\_STRUCTURE, VD\_STD, STD\_LOCK and INT/PROG registers are set to zero. These registers are also cleared when the  $\overline{\text{SMPTE\_BYPASS}}$  pin is LOW.

### 4.13.1 2K Support

In order to fully support 2K standards without customer intervention, Gennum provides FPGA code for enhancing the GS2960A's 2K capability.

The features of the 2K FPGA enhancement are:

- Automatic video standard detection for 2K standards
- 1/1.001 rate detection for 2K standards
- CEA-861 timing generation for 2K standards
- Automatic enabling of audio extraction

This enhancement is an interface between the GS2960A and the customer system. The behaviour of the GS2960A with or without the additional 2K enhancement FPGA code is identical from a user-perspective.

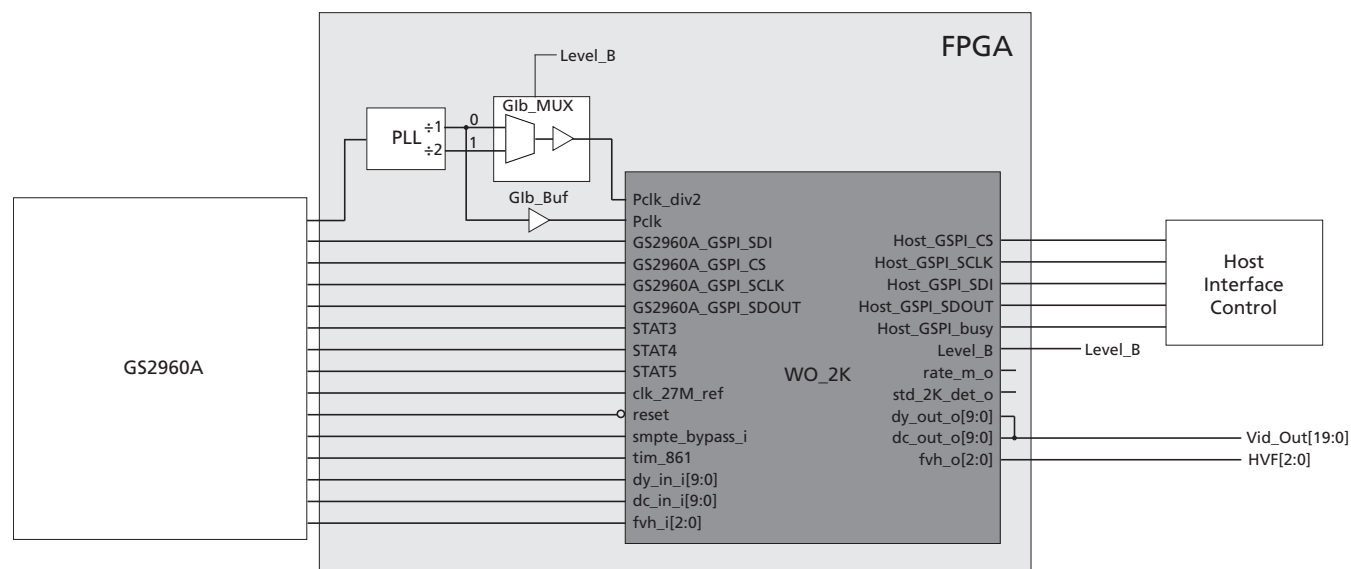


Figure 4-29: 2K Feature Enhancement

For more information, refer to the “Designing 2K with Gennum Receivers” Application Note (document #55590).

### 4.14 Data Format Detection & Indication

In addition to detecting the video standard, the GS2960A detects the data format, i.e. SDTI, SDI, TDM data (SMPTE 346M), etc.

This information is represented by bits in the DATA\_FORMAT\_DSX register accessible through the host interface.

Data format detection is only be carried out when the LOCKED signal is HIGH.

By default (at power up or after system reset), the DATA\_FORMAT\_DSX register is set to Fh (undefined). This register is also set as undefined when the LOCKED signal is LOW and/or the SMPTE\_BYPASS pin is LOW.

**Table 4-11: Data Format Register Codes**

| YDATA_FORMAT[3:0] or<br>CDATA_FORMAT[3:0] | Data Format              | Remarks                                                                                                                    |
|-------------------------------------------|--------------------------|----------------------------------------------------------------------------------------------------------------------------|
| 0h ~ 05h                                  | SDTI                     | SMPTE 321M, SMPTE 322M,<br>SMPTE 326M                                                                                      |
| 6h                                        | SDI                      | –                                                                                                                          |
| 7h                                        | Reserved                 | –                                                                                                                          |
| 8h                                        | TDM                      | SMPTE 346M                                                                                                                 |
| 9h                                        | HD-SDTI                  | –                                                                                                                          |
| Ah ~ Eh                                   | Reserved                 | –                                                                                                                          |
| Fh                                        | Non-SMPTE data<br>format | Detected data format is not SMPTE.<br>LOCKED = LOW.<br>NOTE: This Data Format register is<br>invalid in SMPTE_BYPASS mode. |

The data format is determined using the following criteria:

- If TRS ID words are detected but no SDTI header or TDM header is detected, then the data format is SDI
- If TRS ID words are detected and the SDTI header is available then the format is SDTI
- If TRS ID words are detected and the TDM data header is detected then the format is TDM video
- No TRS words are detected, but the PLL is locked, then the data format is unknown

**NOTE:** Two data format sets are provided for HD video rates. This is because the Y and Cr/Cb channels can be used separately to carry SDTI data streams of different data formats. In SD video mode, only the Y data format register contains the data, and the C register is set to Fh (undefined format).

## 4.15 EDH Detection

### 4.15.1 EDH Packet Detection

The GS2960A determines if EDH packets are present in the incoming video data and asserts the EDH\_DETECT status according to the SMPTE standard.

EDH\_DETECT is set HIGH when EDH packets have been detected and remains HIGH until EDH packets are no longer present. It is set LOW at the end of the vertical blanking (falling edge of V) if an EDH packet has not been detected during vertical blanking.

EDH\_DETECT can be programmed to be output on the multi-function output port pins. The EDH\_DETECT bit is also available in the host interface.

## 4.15.2 EDH Flag Detection

The EDH flags for ancillary data, active picture, and full field regions are extracted from the detected EDH packets and placed in the EDH\_FLAG\_IN register.

When the EDH\_FLAG\_UPDATE\_MASK bit in the host interface is set HIGH, the GS2960A updates the Ancillary Data, Full Field, and Active Picture EDH flags according to SMPTE RP165. The updated EDH flags are available in the EDH\_FLAG\_OUT register. The EDH packet output from the device contains these updated flags.

One set of flags is provided for both fields 1 and 2. The field 1 flag data is overwritten by the field 2 flag data.

When EDH packets are not detected, the UES flags in the EDH\_FLAG\_OUT register are set HIGH to signify that the received signal does not support Error Detection and Handling. In addition, the EDH\_DETECT bit is set LOW. These flags are set regardless of the setting of the EDH\_FLAG\_UPDATE\_MASK bit.

EDH\_FLAG\_OUT and EDH\_FLAG\_IN may be read via the host interface at any time during the received frame except on the lines defined in SMPTE RP165, when these flags are updated.

The GS2960A indicates the CRC validity for both active picture and full field CRCs. The AP\_CRC\_V bit in the host interface indicates the active picture CRC validity, and the FF\_CRC\_V bit indicates the full field CRC validity. When EDH\_DETECT = LOW, these bits are cleared.

The EDH\_FLAG\_OUT and EDH\_FLAG\_IN register values remain set until overwritten by the decoded flags in the next received EDH packet. When an EDH packet is not detected during vertical blanking, the flag registers are cleared at the end of the vertical blanking period.

## 4.16 Video Signal Error Detection & Indication

The GS2960A includes a number of video signal error detection functions. These are provided to enhance operation of the device when operating in SMPTE mode ( $\overline{\text{SMPTE\_BYPASS}} = \text{HIGH}$ ). These features are not available in the other operating modes of the device (i.e. when  $\overline{\text{SMPTE\_BYPASS}} = \text{LOW}$ ).

Signal errors that can be detected include:

1. TRS errors.
2. HD line based CRC errors.
3. EDH errors.
4. HD line number errors.
5. Video standard errors.

The device maintains an ERROR\_STAT\_X register. Each error condition has a specific flag in the ERROR\_STAT\_X register, which is set HIGH whenever an error condition is detected.

An ERROR\_MASK register is also provided, allowing the user to select which error conditions are reported. Each bit of the ERROR\_MASK register corresponds to a unique error type.

Each bit of each ERROR\_MASK register corresponds to a unique error type.

By default (at power up or after system reset), all bits of the ERROR\_MASK registers are zero, enabling all errors to be reported. Individual error detection may be disabled by setting the corresponding bit HIGH in the mask registers.

Error conditions are indicated by a  $\overline{\text{DATA\_ERROR}}$  signal, which is also available on the multifunction I/O pins. This signal is normally HIGH, but is set LOW by the device when an error condition has been detected.

This signal is a logical 'NOR' of the appropriate error status flags stored in the ERROR\_STAT\_X register, which are gated by the bit settings in the ERROR\_MASK registers. When an error status bit is HIGH and the corresponding error mask bit is LOW, the corresponding  $\overline{\text{DATA\_ERROR}}$  signal is set LOW by the device.

The ERROR\_STAT\_X registers, and correspondingly the  $\overline{\text{DATA\_ERROR}}$  signal, are cleared at the start of the next video field or when read via the host interface, whichever condition occurs first.

All bits of the ERROR\_STAT\_X registers are also cleared under any of the following conditions:

1. LOCKED signal = LOW.
2.  $\overline{\text{SMPTE\_BYPASS}}$  = LOW.
3. When a change in video standard has been detected.
4.  $\overline{\text{RESET\_TRST}}$  = LOW

Table 4-12 shows the ERROR\_STAT\_X register and ERROR\_MASK\_X register.

**NOTE:** Since the error indication registers are cleared once per field, if an external host micro is polling the error registers periodically, an error flag may be missed if it is intermittent, and the polling frequency is less than the field rate.

**Table 4-12: Error Status Register and Error Mask Register**

| Video Error Status Register | Video Error Mask Register  |
|-----------------------------|----------------------------|
| SAV_ERR (02h, 03h)          | SAV_ERR_MASK (037h, 038h)  |
| EAV_ERR (02h, 03h)          | EAV_ERR_MASK (037h, 038h)  |
| YCRC_ERR (02h, 03h)         | YCRC_ERR_MASK (037h, 038h) |
| CCRC_ERR (02h, 03h)         | CCRC_ERR_MASK (037h, 038h) |
| LNUM_ERR (02h, 03h)         | LNUM_ERR_MASK (037h, 038h) |
| YCS_ERR (02h, 03h)          | YCS_ERR_MASK (037h, 038h)  |
| CCS_ERR (02h, 03h)          | CCS_ERR_MASK (037h, 038h)  |
| AP_CRC_ERR (02h)            | AP_CRC_ERR_MASK (037h)     |
| FF_CRC_ERR (02h)            | FF_CRC_ERR_MASK (037h)     |
| VD_STD_ERR (02h, 03h)       | VD_STD_ERR_MASK (037h)     |

**NOTE:** In 3G Level B mode, separate Video Error Mask registers exist for Link A and Link B. The GS2960A distinguishes between Level A and Level B mappings at 3Gb/s. When Level B data is detected, error detection is enabled separately for Data Stream 1 and Data Stream 2 (Link A and Link B, respectively). Therefore, a second set of error status and mask registers is available for Data Stream 2, and is only valid when 3Gb/s Level B data is detected by the device.

#### 4.16.1 TRS Error Detection

TRS error flags are generated by the GS2960A under the following two conditions:

1. A phase shift in received TRS timing is observed on a non-switching line.
2. The received TRS Hamming codes are incorrect.

Both SAV and EAV TRS words are checked for timing and data integrity errors.

For HD mode, only the Y channel TRS codes are checked for errors.

For 3G mode Level A signals, only data stream one TRS codes are checked for errors. For 3G Level B signals, the Y channel TRS codes of both Link A and Link B are checked for errors.

Both 8-bit and 10-bit TRS code words are checked for errors.

The SAV\_ERR bit of the ERROR\_STAT\_X register is set HIGH when an SAV TRS error is detected.

The EAV\_ERR bit of the ERROR\_STAT\_X register is set HIGH when an EAV TRS error is detected.

#### 4.16.2 Line Based CRC Error Detection

The GS2960A calculates line based CRCs for HD and 3G video signals. CRC calculations are done for each 10-bit channel (Y and C for HD video, DS1 and DS2 for 3G video).

These calculated CRC values are compared with the received CRC values.

If a mismatch in the calculated and received CRC values is detected for Y channel data (Data Stream 1 for 3G video), the YCRC\_ERR bit in the ERROR\_STAT\_X register is set HIGH.

If a mismatch in the calculated and received CRC values is detected for C channel data (Data Stream 2 for 3G video), the CCRC\_ERR bit in the ERROR\_STAT\_X register is set HIGH.

Y or C CRC errors are also generated if CRC values are not embedded.

Line based CRC errors are only generated when the device is operating in HD and 3G modes.

**NOTE:** By default, 8-bit to 10-bit TRS remapping is enabled. If an 8-bit input is used, the HD CRC check is based on the 10-bit remapped value, not the 8-bit value, so the CRC Error Flag is incorrectly asserted and should be ignored. If 8-bit to 10-bit remapping is enabled, then CRC correction and insertion should be enabled by setting the CRC\_INS\_MASK bit in the IOPROC\_DISABLE register LOW. This ensures that the CRC values are updated.

### 4.16.3 EDH CRC Error Detection

The GS2960A also calculates Full Field (FF) and Active Picture (AP) CRC's according to SMPTE RP165 in support of Error Detection and Handling packets in SD signals.

These calculated CRC values are compared with the received CRC values.

Error flags for AP and FF CRC errors are provided and each error flag is a logical OR of the field 1 and field 2 error conditions.

The AP\_CRC\_ERR bit in the VIDEO\_ERROR\_STAT\_X register is set HIGH when an Active Picture CRC mismatch has been detected in field 1 or 2.

The FF\_CRC\_ERR bit in the VIDEO\_ERROR\_STAT\_X register is set HIGH when a Full Field CRC mismatch has been detected in field 1 or 2.

EDH CRC errors are only indicated when the device is operating in SD mode and when the device has correctly received EDH packets.

### 4.16.4 HD & 3G Line Number Error Detection

If a mismatch in the calculated and received line numbers is detected, the LNUM\_ERR bit in the VIDEO\_ERROR\_STAT\_X register is set HIGH.

## 4.17 Ancillary Data Detection & Indication

The GS2960A detects ancillary data in both the vertical and horizontal ancillary data spaces. Status signal outputs Y/1ANC and C/2ANC are provided to indicate the position of ancillary data in the output data streams. These signals may be selected on the multi-function I/O port pins (STAT[5:0]).

The GS2960A indicates the presence of all types of ancillary data by detecting the 000h, 3FFh, 3FFh (00h, FFh, FFh for 8-bit video) ancillary data preamble.

**NOTE:** Both 8 and 10-bit ancillary data preambles are detected by the device.

By default (at power up or after system reset) the GS2960A indicates all types of ancillary data. Up to 5 types of ancillary data can be specifically programmed for recognition.

For HD video signals, ancillary data may be placed in both the Y and Cb/Cr video data streams separately. For SD video signals, the ancillary data is multiplexed and combined into the YCbCr data space.

For 3G signals, ancillary data may be placed in either or both of the virtual interface data streams. Both data streams are examined for ancillary data.

For a 3G data stream formatted as per Level A mapping:

- The ancillary data is placed in Data Stream 1 first, with overflow into Data Stream 2
- SMPTE 352M packets are duplicated in both data streams

For a 3G data stream formatted as per Level B mapping:

- Each multiplexed data stream forming the 3G signal contains ancillary data embedded according to SMPTE 291M
- Each multiplexed data stream forming the 3G signal contains SMPTE 352M packets embedded according to SMPTE 425M

When operating in HD mode, the Y/1ANC signal is HIGH whenever ancillary data is detected in the Luma data stream, and C/2ANC is HIGH whenever ancillary data is detected in the Chroma data stream. The signals are asserted HIGH at the start of the ancillary data preamble, and remain HIGH until after the ancillary data checksum.

When detecting ancillary data in 3G Level A data, the Y/1ANC status output is HIGH whenever Data Stream 1 ancillary data is detected and the C/2ANC status output is HIGH whenever Data Stream 2 ancillary data is detected.

When detecting ancillary data in 3G Level B data, the Y/1ANC status output is HIGH whenever Data Stream 1 ancillary data is detected on either Y or C channels and the C/2ANC status output is HIGH whenever Data Stream 2 ancillary data is detected on either Y or C channels.

When operating in SD mode, the Y/1ANC and C/2ANC signals depend on the output data format. For 20-bit demultiplexed data, the Y/1ANC and C/2ANC signals operate independently to indicate the first and last ancillary Data Word position in the Luma and/or Chroma data streams. For 10-bit multiplexed data, the Y/1ANC signal is HIGH whenever ancillary data is detected, and the C/2ANC signal is always LOW.

When operating in 3G modes, the Y/1ANC and C/2ANC flags are both zero if the 10-bit multiplexed output format is selected.

These status signal outputs are synchronous with PCLK and may be used as clock-enables for external logic, or as write-enables for an external FIFO or other memory devices.

The operation of the Y/1ANC and C/2ANC signals is shown below in [Figure 4-30](#).

**NOTE 1:** When I/O processing is disabled, the Y/1ANC and C/2ANC flags may toggle, but they are invalid and should be ignored.

**NOTE 2:** In 3G Level B mode, if the ANC\_EXT\_SEL\_DS2\_DS1 bit is HIGH and the ANC\_DATA\_DELETE bit is HIGH, the Y/1ANC and C/2ANC flags are not valid.

**NOTE 3:** For 3G Level B data, the Y/1ANC flag identifies all ANC data on Data Stream 1 (Link A), whether it is embedded in the Y or C component – ANC data is not identified separately for each component. Similarly, the C/2ANC flag identifies all ANC data on Data Stream 2 (Link B), whether it is embedded in the Y or C component.

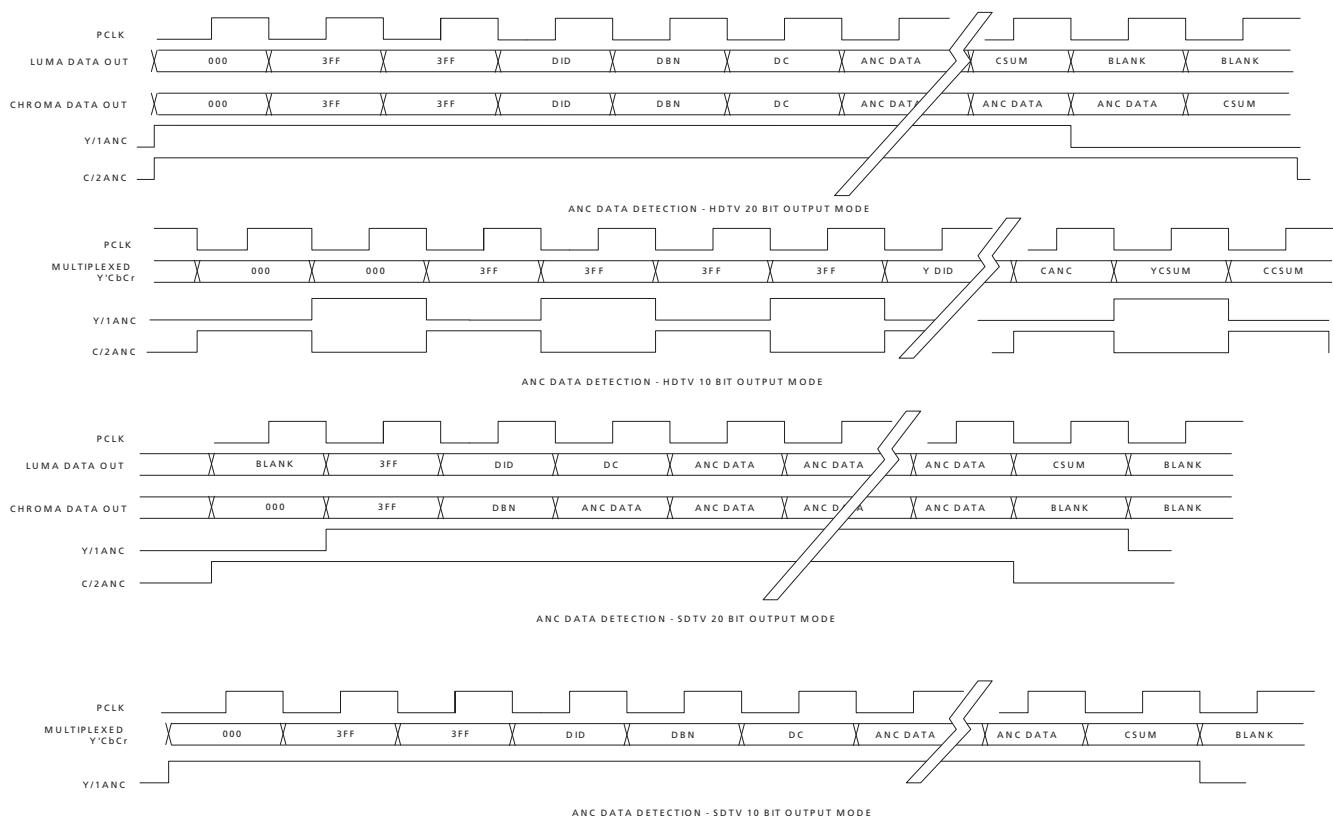


Figure 4-30: Y/1ANC and C/2ANC Signal Timing

#### 4.17.1 Programmable Ancillary Data Detection

As described above in [Section 4.17](#), the GS2960A detects and indicates all ancillary data types by default.

It is possible to program which ancillary data types are to be detected and indicated. Up to 5 different ancillary data types may be programmed for detection by the GS2960A in the ANC\_TYPE\_DS1 registers for SD, HD and 3G Level A data.

When so programmed, the GS2960A only indicates the presence of the specified ancillary data types, ignoring all other ancillary data. For each data type to be detected, the user must program the DID and/or SDID of that ancillary data type. In the case where no DID or SDID values are programmed, the GS2960A indicates the presence of all ancillary data. In the case where one or more, DID and/or SDID values have been programmed, then only those matching data types are detected and indicated.

The timing of the Y/1ANC and C/2ANC signals in this case is as shown in [Figure 4-30](#).

The GS2960A compares the received DID and/or SDID with the programmed values. If a match is found, ancillary data is indicated.

For any DID or SDID value set to zero, no comparison or match is made. For example, if the DID is programmed and the SDID is not programmed, the GS2960A only detects a match to the DID value.

If both DID and SDID values are non-zero, then the received ancillary data type must match both the DID and SDID before Y/1ANC and/or C/2ANC is set HIGH.

**NOTE 1:** For 3G Level B data, the ANC\_TYPE\_DS1 registers are valid for Data Stream 1, and a second set of five ANC\_TYPE registers (ANC\_TYPE\_DS2) is provided for detection of specific ancillary data in Data Stream 2.

**NOTE 2:** SMPTE 352M Payload Identifier packets and Error Detection and Handling (EDH) Packets are always detected by the GS2960A, irrespective of the settings of the ANC\_TYPE registers.

## 4.17.2 SMPTE 352M Payload Identifier

The GS2960A automatically extracts the SMPTE 352M payload identifier present in the input data stream for SD, HD, and 3G Level A signals. The four word payload identifier packets are written to VIDEO\_FORMAT\_352\_A\_X and VIDEO\_FORMAT\_352\_B\_X registers accessible through the host interface.

The device also indicates the version of the payload packet in the VERSION\_352M bit of the DATA\_FORMAT\_DSX register. When the SMPTE 352M packet is formatted as a 'version 1' packet, the VERSION\_352M bit is set HIGH, when the packet is formatted as a 'version 0' packet, this bit is set LOW.

The VIDEO\_FORMAT\_352\_A\_X and VIDEO\_FORMAT\_352\_B\_X registers are only updated if there are no checksum errors in the received SMPTE 352M packets.

By default (at power up or after system reset), the VVIDEO\_FORMAT\_X\_DS1 and VIDEO\_FORMAT\_X\_DS2 bits are set to 0, indicating an undefined format.

**NOTE 1:** When 3G Level B data is detected by the device, the user needs to extract the SMPTE 352M Payload Identifier packets by using the ANC packet extraction block - they are not detected and extracted automatically. In this case:

- The VD\_STD\_ERR bit is not valid
- 352M extraction is only done on one data stream or the other, not both simultaneously (Link A or Link B selected via the host interface)
- Previously embedded 352M packets can be deleted on one data stream only (using the ANC\_DATA\_DELETE bit, see [Section 4.18.8](#)), but these packets are replaced with 10-bit Y/C blanking values only
- It is necessary to manually extract the SMPTE 352M data by programming the DID, SDID and line number information into the ANC data extraction block

**NOTE 2:** SMPTE 352M packet regeneration is enabled by default for 3G Level B inputs, and should be disabled through the host interface if Level B to Level A conversion is not enabled.

### 4.17.2.1 SMPTE 352M Payload Identifier Usage

The SMPTE 352M Payload Identifier is used to confirm the video format identified by the Automatic Video Standards Detection block (see [Section 4.17.4](#))

**Table 4-13: SMPTE 352M Packet Data**

| Bit Name                            | Bit  | Name                 | Description                                                                                                         | R/W | Default |
|-------------------------------------|------|----------------------|---------------------------------------------------------------------------------------------------------------------|-----|---------|
| VIDEO_FORMAT_4_DS1<br>Address: 01Ah | 15-8 | SMPTE 352M<br>Byte 4 | Data is available in this register when Video Payload<br>Identification Packets are detected in the data<br>stream. | R   | 0       |
| VIDEO_FORMAT_3_DS1<br>Address: 01Ah | 7-0  | SMPTE 352M<br>Byte 3 |                                                                                                                     | R   | 0       |
| VIDEO_FORMAT_2_DS1<br>Address: 019h | 15-8 | SMPTE 352M<br>Byte 2 |                                                                                                                     | R   | 0       |
| VIDEO_FORMAT_2_DS1<br>Address: 019h | 7-0  | SMPTE 352M<br>Byte 1 |                                                                                                                     | R   | 0       |

#### 4.17.2.2 3G SMPTE 352M Packets Following Level B to Level A Conversion

After Level B to Level A conversion, modified payload data must be programmed via the host interface into the VIDEO\_FORMAT\_352\_X\_X registers and automatically inserted by the GS2960A on the correct SMPTE 352M Line Number.

SMPTE 352M Packets are embedded in both data streams.

Previously embedded 352M packets may be deleted from one data stream only (using the ANC\_DATA\_DELETE bit, see [Section 4.18.8](#)), but these packets are replaced with 10-bit Y/C blanking values.

**NOTE:** Pre-existing SMPTE 352M Packets that are not deleted are re-mapped to different line numbers during conversion to Level A formatting. These packets should be ignored by the system, since they are on non-standard SMPTE 352M lines.

### 4.17.3 Ancillary Data Checksum Error

The GS2960A calculates checksums for all received ancillary data.

These calculated checksums are compared with the received ancillary data checksum words.

If a mismatch in the calculated and received checksums is detected, then a checksum error is indicated.

When operating in HD mode, the device makes comparisons on both the Y and C channels separately. If an error condition in the Y channel is detected, the YCS\_ERR bit in the VIDEO\_ERROR\_STAT\_X register is set HIGH. If an error condition in the C channel is detected, the CCS\_ERR bit in the VIDEO\_ERROR\_STAT\_X register is set HIGH.

When operating in 3G Level A mode, the device makes comparisons on both the Y (Data Stream 1) and C (Data Stream 2) channels separately. If an error condition in the Y channel is detected, the YCS\_ERR bit in the VIDEO\_ERROR\_STAT\_X register is set HIGH. If an error condition in the C channel is detected, the CCS\_ERR bit in the VIDEO\_ERROR\_STAT\_X register is set HIGH.

When operating in 3G Level B mode, the device makes comparisons on both the Y channel and the C channel of both Link A and Link B.

When operating in SD mode, only the YCS\_ERR bit is set HIGH when checksum errors are detected.

#### 4.17.3.1 Programmable Ancillary Data Checksum Calculation

As described above, the GS2960A calculates and compares checksum values for all ancillary data types by default. It is possible to program which ancillary data types are checked as described in [Section 4.17.1](#).

When so programmed, the GS2960A only checks ancillary data checksums for the specified data types, ignoring all other ancillary data.

The YCS\_ERR and/or CCS\_ERR bits in the VIDEO\_ERROR\_STAT\_X register are only set HIGH if an error condition is detected for the programmed ancillary data types.

#### 4.17.4 Video Standard Error

If a mismatch between the received SMPTE 352M packets and the calculated video standard occurs, the GS2960A indicates a video standard error by setting the VD\_STD\_ERR bit of the VIDEO\_ERROR\_STAT\_X register HIGH.

The device detects the SMPTE 352M Packet version as defined in the SMPTE 352M standard. If the incoming packet is Version Zero, then no comparison is made with the internally generated payload information and the VD\_STD\_ERR bit is not set HIGH.

**NOTE 1:** If the received SMPTE 352M packet indicates 25, 30 or 29.97PsF formats, the device only indicates an error when the video format is actually progressive. The device detects 24 and 23.98PsF video standards and perform error checking at these rates.

**NOTE 2:** The VD\_STD\_ERR bit should be ignored in all 3G modes.

**NOTE 3:** VD\_STD\_ERR\_DS1 is set incorrectly for a 1920x1080/PsF/24 payload ID. To resolve this issue, choose one of the two methods.

- Set the VD\_STD\_ERR\_DS1 mask bit high in the ERROR\_MASK\_1 register to avoid having incorrect assertion of the  $\overline{\text{DATA\_ERROR}}$  pin.
- Monitor the received SMPTE ST0352 packet in the VIDEO\_FORMAT\_352\_A\_1 and VIDEO\_FORMAT\_352\_B\_1 registers and compare that to the video format identified in the VD\_STD\_DS1 bits in the DATA\_FORMAT\_DS1 register. Then, make the determination of whether or not there is a mismatch on their own.

### 4.18 Signal Processing

In addition to error detection and indication, the GS2960A can also correct errors, inserting corrected code words, checksums and CRC values into the data stream.

The following processing can be performed by the GS2960A:

1. TRS error correction and insertion.
2. HD line based CRC correction and insertion.
3. EDH CRC error correction and insertion.
4. HD line number error correction and insertion.
5. Illegal code re-mapping.

6. Ancillary data checksum error correction and insertion.
7. SMPTE 372M (Level B to Level A) Conversion.

All of the above features are only available in SMPTE mode ( $\overline{\text{SMPTE\_BYPASS}} = \text{HIGH}$ ).

To enable these features, the IOPROC\_EN/ $\overline{\text{DIS}}$  pin must be set HIGH, and the individual feature must be enabled via bits in the IOPROC\_DISABLE register.

The IOPROC\_DISABLE register contains one bit for each processing feature allowing each one to be enabled/disabled individually.

By default (at power up or after system reset), all of the IOPROC\_DISABLE register bits are LOW, enabling all of the processing features.

To disable an individual processing feature, set the corresponding IOPROC\_DISABLE bit HIGH in the IOPROC\_DISABLE register.

**Table 4-14: IOPROC\_DISABLE Register Bits**

| Processing Feature                      | IOPROC_DISABLE Register Bit     |
|-----------------------------------------|---------------------------------|
| TRS error correction and insertion      | TRS_INS                         |
| Y and C line based CRC error correction | CRC_INS                         |
| Y and C line number error correction    | LNUM_INS                        |
| Ancillary data check sum correction     | ANC_CHECKSUM_INSERTION          |
| EDH CRC error correction                | EDH_CRC_INS                     |
| Illegal code re-mapping                 | ILLEGAL_WORD_REMAP              |
| H timing signal configuration           | H_CONFIG                        |
| Update EDH Flags                        | EDH_FLAG_UPDATE                 |
| Ancillary Data Extraction               | ANC_DATA_EXT                    |
| Regeneration of 352M packets            | $\overline{\text{REGEN\_352M}}$ |

#### 4.18.1 TRS Correction & Insertion

When TRS Error Correction and Insertion is enabled, the GS2960A generates and overwrites TRS code words as required.

TRS Word Generation and Insertion is performed using the timing generated by the Timing Signal Generator. The timing signal generator performs bit error correction on incoming FVH information based on the Hamming code information embedded in the TRS-XYZ word. This provides an element of noise immunity over using just the received TRS information.

This feature is enabled when the IOPROC\_EN/ $\overline{\text{DIS}}$  pin is HIGH and the TRS\_INS\_DISABLE bit in the IOPROC\_DISABLE register is set LOW.

**NOTE:** Inserted TRS code words are always 10-bit compliant, irrespective of the bit depth of the incoming video stream.

### 4.18.2 Line Based CRC Correction & Insertion

When CRC Error Correction and Insertion is enabled, the GS2960A generates and inserts line based CRC words into both the Y and C channels of the data stream.

Line based CRC word generation and insertion only occur in HD and 3G modes, and is enabled when the IOPROC\_EN/ $\overline{\text{DIS}}$  pin is HIGH and the CRC\_INS\_DSX\_MASK bit in the IOPROC\_X register is set LOW.

### 4.18.3 Line Number Error Correction & Insertion

When Line Number Error Correction and Insertion is enabled, the GS2960A calculates and inserts line numbers into the output data stream. Re-calculated line numbers are inserted into both the Y and C channels.

Line number generation is in accordance with the relevant HD or 3G video standard as determined by the Automatic Standards Detection block.

This feature is enabled when the device is operating in HD or 3G modes, the IOPROC\_EN/ $\overline{\text{DIS}}$  pin is HIGH and the LNUM\_INS\_DSX\_MASK bit in the IOPROC\_X register is set LOW.

### 4.18.4 ANC Data Checksum Error Correction & Insertion

When ANC data Checksum Error Correction and Insertion is enabled, the GS2960A generates and inserts ancillary data checksums for all ancillary data words by default.

Where user specified ancillary data has been programmed (see [Section 4.17.1](#)), only the checksums for the programmed ancillary data is corrected.

This feature is enabled when the IOPROC\_EN/ $\overline{\text{DIS}}$  pin is HIGH and the ANC\_CHECKSUM\_INSERTION\_DSX\_MASK bit in the IOPROC\_X register is set LOW.

### 4.18.5 EDH CRC Correction & Insertion

When EDH CRC Error Correction and Insertion is enabled, the GS2960A generates and overwrites full field and active picture CRC check-words.

Additionally, the device sets the active picture and full field CRC 'V' bits HIGH in the EDH packet. The AP\_CRC\_V and FF\_CRC\_V register bits only report the received EDH validity flags.

EDH FF and AP CRC's are only inserted when the device is operating in SD mode, and if the EDH data packet is detected in the received video data.

Although the GS2960A modifies and inserts EDH CRC's and EDH packet checksums, EDH error flags are only updated when the EDH\_FLAG\_UPDATE\_MASK bit is LOW.

This feature is enabled in SD mode, when the IOPROC\_EN/ $\overline{\text{DIS}}$  pin is HIGH and the EDH\_CRC\_INS\_MASK bit in the IOPROC\_1 register is set LOW.

## 4.18.6 Illegal Word Re-mapping

All words within the active picture (outside the horizontal and vertical blanking periods), between the values of 3FCh and 3FFh are re-mapped to 3FBh. All words within the active picture area between the values of 000h and 003h are remapped to 004h.

This feature is enabled when the IOPROC\_EN/ $\overline{\text{DIS}}$  pin is HIGH and the ILLEGAL\_WORD\_REMAP\_DSX\_MASK bit in the IOPROC\_X register is set LOW.

## 4.18.7 TRS and Ancillary Data Preamble Remapping

8-bit TRS and ancillary data preambles are re-mapped to 10-bit values. 8-bit to 10-bit mapping of TRS headers is only supported if the TRS values are 3FC 000 000. Other values such as 3FD, 3FE, 3FF, 001, 002 and 003 are not supported. This feature is enabled by default, and can be disabled via the IOPROC\_X register.

## 4.18.8 Ancillary Data Extraction

Ancillary data may be extracted externally from the GS2960A output stream using the Y/1ANC and C/2ANC signals, and external logic.

As an alternative, the GS2960A includes a FIFO, which extracts ancillary data using read access via the host interface to ease system implementation. The FIFO stores up to 2048 x 16 bit words of ancillary data in two separate 1024 word memory banks.

The device writes the contents of ANC packets into the FIFO, starting with the first Ancillary Data Flag (ADF), followed by up to 1024 words.

All Data Identification (DID), Secondary Data Identification (SDID), Data Count (DC), user data, and checksum words are written into the device memory.

The device detects ancillary data packet DID's placed anywhere in the video data stream, including the active picture area.

Ancillary data from the Y channel or Data Stream One is placed in the Least Significant Word (LSW) of the FIFO, allocated to the lower 8 bits of each FIFO address.

Ancillary data from the C channel or Data Stream Two is placed in the Most Significant Word (MSW) (upper 8 bits) of each FIFO address.

**NOTE:** Please refer to the ANC insertion and Extraction Application Note (Doc ID: 53410), for discrete steps and example of Ancillary data extraction.

In SD mode, ancillary data is placed in the LSW of the FIFO. The MSW is set to zero.

If the ANC\_TYPE registers are all set to zero, the device extracts all types of ancillary data. If programmable ancillary data extraction is required, then up to five types of ancillary data to be extracted can be programmed in the ANC\_TYPE registers (see [Section 4.17.1](#)).

Additionally, the lines from which the packets are to be extracted can be programmed into the ANC\_LINEA[10:0] and ANC\_LINEB[10:0] registers, allowing ancillary data from a maximum of two lines per frame to be extracted. If only one line number register is programmed (with the other set to zero), ancillary data packets are extracted from one line per frame only. When both registers are set to zero, the device extracts packets from all lines.

To start Ancillary Data Extraction, the ANC\_DATA\_EXT\_MASK bit of the host interface must be set LOW. Ancillary data packet extraction begins in the following frame (see [Figure 4-31: Ancillary Data Extraction - Step A](#)).

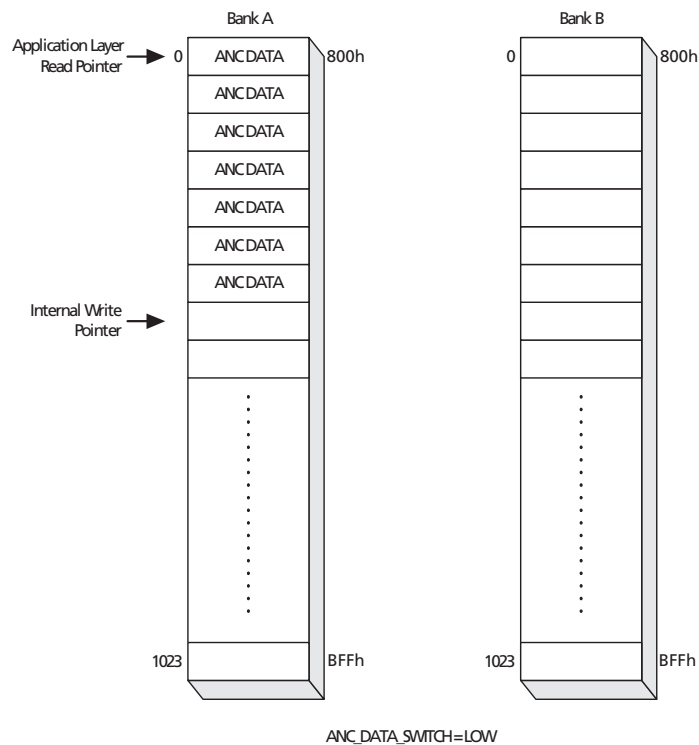


Figure 4-31: Ancillary Data Extraction - Step A

Ancillary data is written into Bank A until full. The Y/1ANC and C/2ANC output flags can be used to determine the length of the ancillary data extracted and when to begin reading the extracted data from memory.

While the ANC\_DATA\_EXT\_MASK bit is set LOW, the ANC\_DATA\_SWITCH bit can be set HIGH during or after reading the extracted data. New data is then written into Bank B (up to 1024 x 16-bit words), at the corresponding host interface addresses (see [Figure 4-32: Ancillary Data Extraction - Step B](#)).

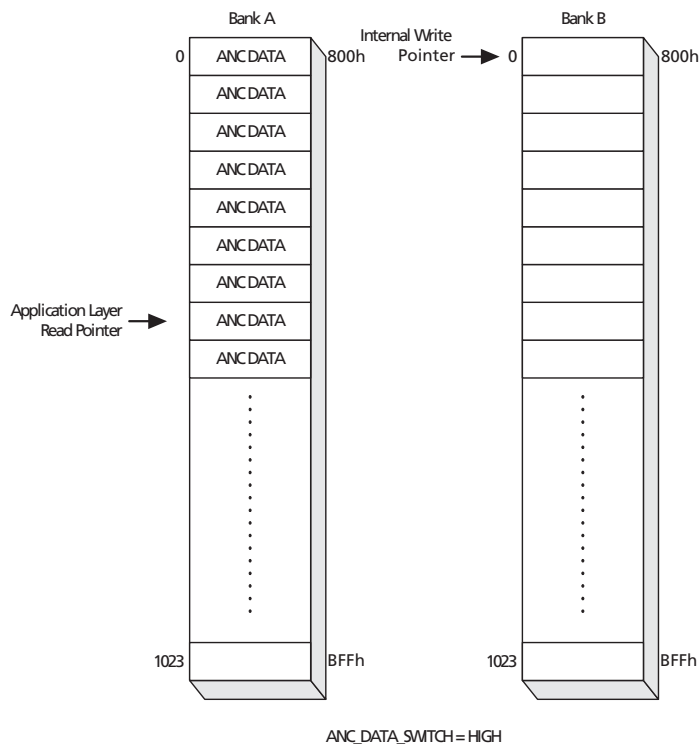


Figure 4-32: Ancillary Data Extraction - Step B

To read the new data, toggle the ANC\_DATA\_SWITCH bit LOW. The old data in Bank A is cleared to zero and extraction continues in Bank B (see [Figure 4-33: Ancillary Data Extraction - Step C](#)).

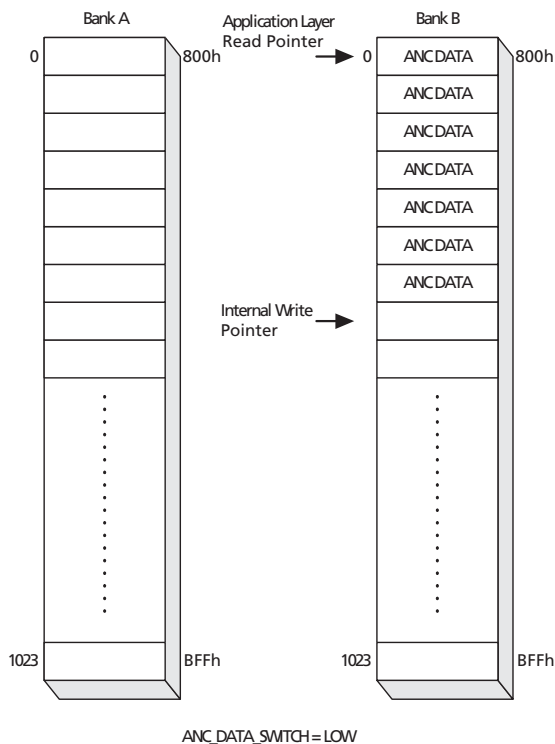


Figure 4-33: Ancillary Data Extraction - Step C

If the ANC\_DATA\_SWITCH bit is not toggled, extracted data is written into Bank B until full. To continue extraction in Bank A, the ANC\_DATA\_SWITCH bit must be toggled HIGH (see [Figure 4-34: Ancillary Data Extraction - Step D](#)).

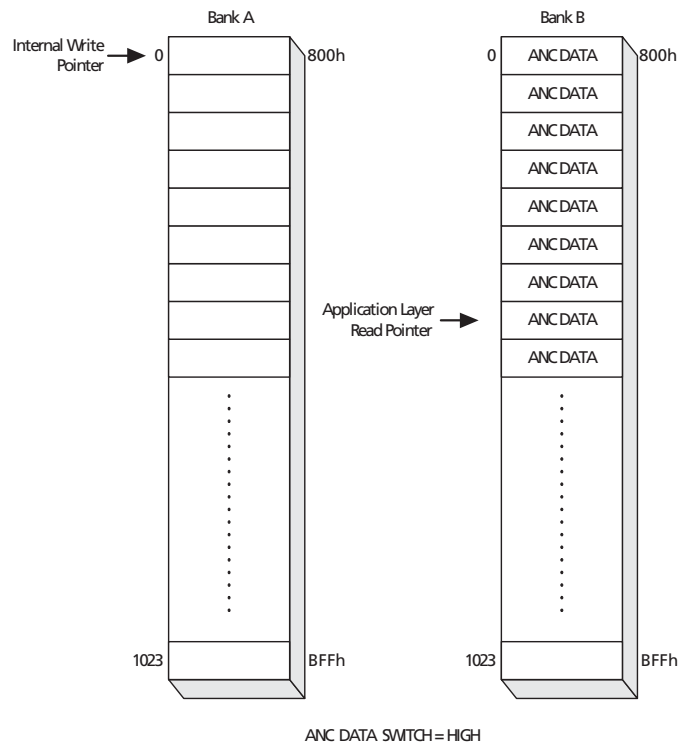


Figure 4-34: Ancillary Data Extraction - Step D

Toggling the ANC\_DATA\_SWITCH bit LOW returns the process to step A ([Figure 4-31](#)).

**NOTE:** Toggling the ANC\_DATA\_SWITCH must occur at a time when no extraction is taking place, i.e. when the both the Y/1ANC and C/2ANC signals are LOW.

To turn extraction off, the ANC\_DATA\_EXT\_MASK bit must be set HIGH.

In HD mode, the device can detect ancillary data packets in the Luma video data only, Chroma video data only, or both. By default (at power-up or after a system reset) the device extracts ancillary data packets from the luma channel only.

In 3G mode Level A, the device can detect ancillary data packets in Luma video (Data Stream One) only, Chroma video (Data Stream Two) only, or both. By default (at power-up or after a system reset) the device extracts ancillary data packets from Data Stream One only.

In 3G mode Level B mode, the device can detect ancillary data packets in Luma video only, Chroma video only, or both from either Link A or Link B. Selection of Link A or Link B for ANC data extraction is done via the host interface. By default (at power-up or after a system reset) the device extracts ancillary data packets from Link A Luma only.

To extract packets from the Chroma/Data Stream Two channel only, the HD\_ANC\_C2 bit of the host interface must be set HIGH. To extract packets from both Luma/Data Stream One and Chroma/Data Stream Two video data, the HD\_ANC\_Y1\_C2 bit must be set HIGH (the setting of the HD\_ANC\_C2 bit is ignored).

The default setting of both the HD\_ANC\_C2 and HD\_ANC\_Y1\_C2 is LOW. The setting of these bits is ignored when the device is configured for SD video standards.

Ancillary data packet extraction and deletion is disabled when the IOPROC\_EN/ $\overline{\text{DIS}}$  pin is set LOW.

After extraction, the ancillary data may be deleted from the video stream by setting the ANC\_DATA\_DEL bit of the host interface HIGH. When set HIGH, all existing ancillary data is removed and replaced with blanking values. If any of the ANC\_TYPE registers are programmed with a DID and/or DID and SDID, only the ancillary data packets with the matching IDs are deleted from the video stream.

**NOTE 1:** After the ancillary data determined by the ANC\_TYPE\_X\_APX registers has been deleted, other existing ancillary data may not be contiguous. The device does not concatenate the remaining ancillary data.

**NOTE 2:** Reading extracted ancillary data from the host interface must be performed while there is a valid video signal present at the serial input and the device is locked (LOCKED signal is HIGH).

### 4.18.9 Level B to Level A Conversion

When IOPROC\_2 register bit LEVEL\_B2A\_CONV\_DISABLE\_MASK is HIGH (default), the GS2960A does not convert 3G LEVEL B streams between Level A and Level B mapping formats.

When LEVEL\_B2A\_CONV\_DISABLE\_MASK is LOW, the GS2960A converts a 3G 1080p Level B stream to the Level A mapping format, as per SMPTE 425M.

The device assumes that Link A and Link B are phase-aligned at the transmitter.

The output data are line multiplexed such that the data content from Link A and Link B are assembled in a continuous fashion, at twice the input data rate. Extracted timing reference information is used to trigger a line counter which embeds the correct line number according to SMPTE 425M.

The Level B/A conversion acts only on the active picture, ANC data can become corrupt outside of this region. In order to ensure that the embedded ANC data remains valid, we recommend extracting the ANC data with the receiver prior to the Level B/A conversion taking place.

**NOTE 1:** If Level B/A conversion is enabled, previous 352M Payload ID packets are not deleted from the data stream.

**NOTE 2:** When Level B/A conversion is enabled, timing reference information (FVH as well as CEA861 timing) present on the STAT outputs is not phase-aligned with the output video data, and should not be used for line or frame synchronization activities. Being that CEA 861 timing is derived from (FVH) timing reference information, it too should not be used. During Level B to Level A conversion, it is advised that the user generates the H and V timing signals from the embedded TRS words.

**NOTE 3:** If the GS2960A sees a synchronous switch where the difference in phases between two Level B inputs is greater than  $\sim 10.7\mu\text{s}$ , the user may observe a missing H pulse on the line following the switch line, when Level B/A conversion is enabled.

**NOTE 4:** Discontinuities in the line of video at the input of the Level B to A converter can cause erroneous mapping to the Level A format. Therefore, when enabling B to A

conversion, it is recommended to reset the Level B to A converter with the following sequence:

1. Assert the B to A converter reset by writing '1' to bit 3 of register 05Eh.
2. Monitor H-pulse for a high-to-low transition.
3. De-assert the B to A converter reset by writing '0' to bit 3 of register 05Eh. This must be completed at the beginning of SAV and should be completed in 1920 PCLK periods.

## 4.19 GSPI - HOST Interface

The GSPI, or Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the system to access additional status and control information through configuration registers in the GS2960A.

The GSPI is comprised of a Serial Data Input signal (SDIN), Serial Data Output signal (SDOUT), an active low Chip Select ( $\overline{CS}$ ), and a Burst Clock (SCLK).

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/ $\overline{HOST}$  is provided.

When JTAG/ $\overline{HOST}$  is LOW, the GSPI interface is enabled. When JTAG/ $\overline{HOST}$  is HIGH, the JTAG interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and  $\overline{CS}$  signals must be provided by the system. The SDOUT pin is a non-clocked loop-through of SDIN and may be connected to the SDIN of another device, allowing multiple devices to be connected to the GSPI chain. See [Section 4.19.2](#) for details. The interface is illustrated in the [Figure 4-35](#) below.

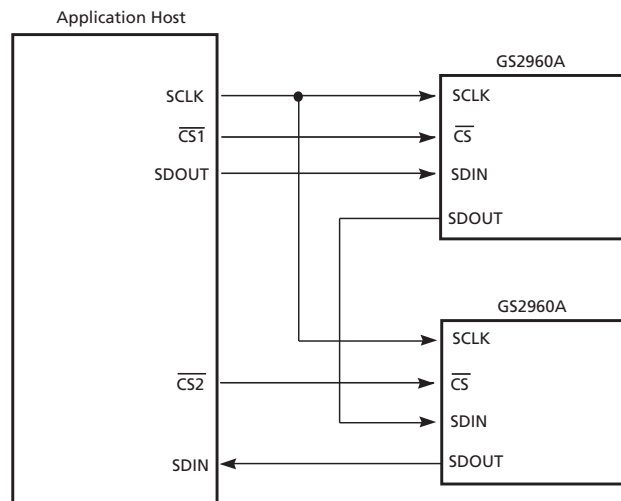


Figure 4-35: GSPI Application Interface Connection

All read or write access to the GS2960A is initiated and terminated by the system host processor. Each access always begins with a Command/Address Word, followed by a data write to, or data read from, the GS2960A.

### 4.19.1 Command Word Description

The Command Word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Increment bit and a 12-bit address.

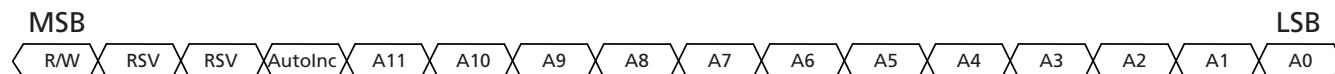


Figure 4-36: Command Word Format

Command Words are clocked into the GS2960A on the rising edge of the Serial Clock SCLK, which operates in a burst fashion. The chip select ( $\overline{CS}$ ) signal must be set low a minimum of 1.5ns ( $t_0$  in Figure 4-38) before the first clock edge to ensure proper operation.

When the Auto-Increment bit is set LOW, each Command Word must be followed by only one Data Word to ensure proper operation.

If the Auto-Increment bit is set HIGH, the following Data Word is written into the address specified in the Command Word, and subsequent Data Words are written into incremental addresses from the first Data Word. This facilitates multiple address writes without sending a Command Word for each Data Word.

**NOTE:** The RSV bits in the GSPI command word can be set to zero as placeholder, though these bits are not used.

### 4.19.2 Data Read or Write Access

During a read sequence (Command Word R/W bit set HIGH) serial data is transmitted or received MSB first, synchronous with the rising edge of the serial clock SCLK. The Chip Select ( $\overline{CS}$ ) signal must be set low a minimum of 1.5ns ( $t_0$  in Figure 4-38) before the first clock edge to ensure proper operation. The first bit (MSB) of the Serial Output (SDOUT) is available ( $t_5$  in Figure 4-39) following the last falling SCLK edge of the read Command Word, the remaining bits are clocked out on the negative edges of SCLK.

**NOTE:** When several devices are connected to the GSPI chain, only one  $\overline{CS}$  may be asserted during a read sequence.

During a write sequence (Command Word R/W bit set LOW), a wait state of 37.1ns ( $t_4$  in Figure 4-38) is required between the Command Word and the following Data Word. This wait state must also be maintained between successive Command Word/Data Word write sequences. When Auto Increment mode is selected (AutoInc = 1), the wait state must be maintained between successive Data Words after the initial Command Word/Data Word sequence.

During the write sequence, all Command and following Data Words input at the SDIN pin are output at the SDOUT pin unchanged. When several devices are connected to the GSPI chain, data can be written simultaneously to all the devices which have  $\overline{CS}$  set LOW.

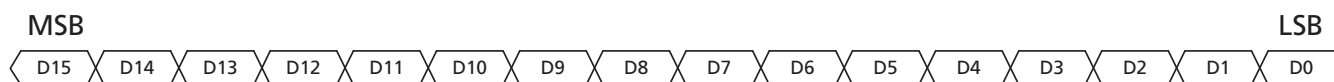


Figure 4-37: Data Word Format

### 4.19.3 GSPI Timing

Write and Read Mode timing for the GSPI interface;

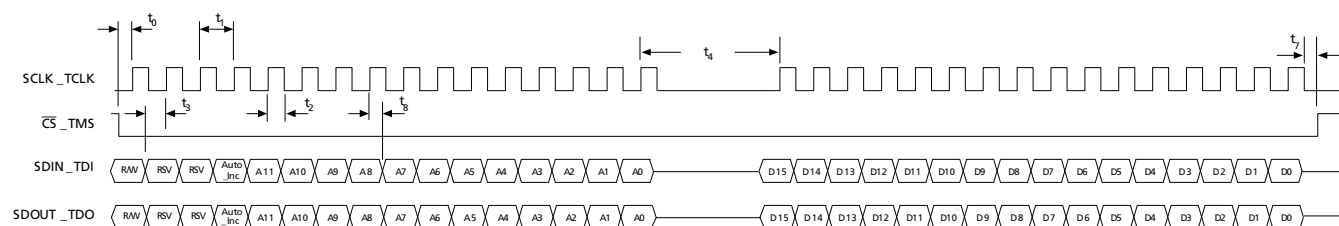


Figure 4-38: Write Mode

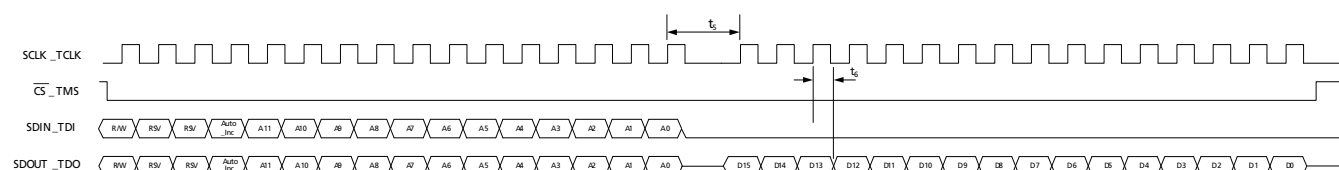


Figure 4-39: Read Mode

SDIN\_TDI to SDOUT\_TDO combinational path for daisy chain connection of multiple GS2960A devices.

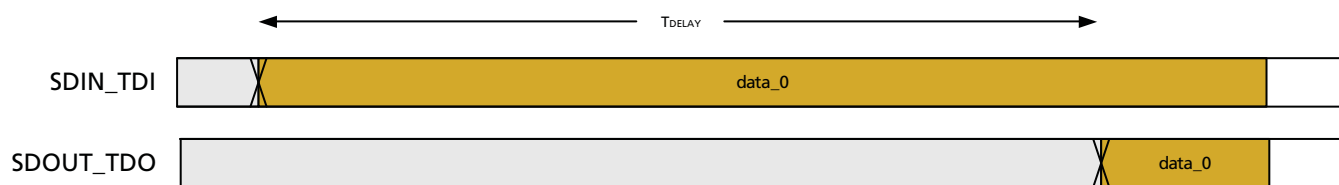


Figure 4-40: GSPI Time Delay

Table 4-15: GSPI Time Delay

| Parameter  | Symbol             | Conditions                 | Min | Typ | Max  | Units |
|------------|--------------------|----------------------------|-----|-----|------|-------|
| Delay Time | $t_{\text{DELAY}}$ | 50% levels; 1.8V operation | -   | -   | 13.1 | ns    |
| Delay Time | $t_{\text{DELAY}}$ | 50% levels; 3.3V operation | -   | -   | 9.7  | ns    |

**Table 4-16: GSPI Timing Parameters** (50% levels; 3.3V or 1.8V operation)

| Parameter                                                                                                                                    | Symbol         | Min        | Typ   | Max | Units |    |
|----------------------------------------------------------------------------------------------------------------------------------------------|----------------|------------|-------|-----|-------|----|
| $\overline{CS}$ low before SCLK rising edge                                                                                                  | t <sub>0</sub> | 1.5        | –     | –   | ns    |    |
| SCLK period                                                                                                                                  | t <sub>1</sub> | 16.67      | –     |     | ns    |    |
| SCLK duty cycle                                                                                                                              | t <sub>2</sub> | 40         | 50    | 60  | %     |    |
| Input data setup time                                                                                                                        | t <sub>3</sub> | 1.5        | –     | –   | ns    |    |
| Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – write cycle                | t <sub>4</sub> | PCLK (MHz) | ns    | –   | –     | ns |
|                                                                                                                                              |                | unlocked   | 100   |     |       |    |
|                                                                                                                                              |                | 27.0       | 37.1  |     |       |    |
|                                                                                                                                              |                | 74.25      | 13.5  |     |       |    |
|                                                                                                                                              |                | 148.5      | 6.7   |     |       |    |
| Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – read cycle.                | t <sub>5</sub> | PCLK (MHz) | ns    | –   | –     | ns |
|                                                                                                                                              |                | unlocked   | –     |     |       |    |
|                                                                                                                                              |                | 27.0       | 148.4 |     |       |    |
|                                                                                                                                              |                | 74.25      | 53.9  |     |       |    |
|                                                                                                                                              |                | 148.5      | 27    |     |       |    |
| Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – read cycle - ANC FIFO Read | t <sub>5</sub> | 222.6      | –     | –   | ns    |    |
| Output hold time (15pF load)                                                                                                                 | t <sub>6</sub> | 1.5        | –     | –   | ns    |    |
| $\overline{CS}$ high after last SCLK rising edge                                                                                             | t <sub>7</sub> | PCLK (MHz) | ns    | –   | –     | ns |
|                                                                                                                                              |                | unlocked   | 445   |     |       |    |
|                                                                                                                                              |                | 27.0       | 37.1  |     |       |    |
|                                                                                                                                              |                | 74.25      | 13.5  |     |       |    |
|                                                                                                                                              |                | 148.5      | 6.7   |     |       |    |
| Input data hold time                                                                                                                         | t <sub>8</sub> | 1.5        | –     | –   | ns    |    |

This timing must be satisfied across all ambient temperature and power supply operating conditions, as described in the [Electrical Characteristics on page 14](#).

## 4.20 Host Interface Register Maps

Table 4-17: Configuration and Status Registers

| Address | Register Name | Bit Name                        | Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                 | R/W | Default |
|---------|---------------|---------------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|
| 000h    | IOPROC_1      | RSVD                            | 15  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                   | R   | 0       |
|         |               | TRS_WORD_REMAP_DS1_DISABLE      | 14  | Disables 8-bit TRS word remapping for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.                                                                                                                                                                                                                                                                                                               | R/W | 0       |
|         |               | RSVD                            | 13  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                   | R/W | 0       |
|         |               | EDH_FLAG_UPDATE_MASK            | 12  | Disables updating of EDH error flags.                                                                                                                                                                                                                                                                                                                                                                       | R/W | 0       |
|         |               | EDH_CRC_INS_MASK                | 11  | Disables EDH_CRC error correction and insertion.                                                                                                                                                                                                                                                                                                                                                            | R/W | 0       |
|         |               | H_CONFIG                        | 10  | Selects the H blanking indication:<br>0: Active line blanking - the H output is HIGH for all the horizontal blanking period, including the EAV and SAV TRS words.<br>1: TRS based blanking - the H output is set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS signals.<br>This signal is only valid when TIM_861 is set to '0' (via pin or host interface). | R/W | 0       |
|         |               | ANC_DATA_EXT_MASK               | 9   | Disables ancillary data extraction FIFO.                                                                                                                                                                                                                                                                                                                                                                    | R/W | 0       |
|         |               | RSVD                            | 8   | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                   | R/W | 0       |
|         |               | TIM_861_PIN_DISABLE             | 7   | Disable TIM_861 pin control when set to '1', and use TIMING_861 bit instead.                                                                                                                                                                                                                                                                                                                                | R/W | 0       |
|         |               | TIMING_861                      | 6   | Selects the output timing reference format: 0 = Digital FVH timing output; 1 = CEA-861 timing output.                                                                                                                                                                                                                                                                                                       | R/W | 0       |
|         |               | RSVD                            | 5   | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                   | R/W | 0       |
|         |               | ILLEGAL_WORD_REMAP_DS1_MASK     | 4   | Disables illegal word remapping for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.                                                                                                                                                                                                                                                                                                                 | R/W | 0       |
|         |               | ANC_CHECKSUM_INSERTION_DS1_MASK | 3   | Disables insertion of ancillary data checksums for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.                                                                                                                                                                                                                                                                                                  | R/W | 0       |
|         |               | CRC_INS_DS1_MASK                | 2   | Disables insertion of HD/3G CRC words for 3G Level B Data Stream 1, 3G Level A, and HD inputs.                                                                                                                                                                                                                                                                                                              | R/W | 0       |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address | Register Name | Bit Name                   | Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                  | R/W | Default |
|---------|---------------|----------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|
| 000h    | IOPROC_1      | LNUM_INS_DS1_MASK          | 1   | Disables insertion of line numbers for 3G Level B Data Stream 1, 3G Level A, and HD inputs.                                                                                                                                                                                                                                                                                                                                                                  | R/W | 0       |
|         |               | TRS_INS_DS1_MASK           | 0   | Disables insertion of TRS words for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.                                                                                                                                                                                                                                                                                                                                                                  | R/W | 0       |
| 001h    | IOPROC_2      | RSVD                       | 15  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                    | R/W | N/A     |
|         |               | NONINV                     | 14  | With DISB_AUTDET set HIGH, if this bit is asserted (HIGH), forces non-inverted MPEG-2 decoding. If deasserted (LOW), forces inverted MPEG-2 decoding. Applicable in DVB-ASI mode only.                                                                                                                                                                                                                                                                       | R/W | 0       |
|         |               | DISB_AUTDET                | 13  | Disables auto detection of inverted DVB ASI MPEG-2 data when HIGH. When LOW, NONINV is ignored and the DVB decoder auto detects for inverted MPEG-2 data. Applicable in DVB-ASI mode only.                                                                                                                                                                                                                                                                   | R/W | 0       |
|         |               | TRS_WORD_REMAP_DS2_DISABLE | 12  | Disables 8-bit TRS word remapping in Data Stream 2 (3G Level B only).                                                                                                                                                                                                                                                                                                                                                                                        | R/W | 0       |
|         |               | RSVD                       | 11  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                    | R/W | 0       |
|         |               | REGEN_352M_MASK            | 10  | Disables regeneration of the SMPTE 352M packet for 3G Level B data. Note: this bit needs to be enabled via the host interface to disable SMPTE 352M packet generation. It is strongly recommended to set this bit LOW only when Level B to Level A conversion is enabled.                                                                                                                                                                                    | R/W | 0       |
|         |               | DS_SWAP_3G                 | 9   | Swaps Data Stream 1 (DS1) and Data Stream 2 (DS2) at the output in 3G mode.<br><br>In 20-bit output mode, DS1 shall be present on DOUT pins [19:10] and DS2 shall be present on DOUT pins [9:0] by default. When DS_SWAP_3G is set to '1', DS2 shall be present on DOUT pins [19:10] and DS1 shall be present on DOUT pins [9:0]<br><br>In 10-bit (DDR) output mode, DS2 shall precede DS1 by default. When DS_SWAP_3G is set to '1', DS1 shall precede DS2. | R/W | 0       |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address | Register Name | Bit Name                        | Bit | Description                                                                                                                                                                                   | R/W | Default |
|---------|---------------|---------------------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|
| 001h    | IOPROC_2      | LEVEL_B2A_CONV_DISABLE_MASK     | 8   | Disable conversion of a 3G Level B input to a 3G Level A format. Only effective if in 3G Level B mode. Default is active HIGH (disabled), so Level B inputs are formatted as Level B outputs. | R/W | 1       |
|         |               | ANC_EXT_SEL_DS2_DS1             | 7   | Selects data stream to extract ANC data from (valid for 3G Level B data).                                                                                                                     | R/W | 0       |
|         |               | RSVD                            | 6-5 | Reserved.                                                                                                                                                                                     | R/W | 0       |
|         |               | ILLEGAL_WORD_REMAP_DS2_MASK     | 4   | Disables illegal word remapping in Data Stream 2 (3G Level B only).                                                                                                                           | R/W | 0       |
|         |               | ANC_CHECKSUM_INSERTION_DS2_MASK | 3   | Disables insertion of ancillary data checksums in Data Stream 2 (3G Level B only).                                                                                                            | R/W | 0       |
|         |               | CRC_INS_DS2_MASK                | 2   | Disables insertion of CRC words in Data Stream 2 (3G Level B only).                                                                                                                           | R/W | 0       |
|         |               | LNUM_INS_DS2_MASK               | 1   | Disables insertion of line numbers in Data Stream 2 (3G Level B only).                                                                                                                        | R/W | 0       |
|         |               | TRS_INS_DS2_MASK                | 0   | Disable insertion of TRS words in Data Stream 2 (3G Level B only).                                                                                                                            | R/W | 0       |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address | Register Name | Bit Name       | Bit   | Description                                                                                                 | R/W  | Default |
|---------|---------------|----------------|-------|-------------------------------------------------------------------------------------------------------------|------|---------|
| 002h    | ERROR_STAT_1  | RSVD           | 15-11 | Reserved.                                                                                                   | ROCW | 0       |
|         |               | VD_STD_ERR_DS1 | 10    | Video Standard Error indication for HD and SD inputs.                                                       | ROCW | 0       |
|         |               | FF_CRC_ERR     | 9     | EDH Full Frame CRC error indication.                                                                        | ROCW | 0       |
|         |               | AP_CRC_ERR     | 8     | EDH Active Picture CRC error indication.                                                                    | ROCW | 0       |
|         |               | RSVD           | 7     | Reserved.                                                                                                   | ROCW | 0       |
|         |               | CCS_ERR_DS1    | 6     | Chroma ancillary data checksum error indication for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs. | ROCW | 0       |
|         |               | YCS_ERR_DS1    | 5     | Luma ancillary data checksum error indication for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.   | ROCW | 0       |
|         |               | CCRC_ERR_DS1   | 4     | Chroma CRC error indication for 3G Level B Data Stream 1, 3G Level A, and HD inputs.                        | ROCW | 0       |
|         |               | YCRC_ERR_DS1   | 3     | Luma CRC error indication for 3G Level B Data Stream 1, 3G Level A, and HD inputs.                          | ROCW | 0       |
|         |               | LNUM_ERR_DS1   | 2     | Line number error indication for 3G Level B Data Stream 1, 3G Level A, and HD inputs.                       | ROCW | 0       |
|         |               | SAV_ERR_DS1    | 1     | SAV error indication for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.                            | ROCW | 0       |
|         |               | EAV_ERR_DS1    | 0     | EAV error indication for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.                            | ROCW | 0       |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address | Register Name | Bit Name     | Bit  | Description                                                                          | R/W  | Default |
|---------|---------------|--------------|------|--------------------------------------------------------------------------------------|------|---------|
| 003h    | ERROR_STAT_2  | RSVD         | 15-7 | Reserved.                                                                            | ROCW | 0       |
|         |               | CCS_ERR_DS2  | 6    | Chroma ancillary data checksum error indication for Data Stream 2 (3G Level B only). | ROCW | 0       |
|         |               | YCS_ERR_DS2  | 5    | Luma ancillary data checksum error indication for Data Stream 2 (3G Level B only).   | ROCW | 0       |
|         |               | CCRC_ERR_DS2 | 4    | Chroma CRC error indication for Data Stream 2 (3G Level B only).                     | ROCW | 0       |
|         |               | YCRC_ERR_DS2 | 3    | Luma CRC error indication for Data Stream 2 (3G Level B only).                       | ROCW | 0       |
|         |               | LNUM_ERR_DS2 | 2    | Line number error indication for Data Stream 2 (3G Level B only).                    | ROCW | 0       |
|         |               | SAV_ERR_DS2  | 1    | SAV error indication for Data Stream 2 (3G Level B only).                            | ROCW | 0       |
|         |               | EAV_ERR_DS2  | 0    | EAV error indication for Data Stream 2 (3G Level B only).                            | ROCW | 0       |
| 004h    | EDH_FLAG_IN   | EDH_DETECT   | 15   | Embedded EDH packet detected.                                                        | RO   | 0       |
|         |               | ANC_UES_IN   | 14   | Ancillary data – unknown error status flag.                                          | RO   | 0       |
|         |               | ANC_IDA_IN   | 13   | Ancillary data – internal error detected already flag.                               | RO   | 0       |
|         |               | ANC_IDH_IN   | 12   | Ancillary data – internal error detected here flag                                   | RO   | 0       |
|         |               | ANC_EDA_IN   | 11   | Ancillary data – error detected already flag.                                        | RO   | 0       |
|         |               | ANC_EDH_IN   | 10   | Ancillary data – error detected here flag.                                           | RO   | 0       |
|         |               | FF_UES_IN    | 9    | EDH Full Field – unknown error status flag.                                          | RO   | 0       |
|         |               | FF_IDA_IN    | 8    | EDH Full Field – internal error detected already flag.                               | RO   | 0       |
|         |               | FF_IDH_IN    | 7    | EDH Full Field – internal error detected here flag.                                  | RO   | 0       |
|         |               | FF_EDA_IN    | 6    | EDH Full Field – error detected already flag.                                        | RO   | 0       |
|         |               | FF_EDH_IN    | 5    | EDH Full Field – error detected here flag.                                           | RO   | 0       |
|         |               | AP_UES_IN    | 4    | EDH Active Picture – unknown error status flag.                                      | RO   | 0       |
|         |               | AP_IDA_IN    | 3    | EDH Active Picture – internal error detected already flag.                           | RO   | 0       |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address | Register Name | Bit Name  | Bit | Description                                                | R/W | Default |
|---------|---------------|-----------|-----|------------------------------------------------------------|-----|---------|
| 004h    | EDH_FLAG_IN   | AP_IDH_IN | 2   | EDH Active Picture – internal error detected here flag.    | RO  | 0       |
|         |               | AP_EDA_IN | 1   | EDH Active Picture – error detected already flag.          | RO  | 0       |
|         |               | AP_EDH_IN | 0   | EDH Active Picture – error detected here flag.             | RO  | 0       |
| 005h    | EDH_FLAG_OUT  | RSVD      | 15  | Reserved.                                                  | RO  | 0       |
|         |               | ANC_UES   | 14  | Ancillary data – Unknown Error Status flag.                | RO  | 1       |
|         |               | ANC_IDA   | 13  | Ancillary data – Internal error Detected Already flag.     | RO  | 0       |
|         |               | ANC_IDH   | 12  | Ancillary data – Internal error Detected Here flag.        | RO  | 0       |
|         |               | ANC_EDA   | 11  | Ancillary data – Error Detected Already flag.              | RO  | 0       |
|         |               | ANC_EDH   | 10  | Ancillary data – Error Detected Here flag.                 | RO  | 0       |
|         |               | FF_UES    | 9   | EDH Full Field – Unknown Error Status flag.                | RO  | 1       |
|         |               | FF_IDA    | 8   | EDH Full Field – Internal error Detected Already flag.     | RO  | 0       |
|         |               | FF_IDH    | 7   | EDH Full Field – Internal error Detected Here flag.        | RO  | 0       |
|         |               | FF_EDA    | 6   | EDH Full Field – Error Detected Already flag.              | RO  | 0       |
|         |               | FF_EDH    | 5   | EDH Full Field – Error Detected Here flag.                 | RO  | 0       |
|         |               | AP_UES    | 4   | EDH Active Picture – Unknown Error Status flag.            | RO  | 1       |
|         |               | AP_IDA    | 3   | EDH Active Picture – Internal error Detected Already flag. | RO  | 0       |
|         |               | AP_IDH    | 2   | EDH Active Picture – Internal error Detected Here flag.    | RO  | 0       |
|         |               | AP_EDA    | 1   | EDH Active Picture – Error Detected Already flag.          | RO  | 0       |
|         |               | AP_EDH    | 0   | EDH Active Picture – Error Detected Here flag.             | RO  | 0       |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address | Register Name   | Bit Name         | Bit   | Description                                                                                                                                                    | R/W | Default |
|---------|-----------------|------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|
| 006h    | DATA_FORMAT_DS1 | FF_CRC_V         | 15    | EDH Full Field CRC Validity bit.                                                                                                                               | RO  | 0       |
|         |                 | AP_CRC_V         | 14    | EDH Active Picture CRC Validity bit.                                                                                                                           | RO  | 0       |
|         |                 | VD_STD_DS1       | 13-8  | Detected Video Standard for 3G Level B Data Stream 1, 3G Level A, HD and SD inputs.                                                                            | RO  | 29      |
|         |                 | CDATA_FORMAT_DS1 | 7-4   | Data format as indicated in Chroma channel for 3G Level B Data Stream 1, HD and SD inputs;<br>Data format as indicated in Data Stream 2 for 3G Level A inputs. | RO  | 15      |
|         |                 | YDATA_FORMAT_DS1 | 3-0   | Data format as indicated in Luma channel for 3G Level B Data Stream 1, HD and SD inputs;<br>Data format as indicated in Data Stream 1 for 3G Level A inputs.   | RO  | 15      |
| 007h    | DATA_FORMAT_DS2 | RSVD             | 15-14 | Reserved.                                                                                                                                                      | RO  | 0       |
|         |                 | VD_STD_DS2       | 13-8  | Detected Video Standard for Data Stream 2 (3G Level B only).                                                                                                   | RO  | 29      |
|         |                 | CDATA_FORMAT_DS2 | 7-4   | Data Format as indicated in Chroma channel for Data Stream 2 (3G Level B only).                                                                                | RO  | 15      |
|         |                 | YDATA_FORMAT_DS2 | 3-0   | Data Format as indicated in Luma channel for Data Stream 2 (3G Level B only).                                                                                  | RO  | 15      |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address | Register Name | Bit Name     | Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | R/W | Default |
|---------|---------------|--------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|
| 008h    | IO_CONFIG     | RSVD         | 15    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | RW  | 0       |
|         |               | STAT2_CONFIG | 14-10 | Configure STAT2 output pin:<br>00000: H Blanking when TIM_861 = 0; HSYNC when TIM_861 = 1<br>00001: V Blanking when TIM_861 = 0; VSYNC when TIM_861 = 1<br>00010: F bit when TIM_861 = 0; Data Enable (DE) when TIM_861 = 1<br>00011: LOCKED<br>00100: Y/1ANC: ANC indication (SD), Luma ANC indication (HD), Data Stream 1 ANC data indication (3G)<br>00101: C/2ANC: Chroma ANC indication (HD) or Data Stream 2 ANC data indication (3G)<br>00110: Data Error<br>00111: Video Error<br>01000: Reserved<br>01001: EDH Detected<br>01010: Carrier Detect<br>01011: RATE_DET0<br>01100: RATE_DET1<br>01101 - 11111: Reserved | RW  | 2       |
|         |               | STAT1_CONFIG | 9-5   | Configure STAT1 output pin. (Refer to above for decoding)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | RW  | 1       |
|         |               | STAT0_CONFIG | 4-0   | Configure STAT0 output pin. (Refer to above for decoding)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | RW  | 0       |
| 009h    | IO_CONFIG2    | RSVD         | 15    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | RW  | 0       |
|         |               | STAT5_CONFIG | 14-10 | Configure STAT5 output pin. (Refer to above for decoding)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | RW  | 6       |
|         |               | STAT4_CONFIG | 9-5   | Configure STAT4 output pin. (Refer to above for decoding)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | RW  | 4       |
|         |               | STAT3_CONFIG | 4-0   | Configure STAT3 output pin. (Refer to above for decoding)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | RW  | 3       |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address     | Register Name  | Bit Name        | Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                               | R/W | Default |
|-------------|----------------|-----------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|
| 00Ah        | ANC_CONTROL    | RSVD            | 15-4  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                 | RW  | 0       |
|             |                | ANC_DATA_SWITCH | 3     | Switches between FIFO memories.                                                                                                                                                                                                                                                                                                                                                                           | RW  | 0       |
|             |                | ANC_DATA_DEL    | 2     | Remove Ancillary Data from output video stream, set to Luma and Chroma blanking values.                                                                                                                                                                                                                                                                                                                   | RW  | 0       |
|             |                | HD_ANC_Y1_C2    | 1     | Extract Ancillary data from Luma and Chroma channels (HD inputs)<br>Extract Ancillary data from Data Stream 1 and Data Stream 2 (3G Level A inputs)<br>Extract Ancillary data from Luma and Chroma channels of Data Stream 1 (3G Level B inputs, when ANC_EXT_SEL_DS2_DS1 = 0)<br>Extract Ancillary data from Luma and Chroma channels of Data Stream 2 (3G Level B inputs, when ANC_EXT_SEL_DS2_DS1 = 1) | RW  | 0       |
|             |                | HD_ANC_C2       | 0     | Extract Ancillary data only from Chroma channel (HD inputs)<br>Extract Ancillary data only from Data Stream 2 (3G Level A inputs)<br>Extract Ancillary data only from Chroma channel of Data Stream 1 (3G Level B inputs, when ANC_EXT_SEL_DS2_DS1 = 0)<br>Extract Ancillary data only from Chroma channel of Data Stream 2 (3G Level B inputs, when ANC_EXT_SEL_DS2_DS1 = 1)                             | RW  | 0       |
| 00Bh        | ANC_LINE_A     | RSVD            | 15-11 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                 | R/W | 0       |
|             |                | ANC_LINE_A      | 10-0  | Video Line to extract Ancillary data from.                                                                                                                                                                                                                                                                                                                                                                | R/W | 0       |
| 00Ch        | ANC_LINE_B     | RSVD            | 15-11 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                 | R/W | 0       |
|             |                | ANC_LINE_B      | 10-0  | Second video Line to extract Ancillary data from.                                                                                                                                                                                                                                                                                                                                                         | R/W | 0       |
| 00Dh - 00Eh | RSVD           | RSVD            | 15-0  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                 | RO  | 0       |
| 00Fh        | ANC_TYPE_1_AP2 | ANC_TYPE1_DS1   | 15-0  | Programmable DID/SDID pair #1 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats ([15:8] = DID, [7:0] = SDID).                                                                                                                                                                                                                                                                 | R/W | 0       |
| 010h        | ANC_TYPE_2_AP1 | ANC_TYPE2_DS1   | 15-0  | Programmable DID/SDID pair #2 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats ([15:8] = DID, [7:0] = SDID).                                                                                                                                                                                                                                                                 | R/W | 0       |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address | Register Name            | Bit Name           | Bit  | Description                                                                                                                               | R/W | Default |
|---------|--------------------------|--------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|
| 011h    | ANC_TYPE_3<br>_AP1       | ANC_TYPE3_DS1      | 15-0 | Programmable DID/SDID pair #3 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats ([15:8] = DID, [7:0] = SDID). | R/W | 0       |
| 012h    | ANC_TYPE_4<br>_AP1       | ANC_TYPE4_DS1      | 15-0 | Programmable DID/SDID pair #4 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats ([15:8] = DID, [7:0] = SDID). | R/W | 0       |
| 013h    | ANC_TYPE_5<br>_AP1       | ANC_TYPE5_DS1      | 15-0 | Programmable DID/SDID pair #5 to extract from 3G Level B Data Stream 1, 3G Level A, HD and SD input formats ([15:8] = DID, [7:0] = SDID). | R/W | 0       |
| 014h    | ANC_TYPE_1<br>_AP2       | ANC_TYPE1_DS2      | 15-0 | Programmable DID/SDID pair #1 to extract from 3G Level B Data Stream 2 ([15:8] = DID, [7:0] = SDID).                                      | R/W | 0       |
| 015h    | ANC_TYPE_2<br>_AP2       | ANC_TYPE2_DS2      | 15-0 | Programmable DID/SDID pair #2 to extract from 3G Level B Data Stream 2 ([15:8] = DID, [7:0] = SDID).                                      | R/W | 0       |
| 016h    | ANC_TYPE_3<br>_AP2       | ANC_TYPE3_DS2      | 15-0 | Programmable DID/SDID pair #3 to extract from 3G Level B Data Stream 2 ([15:8] = DID, [7:0] = SDID).                                      | R/W | 0       |
| 017h    | ANC_TYPE_4<br>_AP2       | ANC_TYPE4_DS2      | 15-0 | Programmable DID/SDID pair #4 to extract from 3G Level B Data Stream 2 ([15:8] = DID, [7:0] = SDID).                                      | R/W | 0       |
| 018h    | ANC_TYPE_5<br>_AP2       | ANC_TYPE5_DS2      | 15-0 | Programmable DID/SDID pair #5 to extract from 3G Level B Data Stream 2 ([15:8] = DID, [7:0] = SDID).                                      | R/W | 0       |
| 019h    | VIDEO_FORMAT_<br>352_A_1 | VIDEO_FORMAT_2_DS1 | 15-8 | SMPTE 352M embedded packet – byte 2.                                                                                                      | R   | 0       |
|         |                          | VIDEO_FORMAT_1_DS1 | 7-0  | SMPTE 352M embedded packet – byte 1: [7]: Version identifier [6:0]: Video Payload Identifier.                                             | R   | 0       |
| 01Ah    | VIDEO_FORMAT_<br>352_B_1 | VIDEO_FORMAT_4_DS1 | 15-8 | SMPTE 352M embedded packet – byte 4.                                                                                                      | R   | 0       |
|         |                          | VIDEO_FORMAT_3_DS1 | 7-0  | SMPTE 352M embedded packet – byte 3.                                                                                                      | R   | 0       |
| 01Bh    | VIDEO_FORMAT_<br>352_A_2 | VIDEO_FORMAT_2_DS2 | 15-8 | SMPTE 352M embedded packet – byte 2 (3G Data Stream 2 only).                                                                              | R   | 0       |
|         |                          | VIDEO_FORMAT_1_DS2 | 7-0  | SMPTE 352M embedded packet – byte 1 (3G Data Stream 2 only):<br>[7]: Version identifier<br>[6:0]: Video Payload Identifier.               | R   | 0       |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address | Register Name          | Bit Name                                                                                                                                                                                            | Bit   | Description                                                                    | R/W | Default |
|---------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------------------------------------------------------------------------------|-----|---------|
| 01Ch    | VIDEO_FORMAT_352_B_2   | VIDEO_FORMAT_4_DS2                                                                                                                                                                                  | 15-8  | SMPTE 352M embedded packet – byte 4 (3G Data Stream 2 only).                   | R   | 0       |
|         |                        | VIDEO_FORMAT_3_DS2                                                                                                                                                                                  | 7-0   | SMPTE 352M embedded packet – byte 3 (3G Data Stream 2 only).                   | R   | 0       |
| 01Dh    | VIDEO_FORMAT_352_INS_A | VIDEO_FORMAT_2_INS                                                                                                                                                                                  | 15-8  | SMPTE 352M packet - byte 2 to be embedded after Level B to Level A conversion. | R/W | 0       |
|         |                        | VIDEO_FORMAT_1_INS                                                                                                                                                                                  | 7-0   | SMPTE 352M packet - byte 1 to be embedded after Level B to Level A conversion. | R/W | 0       |
| 01Eh    | VIDEO_FORMAT_352_INS_B | VIDEO_FORMAT_4_INS                                                                                                                                                                                  | 15-8  | SMPTE 352M packet - byte 4 to be embedded after Level B to Level A conversion. | R/W | 0       |
|         |                        | VIDEO_FORMAT_3_INS                                                                                                                                                                                  | 7-0   | SMPTE 352M packet - byte 3 to be embedded after Level B to Level A conversion. | R/W | 0       |
| 01Fh    | RASTER_STRUC_1         | RSVD                                                                                                                                                                                                | 15-14 | Reserved.                                                                      | R   | 0       |
|         |                        | WORDS_PER_ACTLINE                                                                                                                                                                                   | 13-0  | Words Per Active Line.                                                         | R   | 0       |
| 020h    | RASTER_STRUC_2         | RSVD                                                                                                                                                                                                | 15-14 | Reserved.                                                                      | R   | 0       |
|         |                        | WORDS_PER_LINE                                                                                                                                                                                      | 13-0  | Total Words Per Line.                                                          | R   | 0       |
| 021h    | RASTER_STRUC_3         | RSVD                                                                                                                                                                                                | 15-11 | Reserved.                                                                      | R   | 0       |
|         |                        | LINES_PER_FRAME                                                                                                                                                                                     | 10-0  | Total Lines Per Frame.                                                         | R   | 0       |
| 022h    | RASTER_STRUC_4         | RATE_SEL_READBACK                                                                                                                                                                                   | 15-14 | Read back detected data rate:<br>0 = HD,<br>1,3=SD,<br>2=3G                    | R   | 0       |
|         |                        | M                                                                                                                                                                                                   | 13    | Specifies detected M value<br>0: 1.000<br>1: 1.001                             | R   | 0       |
|         |                        | <b>Note:</b> In certain systems, due to greater ppm offsets in the crystal, the 'M' bit may not assert properly. In such cases, bits 3:0 in Register 06Fh can be increased to a maximum value of 4. |       |                                                                                |     |         |
|         |                        | STD_LOCK                                                                                                                                                                                            | 12    | Video standard lock.                                                           | R   | 0       |
|         |                        | INT_PROG                                                                                                                                                                                            | 11    | Interlaced or progressive.                                                     | R   | 0       |
|         |                        | ACTLINE_PER_FIELD                                                                                                                                                                                   | 10-0  | Active lines per frame.                                                        | R   | 0       |
|         |                        |                                                                                                                                                                                                     |       |                                                                                |     |         |
|         |                        |                                                                                                                                                                                                     |       |                                                                                |     |         |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address     | Register Name   | Bit Name      | Bit  | Description                                                                                                                                                                       | R/W | Default |
|-------------|-----------------|---------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|
| 023h        | FLYWHEEL_STATUS | RSVD          | 15-5 | Reserved.                                                                                                                                                                         | R   | 0       |
|             |                 | V_LOCK_DS2    | 4    | Indicates that the timing signal generator is locked to vertical timing (3G Level B Data Stream 2 only).                                                                          | R   | 0       |
|             |                 | H_LOCK_DS2    | 3    | Indicates that the timing signal generator is locked to horizontal timing (3G Level B Data Stream 2 only).                                                                        | R   | 0       |
|             |                 | RSVD          | 2    | Reserved.                                                                                                                                                                         | R   | 0       |
|             |                 | V_LOCK_DS1    | 1    | Indicates that the timing signal generator is locked to vertical timing (3G Level B Data Stream 1, 3G Level A, HD and SD inputs).                                                 | R   | 0       |
|             |                 | H_LOCK_DS1    | 0    | Indicates that the timing signal generator is locked to horizontal timing (3G Level B Data Stream 1, 3G Level A, HD and SD inputs).                                               | R   | 0       |
| 024h        | RATE_SEL        | RSVD          | 15-3 | Reserved.                                                                                                                                                                         | R   | 0       |
|             |                 | AUTO/MAN      | 2    | Detect data rate automatically (1) or program manually (0).                                                                                                                       | R/W | 1       |
|             |                 | RATE_SEL_TOP  | 1-0  | Programmable rate select in manual mode:<br>0 = HD,<br>1,3=SD,<br>2=3G                                                                                                            | R/W | 0       |
| 025h        | TIM_861_FORMAT  | RSVD          | 15-7 | Reserved.                                                                                                                                                                         | R   | 0       |
|             |                 | FORMAT_ERR    | 6    | Indicates standard is not recognized for CEA 861 conversion.                                                                                                                      | R   | 1       |
|             |                 | FORMAT_ID_861 | 5-0  | CEA-861 format ID of input video stream. Refer to <a href="#">Table 4-9</a> .                                                                                                     | R   | 0       |
| 026h        | TIM_861_CFG     | RSVD          | 15-3 | Reserved.                                                                                                                                                                         | R   | 0       |
|             |                 | VSYNC_INVERT  | 2    | Invert output VSYNC pulse.                                                                                                                                                        | R/W | 0       |
|             |                 | HSYNC_INVERT  | 1    | Invert output HSYNC pulse.                                                                                                                                                        | R/W | 0       |
|             |                 | TRS_861       | 0    | Sets the timing reference outputs to DFP timing mode when set to '1'. By default, the timing reference outputs follow CEA-861 timing mode. Only valid when TIM_861 is set to '1'. | R/W | 0       |
| 027h - 036h | RSVD            | RSVD          | 15-0 | Reserved.                                                                                                                                                                         | R   | 0       |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address      | Register Name | Bit Name         | Bit   | Description                                                                                                                                                                                                                                                                                                                                                                                         | R/W | Default |
|--------------|---------------|------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|
| 037h         | ERROR_MASK_1  | RSVD             | 15-11 | Reserved.                                                                                                                                                                                                                                                                                                                                                                                           | R   | 0       |
|              |               | ERROR_MASK_1     | 10-0  | Error mask for global error vector (3G Level B Data Stream 1, 3G Level A, HD, SD):<br>bit[0]: EAV_ERR_DS1 mask<br>bit[1]: SAV_ERR_DS1 mask<br>bit[2]: LNUM_ERR_DS1 mask<br>bit[3]: YCRC_ERR_DS1 mask<br>bit[4]: CCRC_ERR_DS1 mask<br>bit[5]: YCS_ERR_DS1 mask<br>bit[6]: CCS_ERR_DS1 mask<br>bit[7]: Reserved<br>bit[8]: AP_CRC_ERR mask<br>bit[9]: FF_CRC_ERR mask<br>bit[10]: VD_STD_ERR_DS1 mask | R/W | 0       |
| 038h         | ERROR_MASK_2  | RSVD             | 15-7  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                           | R   | 0       |
|              |               | ERROR_MASK_2     | 6-0   | Error mask for global error vector (3G Level B Data Stream 2 only):<br>bit[0]: EAV_ERR_DS2 mask<br>bit[1]: SAV_ERR_DS2 mask<br>bit[2]: LNUM_ERR_DS2 mask<br>bit[3]: YCRC_ERR_DS2 mask<br>bit[4]: CCRC_ERR_DS2 mask<br>bit[5]: YCS_ERR_DS2 mask<br>bit[6]: CCS_ERR_DS2 mask                                                                                                                          | R/W | 0       |
| 039h<br>-6Bh | RSVD          | RSVD             | 15-0  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                           | R   | 0       |
| 06Ch         | CLK_GEN       | RSVD             | 15-6  | Reserved.                                                                                                                                                                                                                                                                                                                                                                                           | R/W | 0       |
|              |               | DEL_LINE_CLK_SEL | 5     | Choses between the in-phase (0) and quadrature (1) clocks for DDR mode.                                                                                                                                                                                                                                                                                                                             | R/W | 0       |
|              |               | DEL_LINE_OFFSET  | 4-0   | Controls the offset for the delay line.                                                                                                                                                                                                                                                                                                                                                             | R/W | 0       |

**Table 4-17: Configuration and Status Registers (Continued)**

| Address     | Register Name         | Bit Name              | Bit   | Description                                                                                                                                                                                                                | R/W | Default |
|-------------|-----------------------|-----------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|
| 06Dh        | IO_DRIVE_STRENGTH     | RSVD                  | 15-6  | Reserved.                                                                                                                                                                                                                  | R/W | 0       |
|             |                       | IO_DS_CTRL_DOUT_MSB   | 5-4   | Drive strength adjustment for DOUT[19:10] outputs and PCLK output:<br>00: 4mA;<br>01: 8mA;<br>10: 10mA(1.8V), 12mA(3.3V);<br>11: 12mA(1.8V), 16mA(3.3V)                                                                    | R/W | 2       |
|             |                       | IO_DS_CTRL_STAT       | 3-2   | Drive strength adjustment for STAT[5:0] outputs:<br>00: 4mA;<br>01: 6mA;<br>10: 8mA(1.8V), 10mA(3.3V);<br>11: 10mA(1.8V), 12mA(3.3V)                                                                                       | R/W | 2       |
|             |                       | IO_DS_CTRL_DOUT_LSB   | 1-0   | Drive strength adjustment for DOUT[9:0] outputs:<br>00: 4mA;<br>01: 6mA;<br>10: 8mA(1.8V), 10mA(3.3V);<br>11: 10mA(1.8V), 12mA(3.3V)                                                                                       | R/W | 3       |
| 06Eh        | RSVD                  | RSVD                  | 15-0  | Reserved.                                                                                                                                                                                                                  | R/W | 0       |
| 06Fh        | RSVD                  | RSVD                  | 15-4  | Reserved.                                                                                                                                                                                                                  | R/W | 0       |
|             | M_DETECTION_TOLERANCE | M_DETECTION_TOLERANCE | 3-0   | Sets the detection tolerance.                                                                                                                                                                                              | R/W | 2       |
| 070h - 084h | RSVD                  | RSVD                  | 15-0  | Reserved.                                                                                                                                                                                                                  | R/W | 0       |
| 085h        | RSVD                  | RSVD                  | 15-11 | Reserved.                                                                                                                                                                                                                  | R/W | 0       |
|             | LOCK_NOISE_IMM_INCR   | LOCK_NOISE_IMM_INCR   | 10    | Enables extra noise-immunity on SMPTE detected lock when HIGH by forcing detection of three TRS words with the last two TRS words having the same alignment before locking to SMPTE. Enable this only for AUTO/MAN = HIGH. | R/W | 0       |
|             | RSVD                  | RSVD                  | 9-0   | Reserved.                                                                                                                                                                                                                  | R/W | 0       |

**Table 4-18: ANC Extraction FIFO Access Registers**

| Address     | Register Name   | Bit  | Description                                                                                                                                                       | R/W | Default |
|-------------|-----------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|
| 800h - BFFh | ANC_PACKET_BANK | 15-0 | Extracted Ancillary Data 91024 words.<br>Bit 15-8: Most Significant Word (MSW).<br>Bit 7-0: Least Significant Word (LSW).<br>See <a href="#">Section 4.18.8</a> . | R   | 0       |

## 4.21 JTAG Test Operation

When the JTAG/ $\overline{\text{HOST}}$  pin of the GS2960A is set HIGH and the  $\overline{\text{SMPTE\_BYPASS}}$  pin is LOW, the host interface port is configured for JTAG test operation. In this mode, pins E7, F8, F7, and E8 become TDO, TCK, TMS, and TDI. In addition, the  $\overline{\text{RESET\_TRST}}$  pin operates as the test reset pin.

Boundary scan testing using the JTAG interface is enabled in this mode.

There are two ways in which JTAG can be used:

1. As a stand-alone JTAG interface to be used in in-circuit ATE (Automatic Test Equipment) during PCB assembly.
2. Under control of a host processor for applications such as system power on self tests.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the digital I/O pins. If the tests are to be applied only at ATE, this can be accomplished with tri-state buffers used in conjunction with the JTAG/ $\overline{\text{HOST}}$  input signal. This is shown in Figure 4-41.

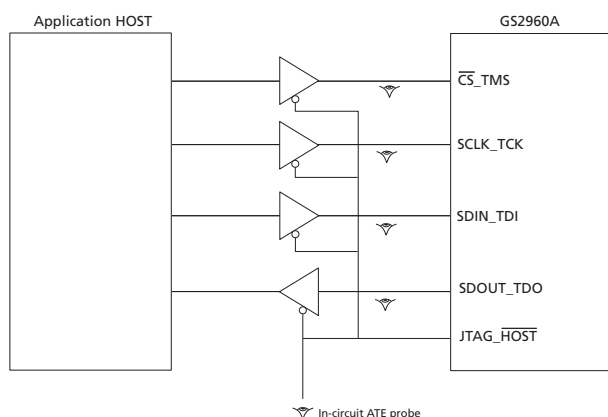


Figure 4-41: In-Circuit JTAG

Alternatively, if the test capabilities are to be used in the system, the host processor may still control the JTAG/ $\overline{\text{HOST}}$  input signal, but some means for tri-stating the host must exist in order to use the interface at ATE. This is represented in Figure 4-42.

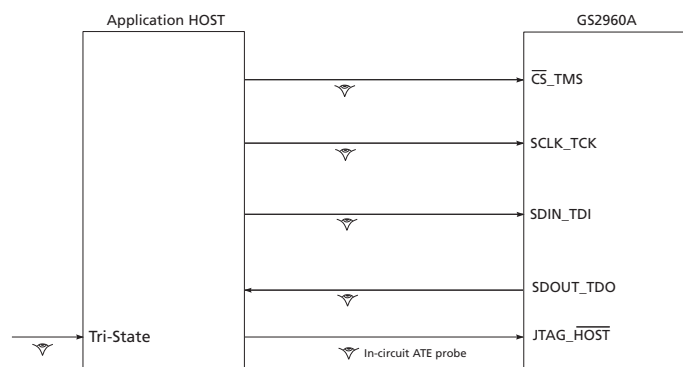


Figure 4-42: System JTAG

Scan coverage is limited to digital pins only. There is no scan coverage for analog pins VCO, SDO/ $\overline{\text{SDO}}$ , RSET, LF, and CP\_RES.

The JTAG/ $\overline{\text{HOST}}$  pin must be held LOW during scan and therefore has no scan coverage.

Please contact your Semtech representative to obtain the BSDL model for the GS2960A.

## 4.22 Device Power-up

Because the GS2960A is designed to operate in a multi-voltage environment, any power-up sequence is allowed. The charge pump, phase detector, core logic, serial digital output and I/O buffers can all be powered up in any order.

NOTE: Power ramp-up time (10% to 90%)  $\geq 40\mu\text{s}$ .

## 4.23 Device Reset

NOTE: At power-up, the device must be reset to operate correctly.

In order to initialize all internal operating conditions to their default states, hold the  $\overline{\text{RESET\_TRST}}$  signal LOW for a minimum of  $t_{\text{reset}} = 1\text{ms}$  after all power supplies are stable. There are no requirements for power supply sequencing.

When held in reset, all device outputs are driven to a high-impedance state.

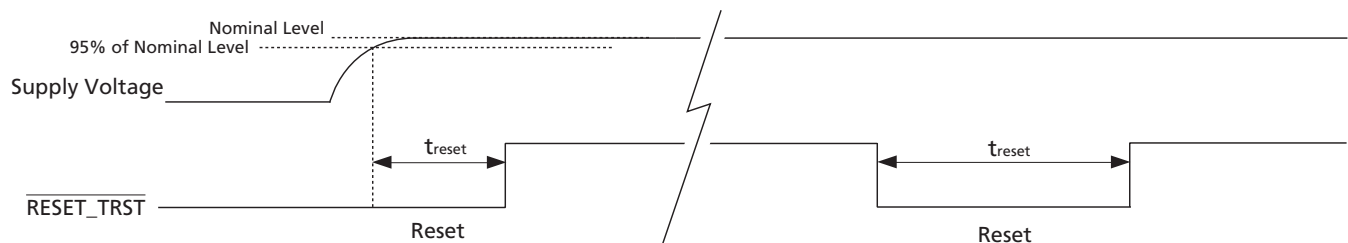


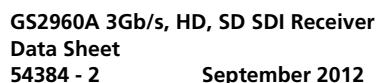
Figure 4-43: Reset Pulse

## 4.24 Standby Mode

The STANDBY pin reduces power to a minimum by disabling all circuits except for the register configuration. Upon removal of the signal to the STANDBY pin, the device returns to its previous operating condition within 1 second, without requiring input from the host interface.

NOTE: In standby mode or reset, the crystal buffer output remains enabled. This allows users to reset the GS2960A device without resetting other downstream devices that are using the same reference. This also allows users to put the GS2960A device in standby mode and still use the loop-through mode.

## 5.1 Typical Application Circuit

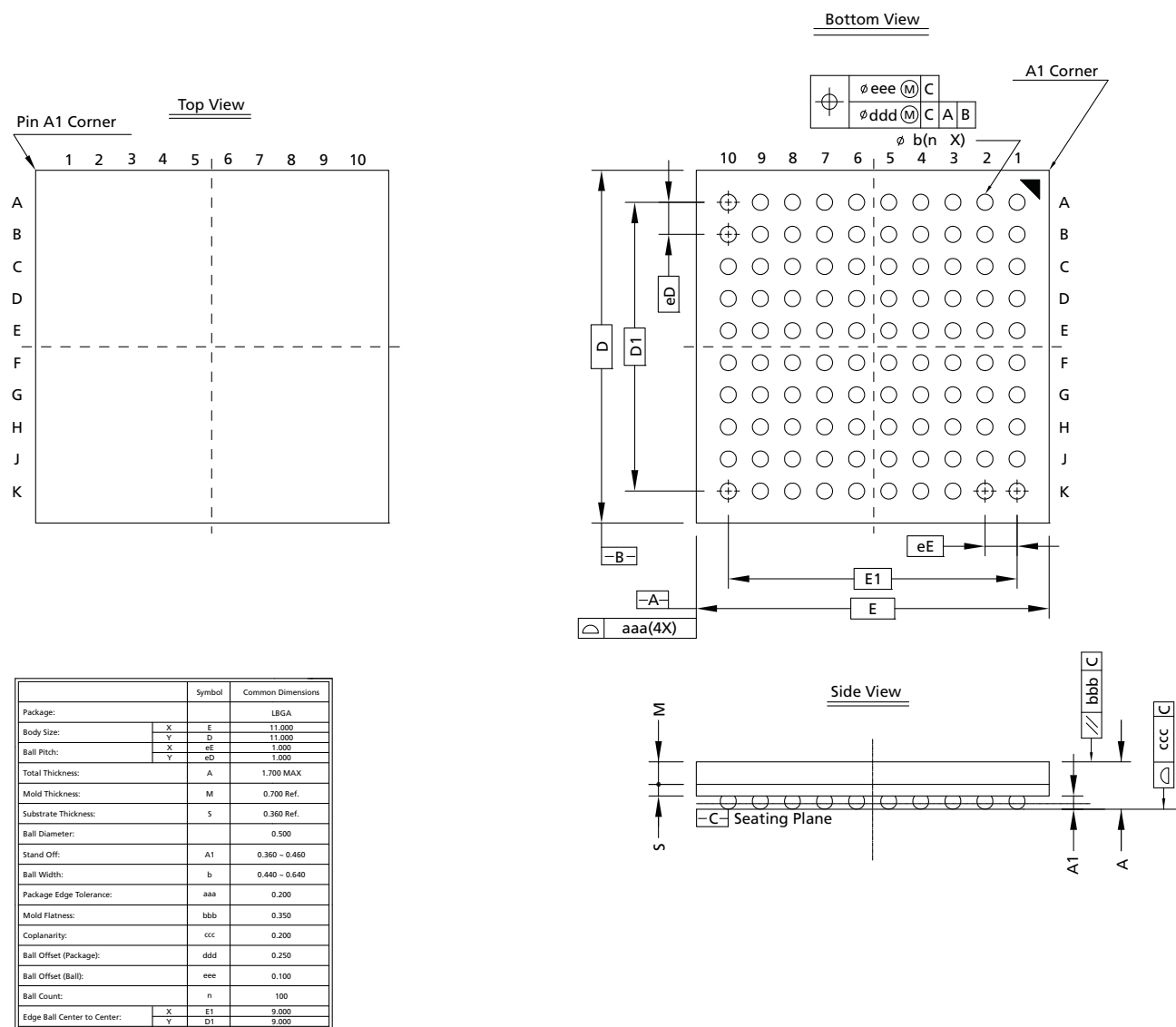


## 6. References & Relevant Standards

|             |                                                                                                     |
|-------------|-----------------------------------------------------------------------------------------------------|
| SMPTE 125M  | Component video signal 4:2:2 – bit parallel interface                                               |
| SMPTE 259M  | 10-bit 4:2:2 Component and 4fsc Composite Digital Signals - Serial Digital Interface                |
| SMPTE 260M  | 1125 / 60 high definition production system – digital representation and bit parallel interface     |
| SMPTE 267M  | Bit parallel digital interface – component video signal 4:2:2 16 x 9 aspect ratio                   |
| SMPTE 274M  | 1920 x 1080 scanning analog and parallel digital interfaces for multiple picture rates              |
| SMPTE 291M  | Ancillary Data Packet and Space Formatting                                                          |
| SMPTE 292   | Bit-Serial Digital Interface for High-Definition Television Systems                                 |
| SMPTE 293M  | 720 x 483 active line at 59.94Hz progressive scan production – digital representation               |
| SMPTE 296M  | 1280 x 720 scanning, analog and digital representation and analog interface                         |
| SMPTE 352M  | Video Payload Identification for Digital Television Interfaces                                      |
| SMPTE 424M  | Television - 3Gb/s Signal/Data Serial Interface                                                     |
| SMPTE 425M  | Television - 3Gb/s Signal/Data Serial Interface - Source Image Format Mapping                       |
| SMPTE RP165 | Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television |
| SMPTE RP168 | Definition of Vertical Interval Switching Point for Synchronous Video Switching                     |

# 7. Package & Ordering Information

## 7.1 Package Dimensions



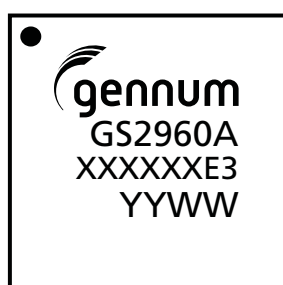
## 7.2 Packaging Data

Table 7-1: Packaging Data

| Parameter                                                            | Value                                                                                  |
|----------------------------------------------------------------------|----------------------------------------------------------------------------------------|
| Package Type                                                         | 11mm x 11mm 100-ball LBGA                                                              |
| Package Drawing Reference                                            | JEDEC M0192 (with exceptions noted in <a href="#">Package Dimensions on page 96</a> ). |
| Moisture Sensitivity Level                                           | 3                                                                                      |
| Junction to Case Thermal Resistance, $\theta_{j-c}$                  | 15.4°C/W                                                                               |
| Junction to Air Thermal Resistance, $\theta_{j-a}$ (at zero airflow) | 37.1°C/W                                                                               |
| Junction to Board Thermal Resistance, $\theta_{j-b}$                 | 26.4°C/W                                                                               |
| Psi, $\psi$                                                          | 0.4°C/W                                                                                |
| Pb-free and RoHS Compliant                                           | Yes                                                                                    |

## 7.3 Marking Diagram

Pin 1  
Indicator



XXXXXX - Last 6 digits (excluding decimal) of  
SAP Batch Assembly (FIN) as listed  
on Packing Slip  
E3 - Pb-free & Green indicator  
YYWW - Date Code

## 7.4 Solder Reflow Profiles

The GS2960A is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 7-1.

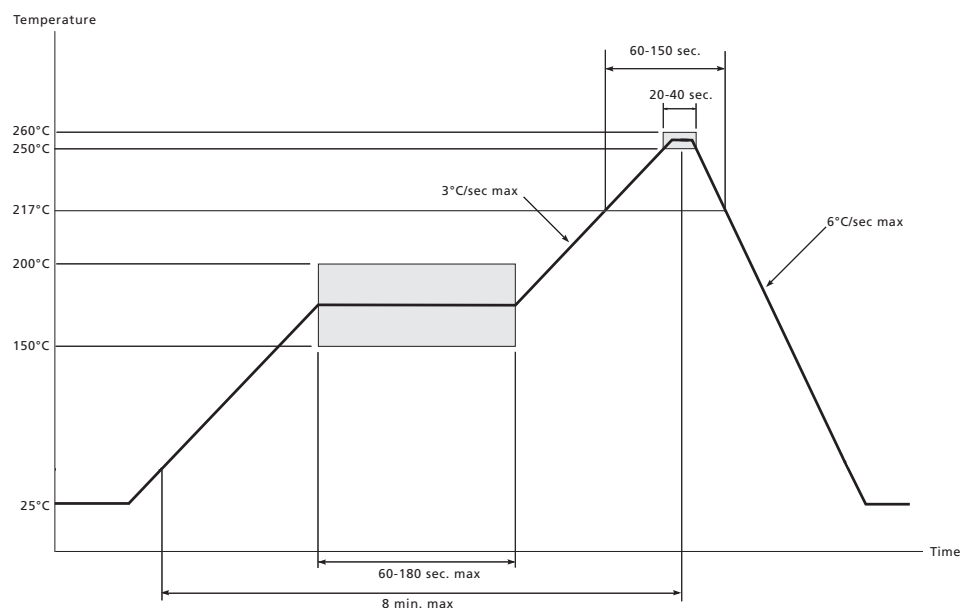


Figure 7-1: Pb-free Solder Reflow Profile

## 7.5 Ordering Information

| Part Number  | Package                             | Pb-free | Temperature Range |
|--------------|-------------------------------------|---------|-------------------|
| GS2960AIB E3 | 100-ball BGA                        | Yes     | -20°C to 85°C     |
| GS2960AIBTE3 | 100-ball BGA<br>(250pc tape & reel) | Yes     | -20°C to 85°C     |

## Revision History

| Version | ECR    | PCN | Date           | Changes and/or Modifications                                                                                                                                                                                             |
|---------|--------|-----|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2       | 158468 | –   | September 2012 | Changes throughout the document.                                                                                                                                                                                         |
| 1       | 155217 | –   | October 2010   | Change pin D7 name to SW_EN in the <a href="#">Functional Block Diagram</a> and <a href="#">Pin Assignment</a> sections. Corrected <a href="#">Package Dimensions</a> and updated <a href="#">Ordering Information</a> . |
| 0       | 153769 | –   | May 2010       | New document.                                                                                                                                                                                                            |



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