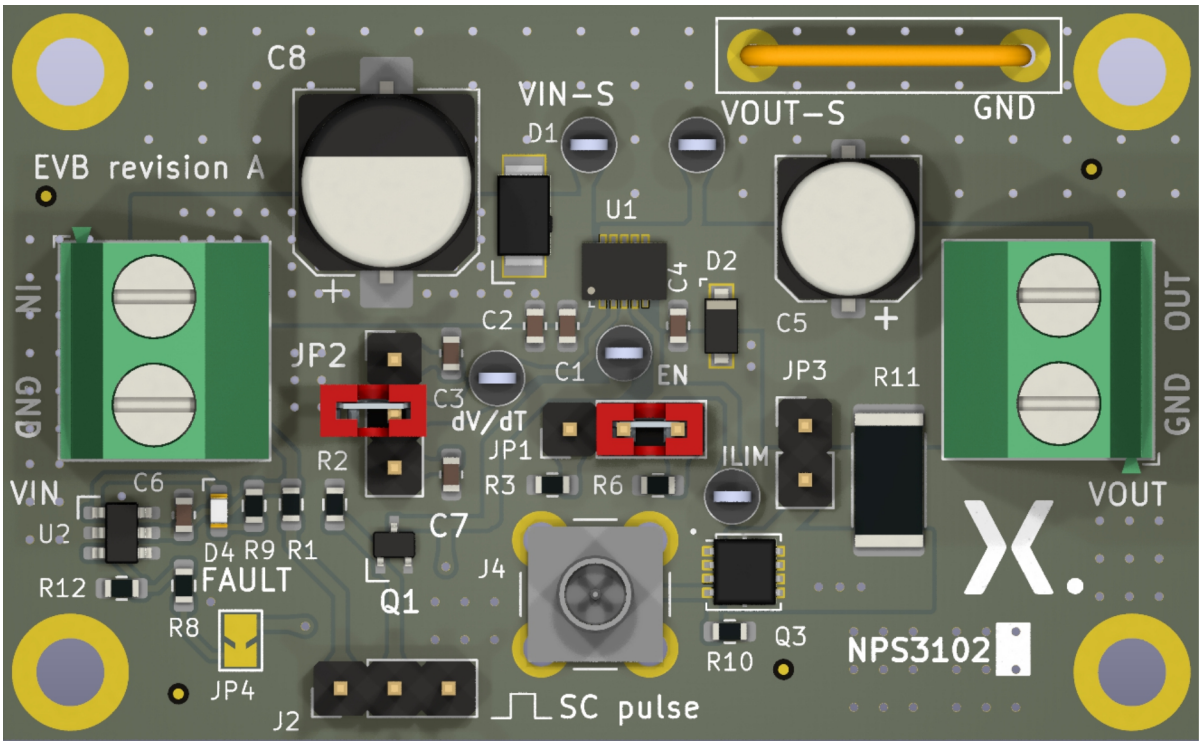
UM90036

Rev. 1 — 18 July 2024

user manual

NPS3102A; NPS3102B 12 V, 2 A-13.5 A, 17 mΩ eFuse evaluation board



Abstract: The NEVB-NPS3102A; NEVB-NPS3102B evaluation board is a 4 layer PCB equipped with either a NPS3102A or NPS3102B electronic fuse. With this evaluation PCB the user can evaluate the performance of the device in several application scenarios.

Keywords: NPS3102A; NPS3102B electronic fuse evaluation board (EVB)

nexperia

1. Introduction

The NPS3102A; NPS3102B is an electronic fuse designed for 12 V systems, featuring an adjustable current clamp, thermal protection, inrush current control, and an internal overvoltage clamp to shield downstream devices from high voltage transients during hot switching.

Two versions are available: Version A latches during faults, requiring a reset afterward, while Version B includes auto-retry circuitry that restarts after fault removal. Each version has a dedicated evaluation board: NEVB-NPS3102A and NEVB-NPS3102B. The eFuses on these boards can be swapped (replacing NPS3102A with NPS3102B or vice versa) to explore differences between latching and auto-retry fuses.

The evaluation PCB contains one eFuse for testing in various scenarios. It integrates an NMOST transistor for short circuit monitoring, comparator circuitry with LED fault indication, selectable output voltage ramp times, and adjustable current limit settings.

2. Features

The following features are available on this evaluation board:

- Two evaluation boards available:
  - NEVB-NPS3102A
  - NEVB-NPS3102B
- Input operating voltage range (V_{IN}): 9 V to 18 V
- Continuous DC load current: 11 A (T_{amb} = 25 °C)
- Selectable current limit
- Selectable output slew rate
- Fault detection indicator
- Short circuit FET
- IN and OUT transient protection diodes
- Open drain enable drive

3. Schematic

Fig. 1 shows the schematic of the NEVB-NPS3102A; NEVB-NPS3102B evaluation board. Explanation of the test pins, jumpers and other features can be found in the next sections.

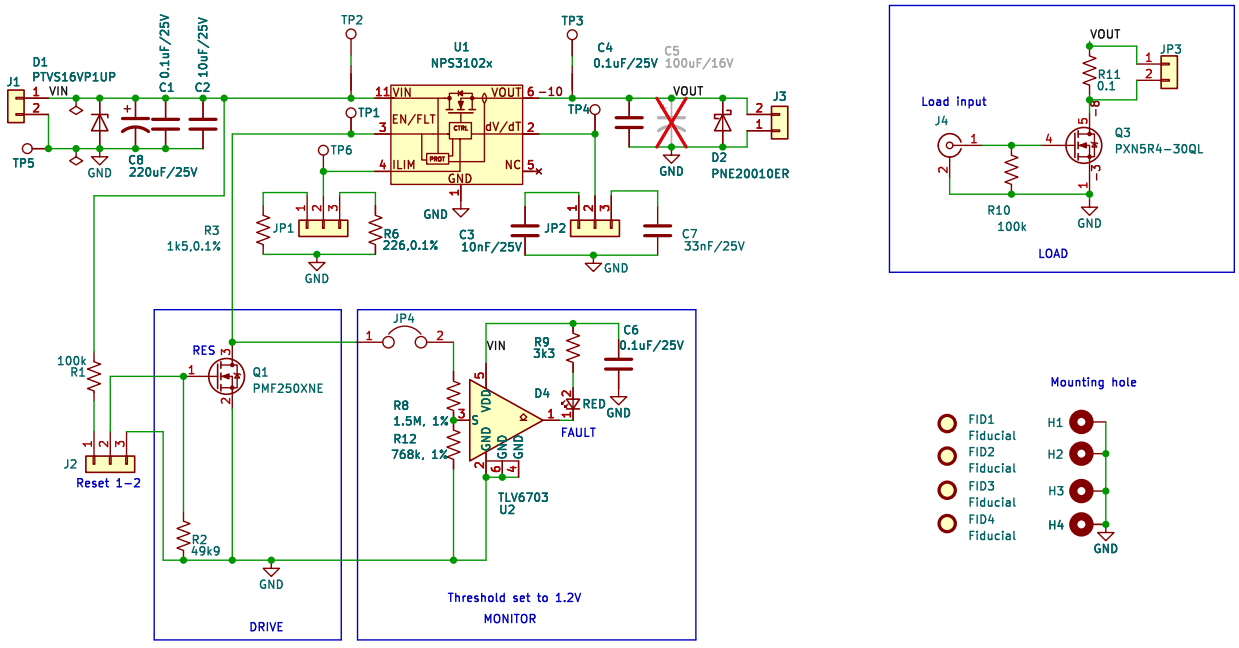


Fig. 1. NPS3102A; NPS3102B EVB schematic

4. PCB layout

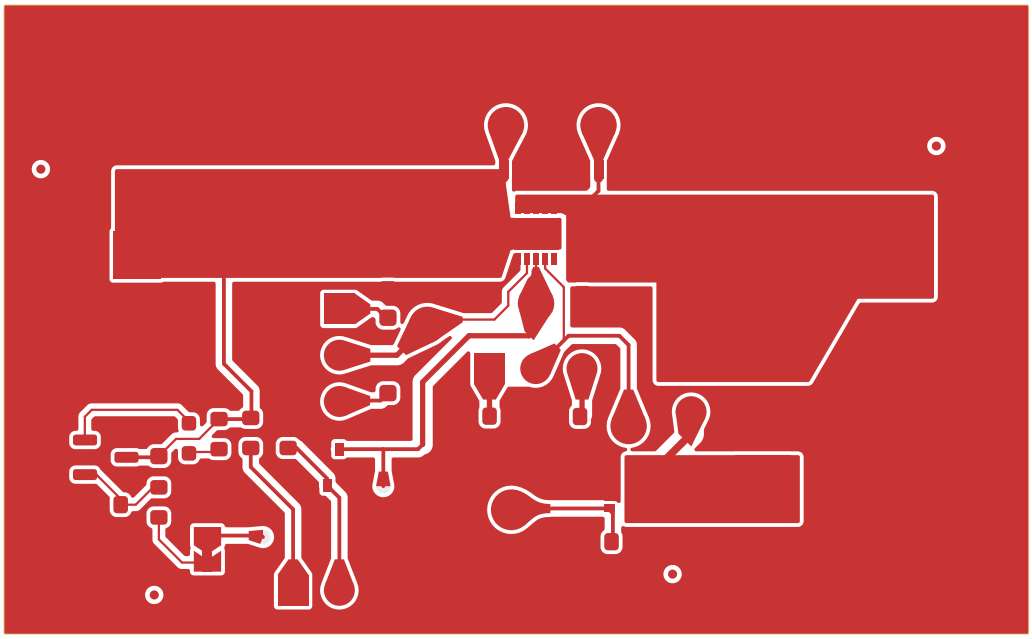


Fig. 2. Top copper layer

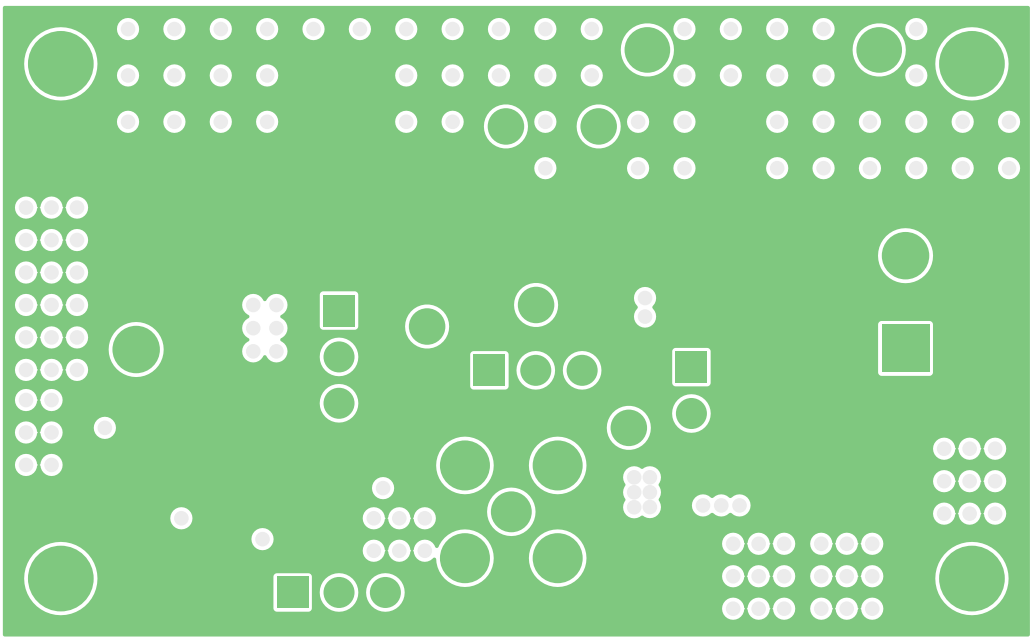


Fig. 3. Inner 1 copper layer

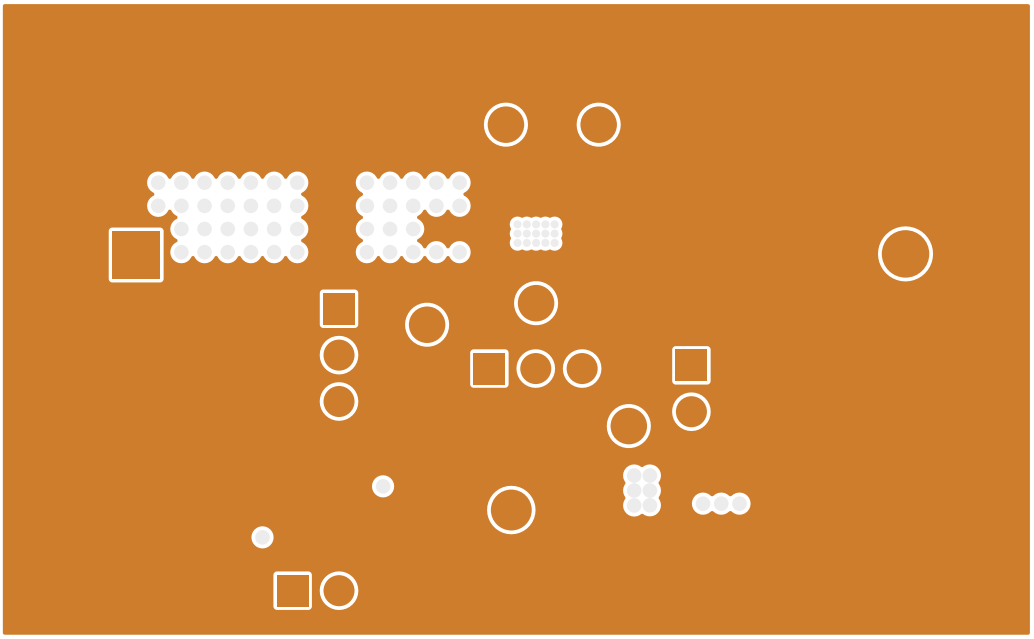


Fig. 4. Inner 2 copper layer

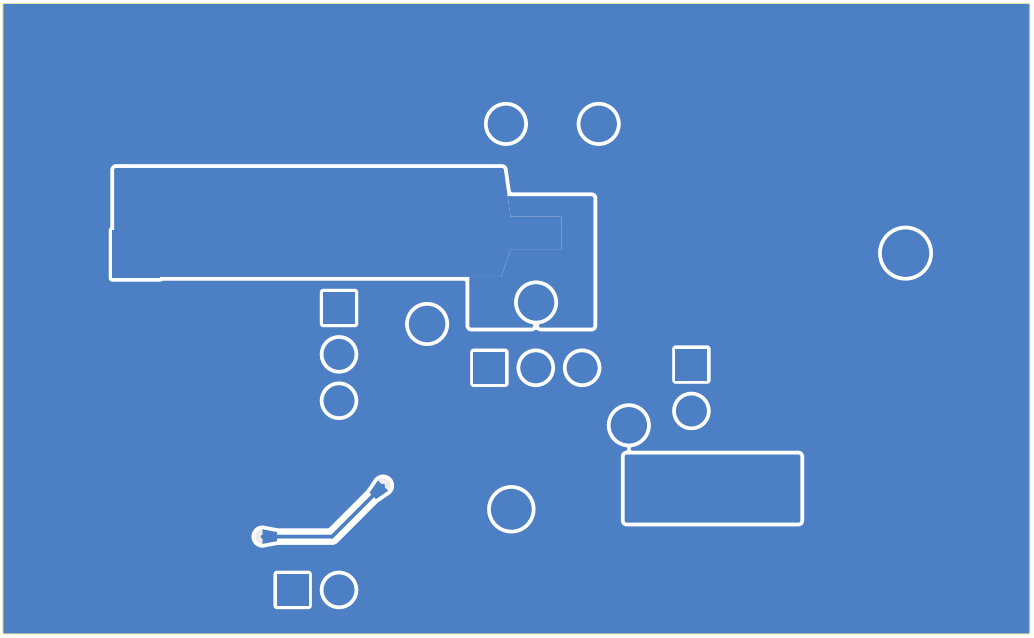


Fig. 5. bottom copper layer

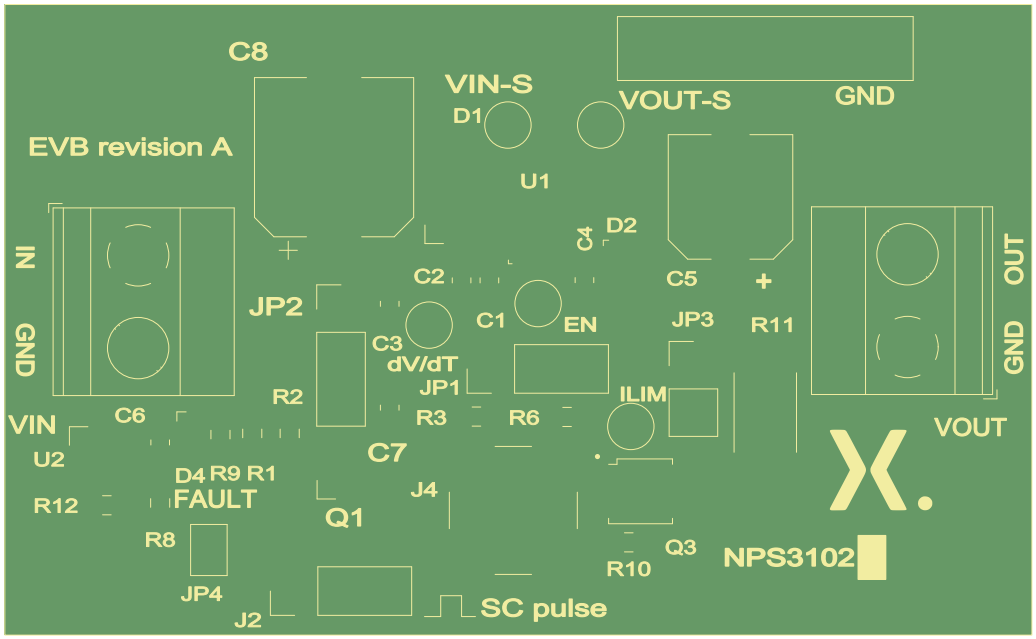


Fig. 6. Component placement top

5. Board stackup

The copper on the printed circuit boards serves as both a conductor and a means to dissipate heat from the exposed pad into the surrounding air. When subjected to high currents and voltage clamping, the device's dissipation can lead to a junction temperature exceeding 125 °C, triggering thermal protection. To achieve low thermal and ground impedance, a 4 layer PCB has been employed. The stackup is illustrated in Fig. 7.

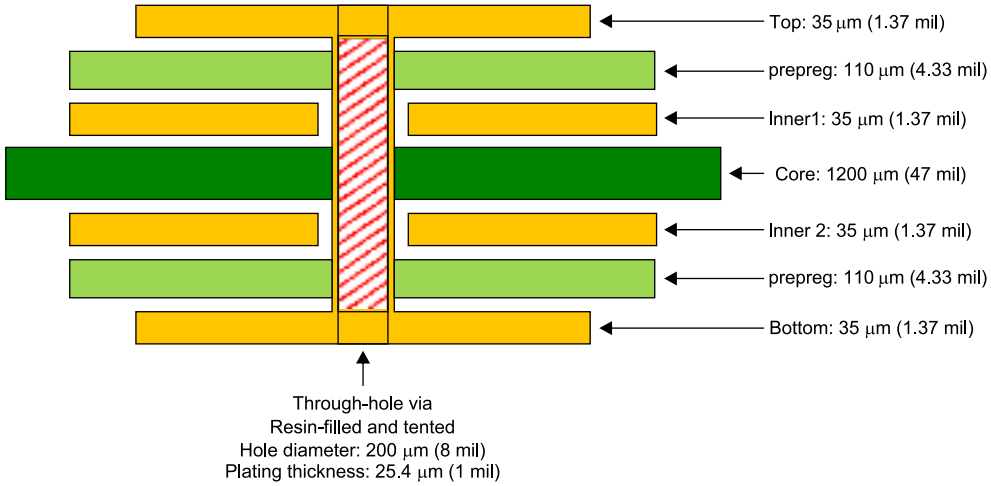


Fig. 7. PCB layer stackup

6. Bill of material

Table 1. Bill of Material (BOM)

Reference	Quantity	Value	Manufacturer name	Manufacturer part number
C1, C4, C6	3	0.1 µF/25 V	KEMET	C0603C104K3RAC7013
C2	1	10 µF/25 V	Murata Electronics	GRM188R61E106MA73D
C3	1	10 nF/25 V	KEMET	C0603C103J3RACTU
C5	1	Not populated	KEMET	EXV107M016A9HAA
C7	1	33 nF/25 V	YAGEO	AC0603JRX7R8BB333
C8	1	220 µF/25 V	Rubycon	25PHV220M8X10.5
D1	1	PTVS16VP1UP	Nexperia	PTVS16VP1UP,115
D2	1	PNE20010ER	Nexperia	PNE20010ERX
D4	1	RED	Kingbright	APHD1608LSURCK
J1, J3	2	Conn_01x02	CUI Devices	TB007-508-02BE
J4	1	Conn_Coaxial	Linx Technologies	CONSMB001-1-G
J2, JP1, JP2	3	Conn_01x03	Wurth Elektronik	61300311121
JP3	1	Dual_testpoint_(2p_header)	SAMTEC	TSW-102-07-L-S
Q1	1	PMF250XNE	Nexperia	PMF250XNEX
Q3	1	PXN5R4-30QL	Nexperia	PXN5R4-30QLJ
R1, R10	2	100k	YAGEO	RT0603FRE10100KL
R2	1	49k9	YAGEO	RT0603FRE0749K9L
R3	1	1k5, 0.1%	YAGEO	RT0603BRD071K5L
R6	1	226, 0.1%	YAGEO	RT0603BRD07226RL
R8	1	1.5 M, 1%	Vishay / Beyschlag	MCT06030C1504FP500
R9	1	3k3	YAGEO	RT0603FRE073K3L
R11	1	0.1	Bourns	CRA2512-FZ-R100ELF
R12	1	768k, 1%	YAGEO	RC0603FR-07768KL
TP1, TP2, TP3, TP4, TP6	2	TestPoint	Keystone Electronics	5001
TP5	1	TestPoint	Keystone Electronics	1430-5
U1	1	NPS3102A or NPS3102B	Nexperia	NPS3102AGB or NPS3102BGB
U2	1	TLV6703	Texas Instruments	TLV6703DDCT
JP1, JP2	2	Jumper Red	Harwin	M7581-46

7. Test setup and operation

Fig. 8 depicts the evaluation board which is initially set up for a maximum device current of 13.5 A and output slew rate configured at 1 ms. Connect the input voltage to J1, and the load circuitry to J3.

To test short circuit behavior, connect a pulse generator with a 5 V amplitude to SMB connector J4. Use JP3 to measure the voltage drop across the 100 mΩ short-circuit resistor. A fault condition will be indicated by LED D4.

Jumper JP2 can be used to change the output slew rate to either 3 ms or 10 ms. The current limit can be changed by means of JP1. Table 3 explains the jumper settings and associated values.

Placing a jumper to J2 pin 1-2 disables the device and resets the latch in case of a NPS3102A. A pulse generator can be connected to J2 pin 2-3 enabling external control of the eFuse.

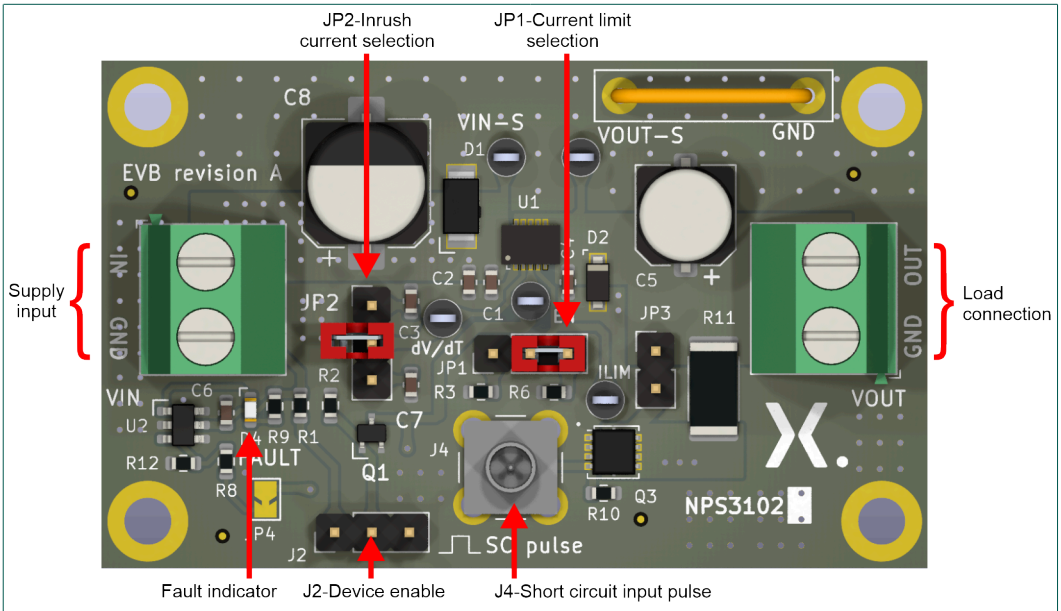


Fig. 8. Evaluation board setup and jumper settings

Table 2. Available test points

Test point	Connected to
TP1	EN/FLT
TP2	VIN-sense
TP3	VOUT-sense
TP4	dV/dt
TP5	Ground
TP6	ILIM

Table 3. Available jumper settings

Jumper	Pin connections		
	1-2	2-3	Open
JP1 – Current Limit	2 A	13.5 A	0 A
JP2 – Inrush Control	3 ms	10 ms	1 ms
J2 – Device Enable	Disable	External drive	Enable

8. Revision history

Table 4. Revision history

Revision number	Date	Description
UM90036 v.1	20240718	Initial version

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