

General Description

The Sanrise SRT04N016L is a low voltage power MOSFET, fabricated using advanced split gate trench technology. The resulting device has extremely low on resistance, low gate charge and fast switching time, making it especially suitable for applications which require superior power density and synchronous rectification.

The SRT04N016L break down voltage is 40V and it has a high rugged avalanche characteristics. The SRT04N016L is available in PDFN5*6 package.

Symbol

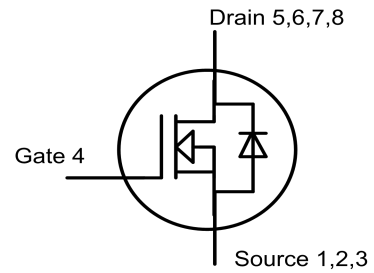


Figure 1 Symbol of SRT04N016L

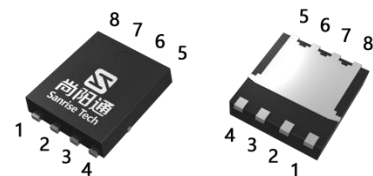
Features

- Ultra Low $R_{DS(ON)_{TYP}} = 1.15m\Omega @ V_{GS} = 10V$.
- Ultra Low Gate Charge, $Q_g = 85nC$ typ.
- Fast switching capability
- Robust design with better EAS performance
- EMI Improved
- Non-automotive Qualified

Application

- Server/Telecom
- High Power Supply
- E-Tools
- BMS

Package Type



PDFN5*6

Figure 2 Package Type of SRT04N016L

Ordering Information

SRT04N016L□□-□		
Circuit Type	□	E: Lead Free
Package	□	G: Green
D56: PDFN5*6	□	Blank: Tube
		TR: Tape & Reel

Package	Part Number	Marking ID	Packing Type
PDFN5*6	SRT04N016LD56TR-G	SRT04N016LD56G	Tape & Reel

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, Silicon	$T_C=25^{\circ}\text{C}$	I_D	173	A
	$T_C=100^{\circ}\text{C}$		109	
	$T_C=125^{\circ}\text{C}$		77	
Pulsed Drain Current (Note 2)		I_{DM}	692	A
Avalanche Energy, Single Pulse (Note 3)		E_{AS}	100	mJ
Avalanche Destructive Energy, Single Pulse (Note 4)		E_{AS_Limit}	756	mJ
Avalanche Energy, Repetitive (Note 2)		E_{AR}	0.2	mJ
Avalanche Current, Repetitive (Note 2)		I_{AR}	50.0	A
Continuous Diode Forward Current		I_S	173	A
Diode Pulse Current		$I_{S,PULSE}$	692	A
Max Power Dissipation		P_D	100	W
Operating Junction Temperature		T_J	150	°C
Storage Temperature		T_{STG}	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)		T_{LEAD}	260	°C

Note:

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. $I_{AS}=20\text{A}$, $V_{DD}=20\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$
4. $I_{AS_Limit}=55\text{A}$, $V_{DD}=20\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$

Thermal Resistance

Parameter		Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	PDFN5*6	R_{thJC}			1.2	°C/W
Thermal Resistance, Junction-to-Ambient	PDFN5*6	R_{thJA}			50	

1.6m Ω , 40V, N-Channel Power MOSFET
SRT04N016L
Electrical Characteristics
 $T_J = 25^\circ\text{C}$, unless otherwise specified.

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics							
Drain-Source Breakdown Voltage		BV _{DSS}	V _{GS} =0V, I _D =250uA	40			V
Zero Gate Voltage Drain Current		I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	uA
Gate-Body Leakage Current	Forward	I _{GSSF}	V _{GS} =20V, V _{DS} =0V			200	nA
	Reverse	I _{GSSR}	V _{GS} =-20V, V _{DS} =0V			-200	
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} =V _{GS} , I _D =0.25mA	1.2	1.8	2.4	V
Static Drain-Source On-Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =50A		1.15	1.6	mΩ
			V _{GS} =4.5V, I _D =50A		2.0	3.05	
Gate Resistance		R _G	f=1MHz, Open Drain		1.3		Ω
Dynamic Characteristics							
Input Capacitance		C _{ISS}	V _{DS} =20V, V _{GS} =0V, f=1MHz		5.8		nF
Output Capacitance		C _{OSS}			1.6		nF
Reverse Transfer Capacitance		C _{RSS}			98		pF
Effective output capacitance, energy related ^{NOTE5}		C _{O(er)}	V _{GS} =0V, V _{DS} =0...32V		2.4		nF
Effective output capacitance, time related ^{NOTE6}		C _{O(tr)}			3.0		
Turn-on Delay Time		t _{d(on)}	V _{DD} =20V, I _D =50A R _G =1.6Ω, V _{GS} =10V		18		ns
Rise Time		t _r			55		
Turn-off Delay Time		t _{d(off)}			60		
Fall Time		t _f			12		
Gate Charge Characteristics							
Gate to Source Charge		Q _{gs}	V _{DD} =20V, I _D =50A V _{GS} =0 to 10V		12.5		nC
Gate to Drain Charge		Q _{gd}			9.5		
Gate Charge Total		Q _g			85		
Gate Plateau Voltage		V _{plateau}			2.3		V
Gate Charge Total, sync FET		Q _g	V _{DD} =0.1V, V _{GS} =0 to 10V		79		nC
Reverse Diode Characteristics							
Drain-Source Diode Forward Voltage		V _{SD}	V _{GS} =0V, I _{SD} =50A		0.84	1.0	V
Reverse Recovery Time		t _{rr}	V _R =20V, I _F =50A dI _F /dt=100A/us		60		ns
Reverse Recovery Charge		Q _{rr}			120		nC
Peak Reverse Recovery Current		I _{rrm}			4.0		A

Note:

- $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 32V
- $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 32V

Typical Performance Characteristics

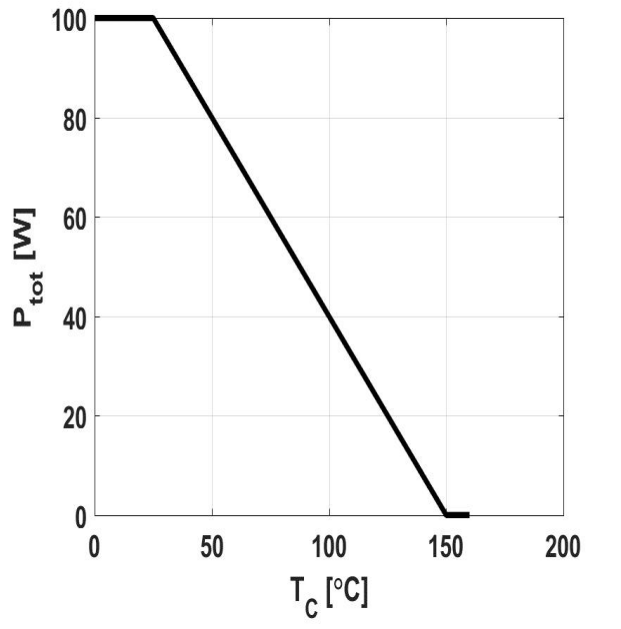
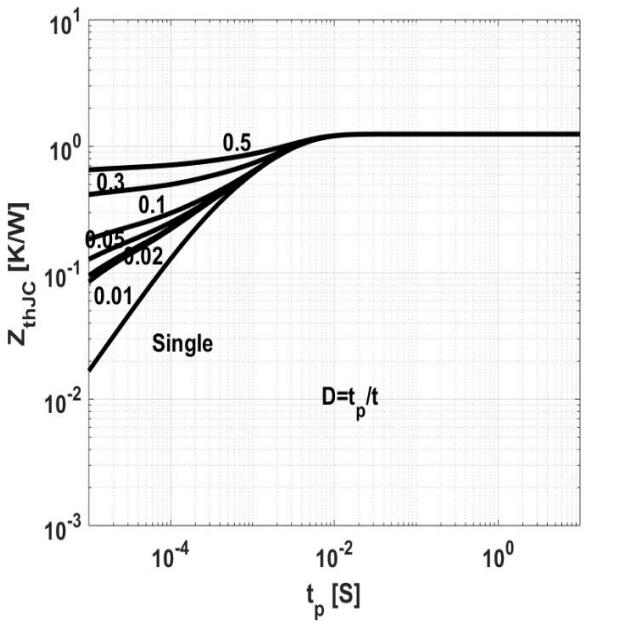
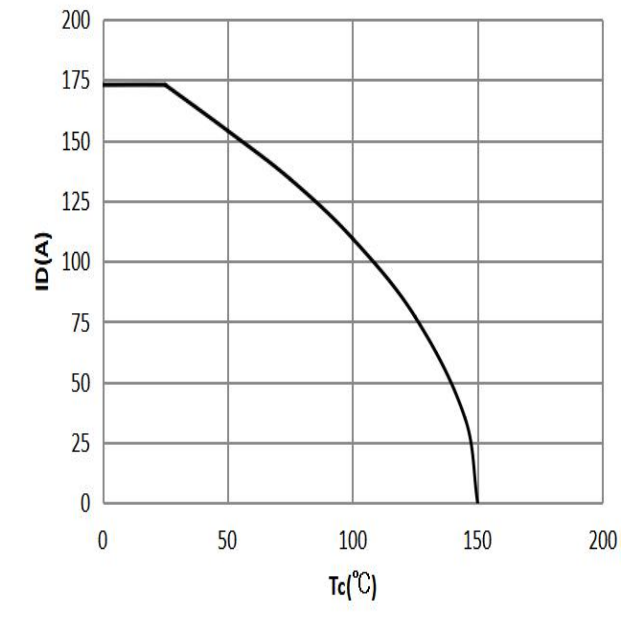
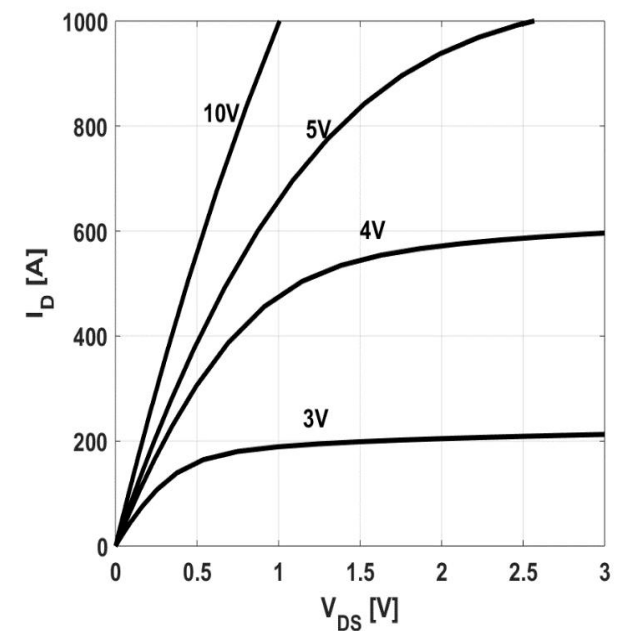
Figure 3: Power Dissipation  $P_{tot}=f(T_c)$	Figure 4: Max. Transient Thermal Impedance  $Z_{(th)JC}=f(t_p)$;parameter:$D=t_p/T$
Figure5: Drain Current  $I_D=f(T_c); V_{GS} \geq 10V$	Figure6: Typ. Output Characteristics  $I_D=f(V_{DS}); T_j=25^{\circ}C$; parameter: V_{GS}

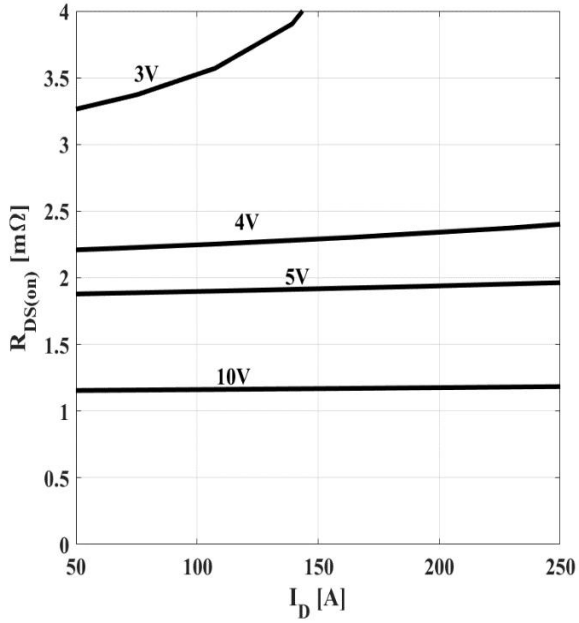
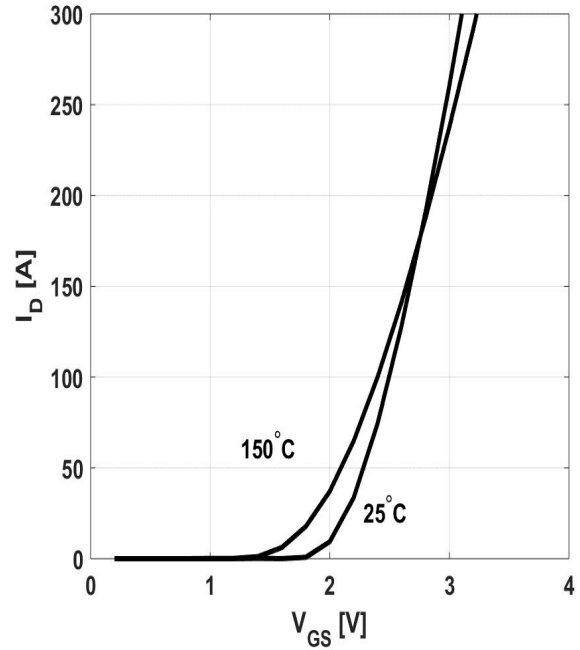
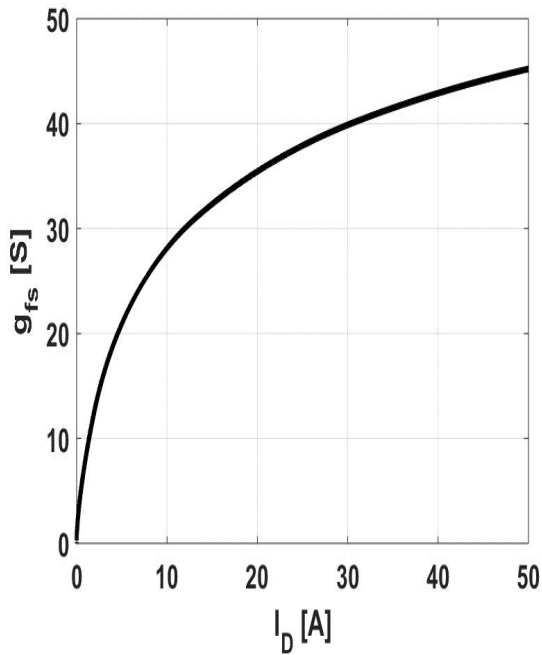
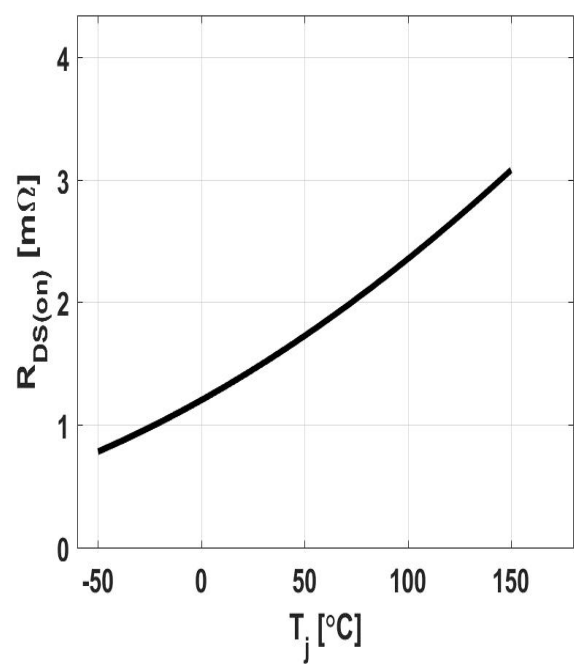
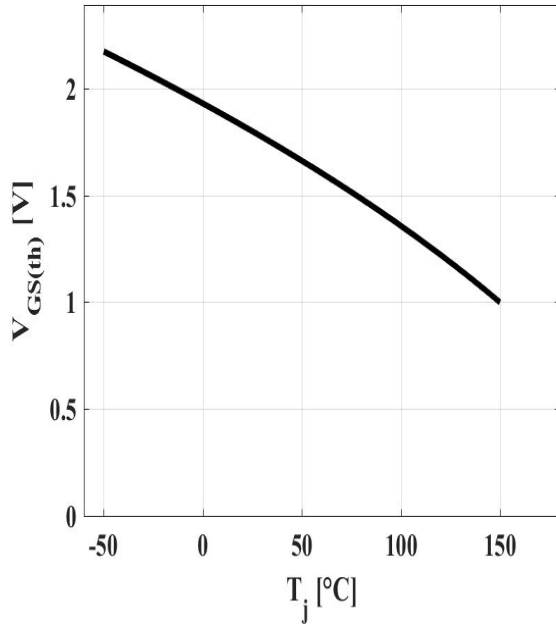
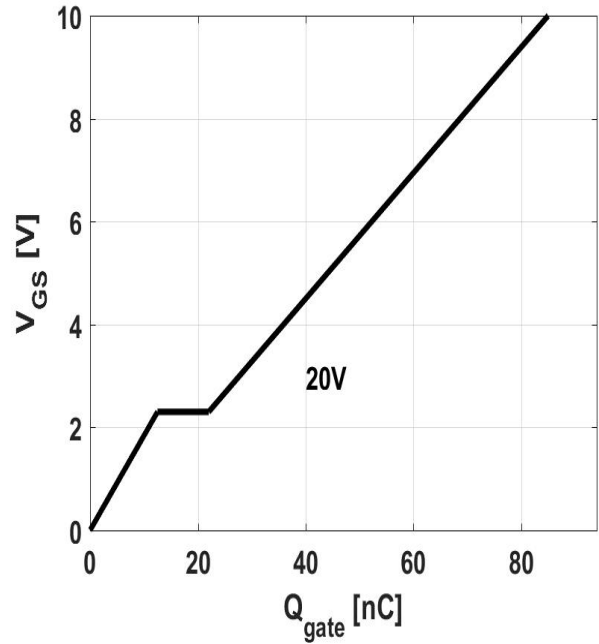
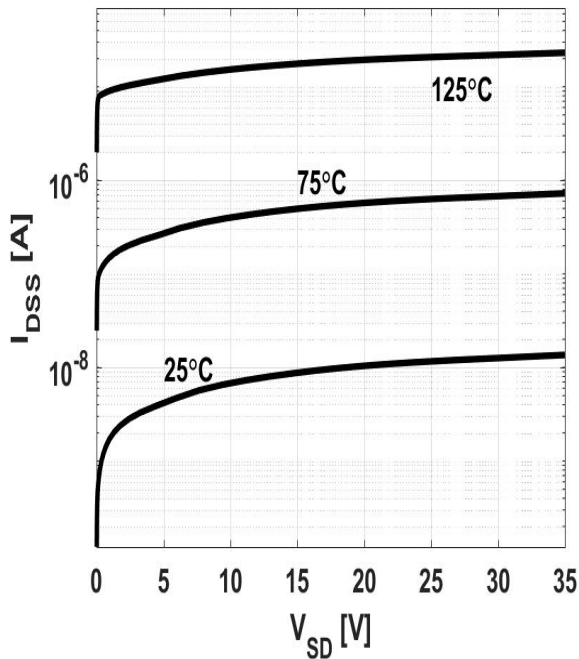
Figure7: Typ. Drain-Source On-State Resistance

 $R_{DS(ON)}=f(I_D); T_j=25^{\circ}C$; parameter: V_{GS}
Figure8: Typ. Transfer Characteristics

 $I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j
Figure9: Typ. Forward Transconductance

 $g_{fs}=f(I_D); T_j=25^{\circ}C$
Figure10: Typ. Drain-Source On-State Resistance

 $R_{DS(ON)}=f(T_j); I_D=50A; V_{GS}=10V$

Figure 11: Typ. Gate Threshold Voltage


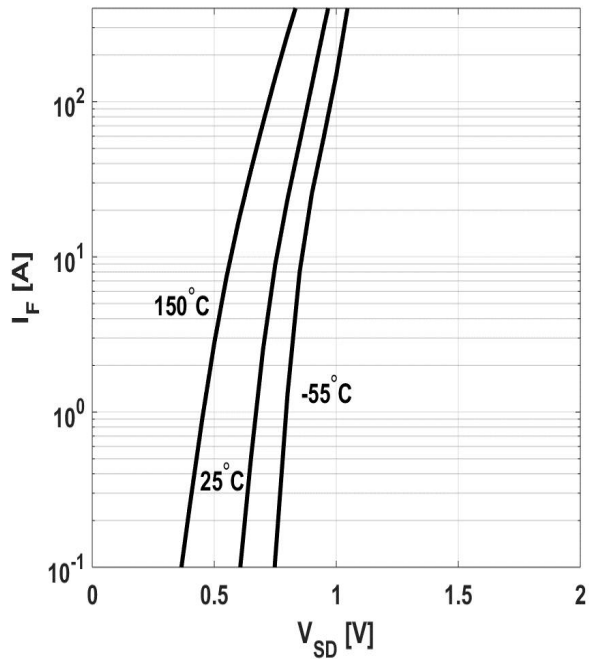
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_{DS} = 250\mu A$$

Figure 12: Typ. Gate Charge


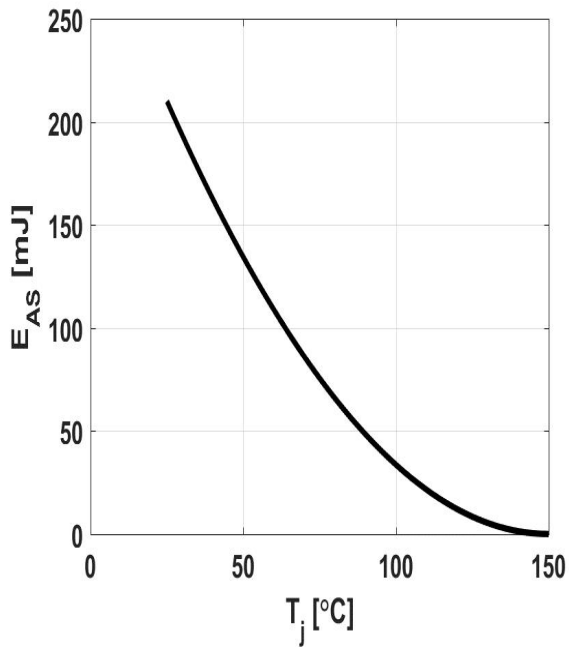
$$V_{GS} = f(Q_{gate}), I_D = 50A \text{ pulsed}$$

Figure 13: Drain-Source Leakage Current


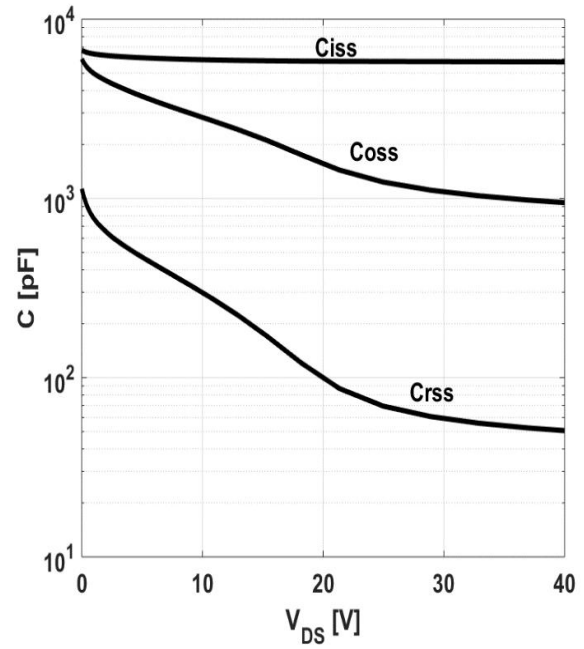
$$I_{DSS} = f(V_{DS}); V_{GS} = 0V; \text{parameter: } T_j$$

Figure 14: Forward Characteristics of Reverse Diode


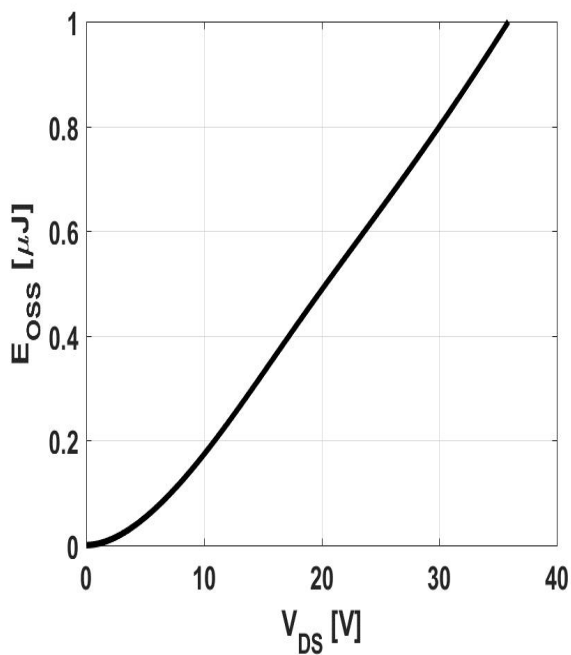
$$I_F = f(V_{SD}); \text{parameter: } T_j$$

Figure 15: Avalanche Energy


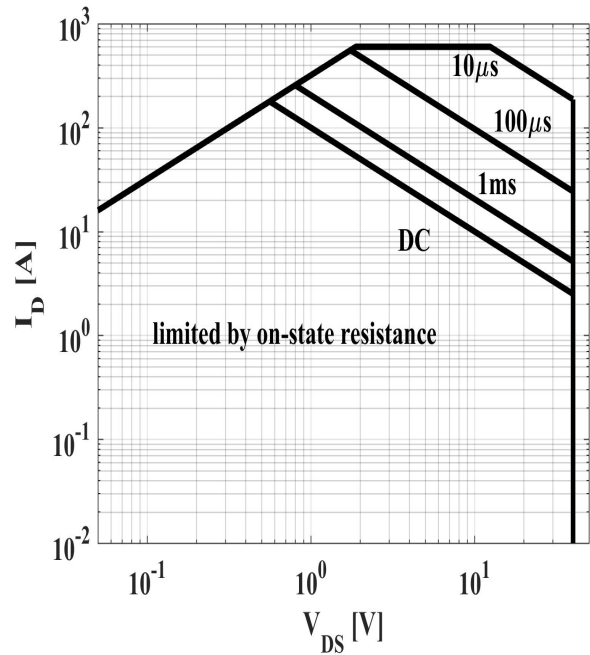
$$E_{AS}=f(T_j); I_D=50.0A; V_{DD}=20V$$

Figure 16: Typ. Capacitances


$$C=f(V_{DS}); V_{GS}=0; f=1MHz$$

Figure 17: Coss Stored Energy


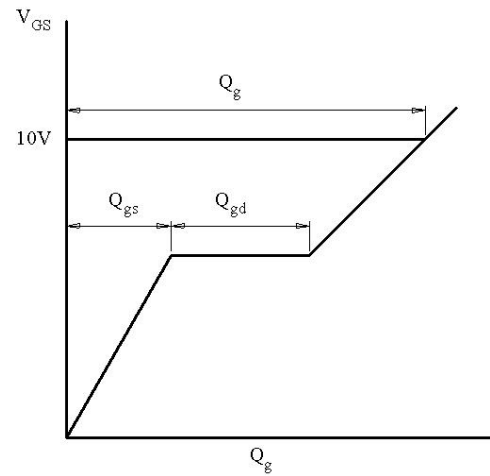
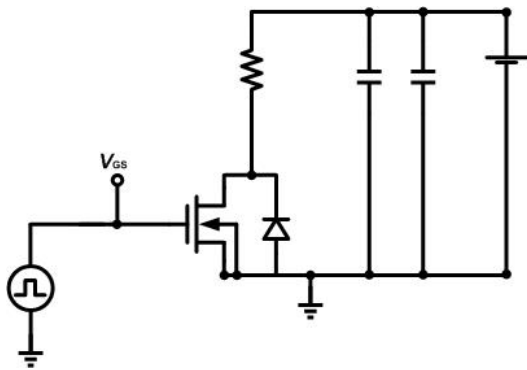
$$E_{OSS}=f(V_{DS})$$

Figure 18: Safe Operating Area


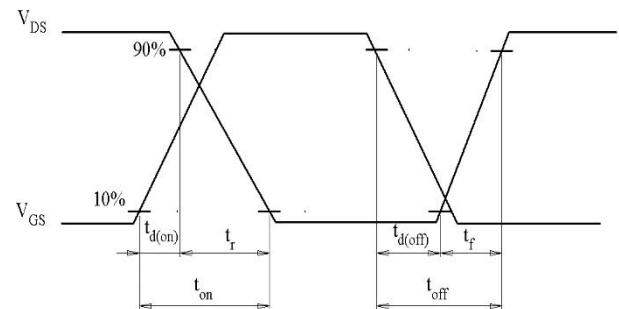
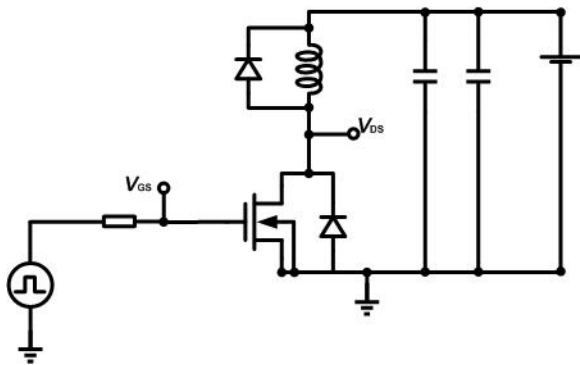
$$I_D = f(V_{DS}); T_c = 25^\circ C; V_{GS} > 7V; \text{parameter } t_p$$

Test Circuits

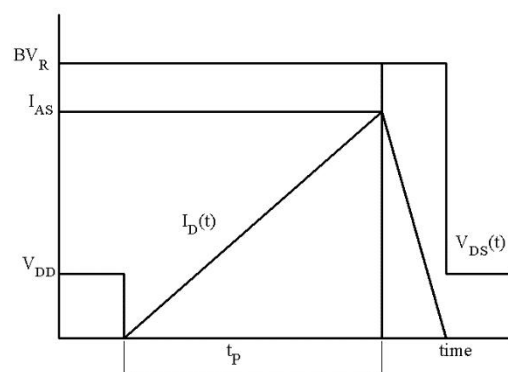
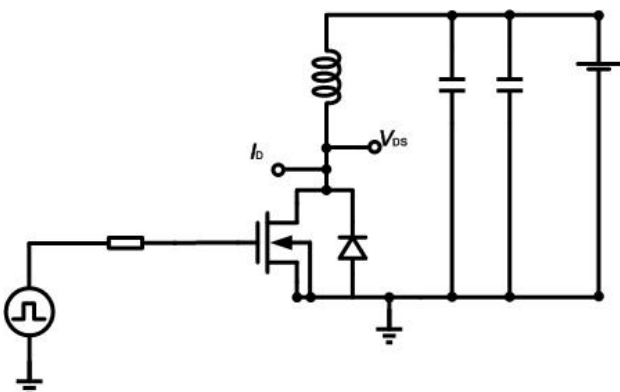
1. Gate Charge Test Circuit & Waveform



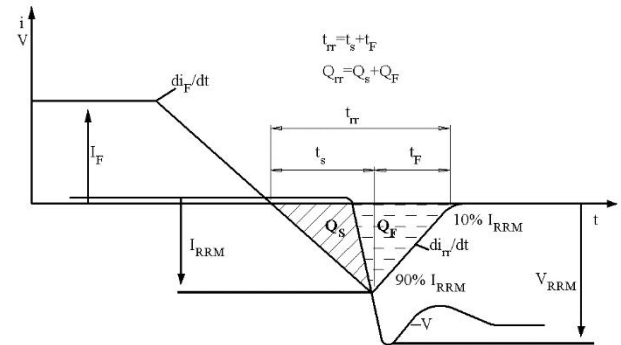
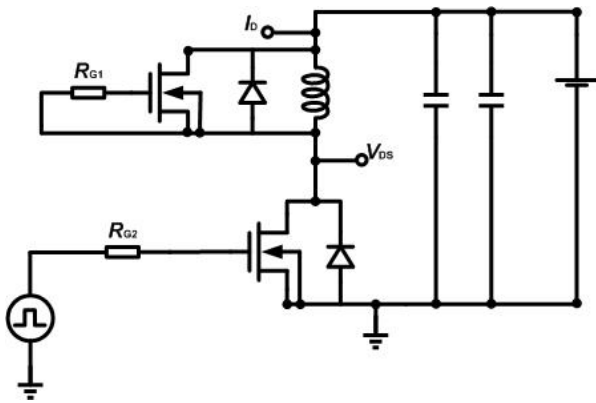
2. Switch Time Test Circuit

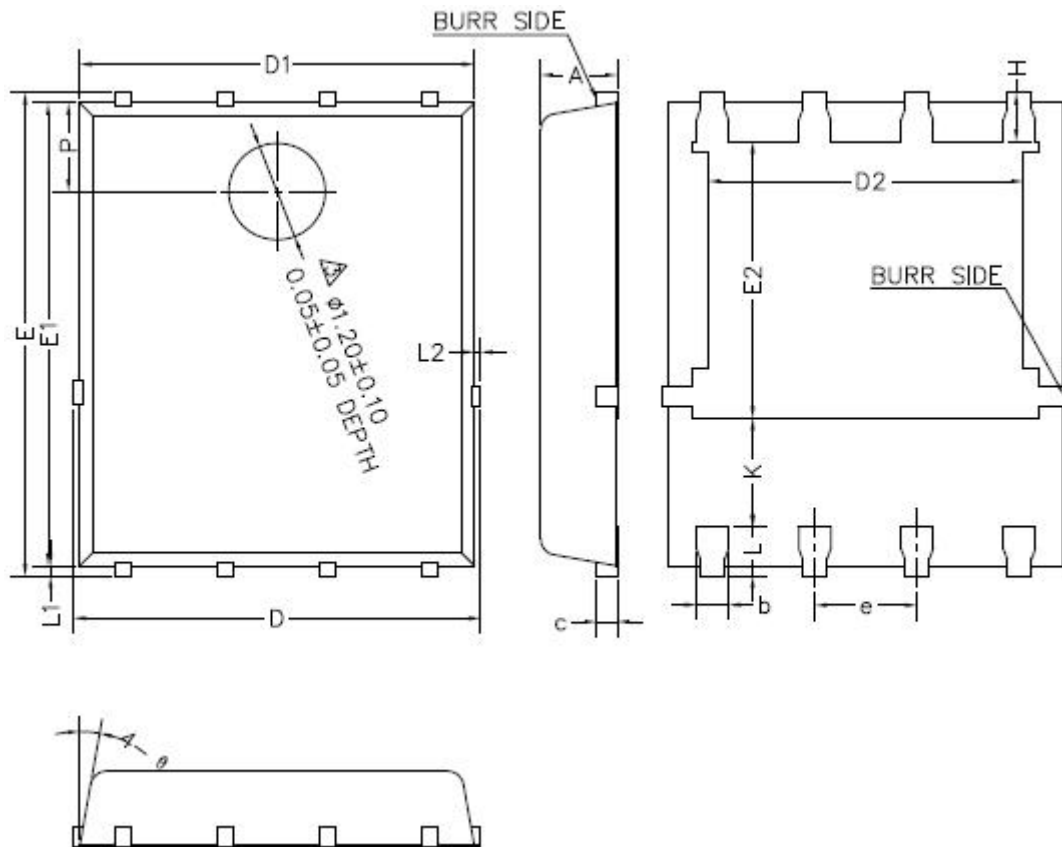


3. Unclamped Inductive Switching Test Circuit & Waveforms



4. Test Circuit and Waveform for Diode Characteristics



Mechanical Dimensions
PDFN5*6-8
Unit: mm


Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A	0.90	1.10	1.20
b	0.35	0.40	0.45
c	0.21	0.25	0.34
D			5.10
D1	4.80	4.90	5.00
D2	3.91	4.01	4.11
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.34	3.44	3.54
H	0.51	0.61	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°



Sanrise Technology Limited Company

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