

Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	850	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	2.7
Q_g (Max.) (nC)	78	
Q_{gs} (nC)	9.6	
Q_{gd} (nC)	45	
Configuration	Single	

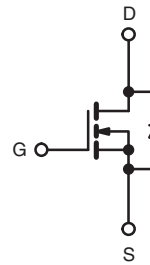
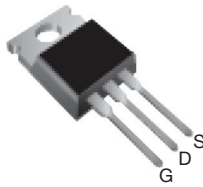
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



RoHS*
 COMPLIANT
 HALOGEN
FREE
 Available

TO-220AB



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	850	V
Gate-Source Voltage			V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	4.1	A
		T _C = 100 °C		2.6	
Pulsed Drain Current ^a			I _{DM}	16	
Linear Derating Factor				1.0	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	260	mJ
Avalanche Current ^a			I _{AR}	4.1	A
Repetitive Avalanche Energy ^a			E _{AR}	13	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	125	W
Peak Diode Recovery dV/dt ^c			dV/dt	2.0	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 29\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 4.1\text{ A}$ (see fig. 12).
- $I_{SD} \leq 4.1\text{ A}$, $dI/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq 600\text{ V}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	-	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		850	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.90	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 800 V, V _{GS} = 0 V		-	-	100	μA
		V _{DS} = 640 V, V _{GS} = 0 V, T _J = 125 °C		-	-	500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 2.5 A ^b	-	2.7	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 100 V, I _D = 2.5 A		2.5	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1300	-	pF
Output Capacitance	C _{oss}			-	310	-	
Reverse Transfer Capacitance	C _{rss}			-	190	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 4.1 A, V _{DS} = 400 V, see fig. 6 and 13 ^b	-	-	78	nC
Gate-Source Charge	Q _{gs}			-	-	9.6	
Gate-Drain Charge	Q _{gd}			-	-	45	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 400 V, I _D = 4.1 A, R _g = 12 Ω, R _D = 95 Ω, see fig. 10 ^b		-	12	-	ns
Rise Time	t _r			-	33	-	
Turn-Off Delay Time	t _{d(off)}			-	82	-	
Fall Time	t _f			-	30	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	4.1	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	16	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 4.1 A, V _{GS} = 0 V ^b		-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 4.1 A, dI/dt = 100 A/μs ^b		-	480	720	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	1.8	2.7	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

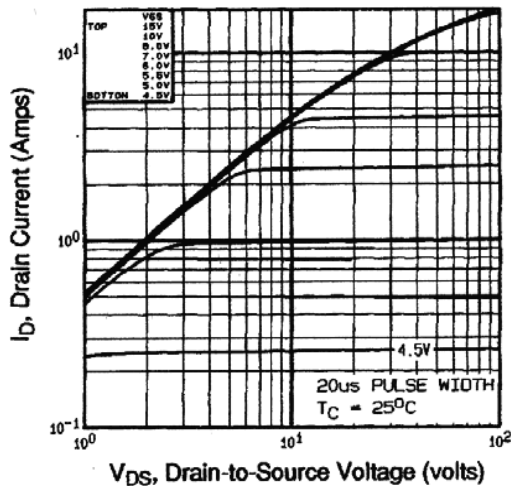


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$

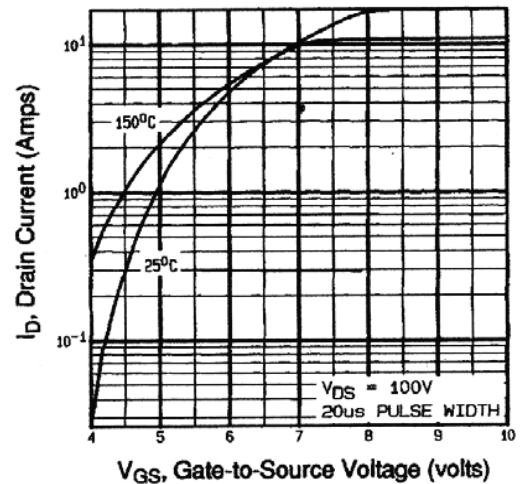


Fig. 3 - Typical Transfer Characteristics

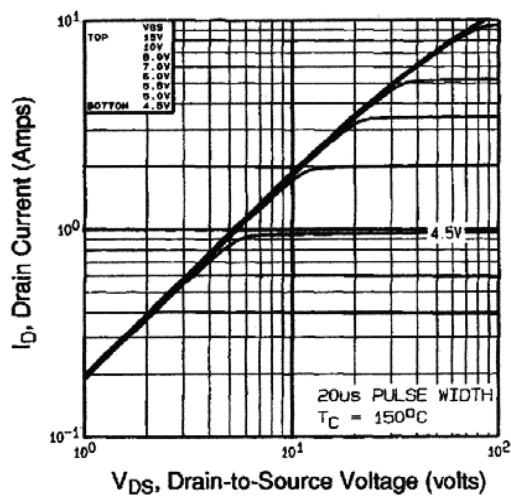


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^{\circ}\text{C}$

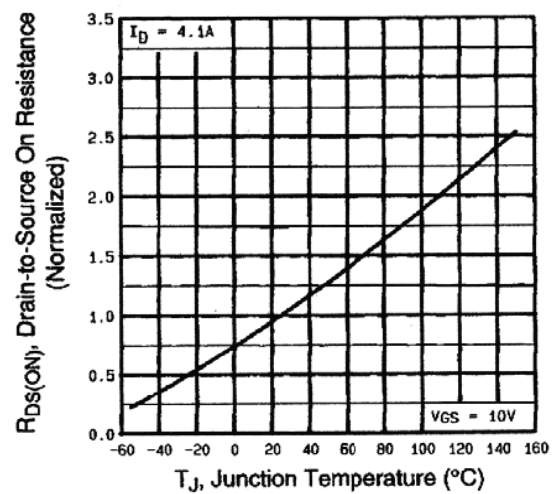


Fig. 4 - Normalized On-Resistance vs. Temperature

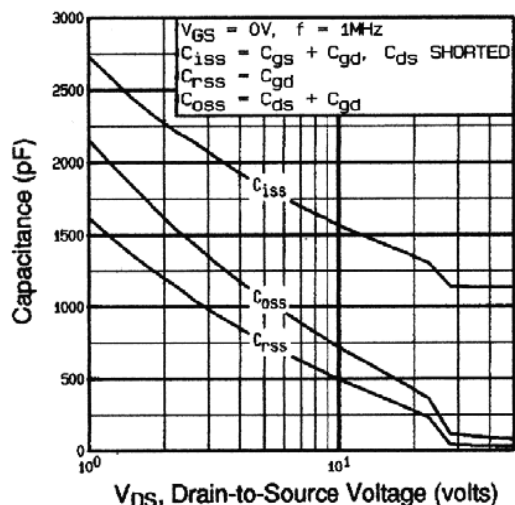


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

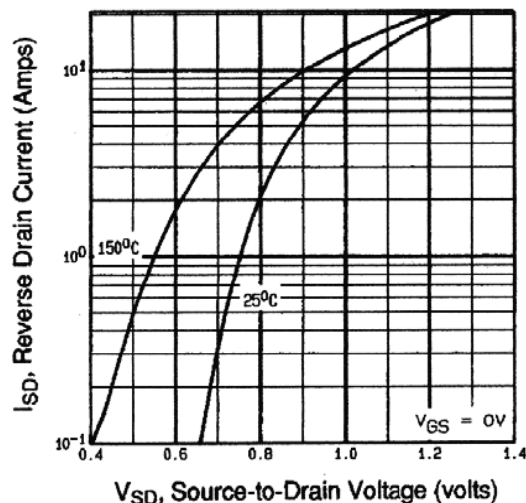


Fig. 7 - Typical Source-Drain Diode Forward Voltage

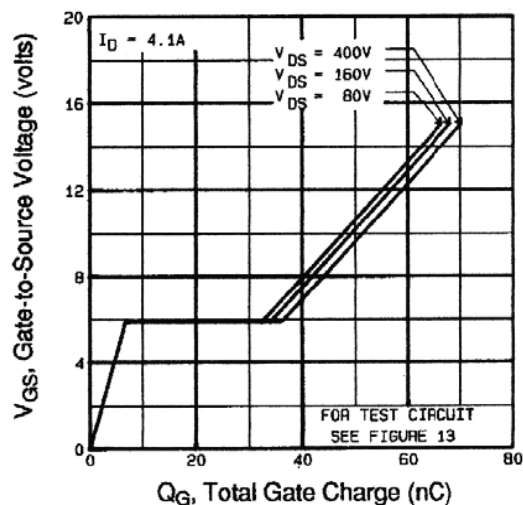


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

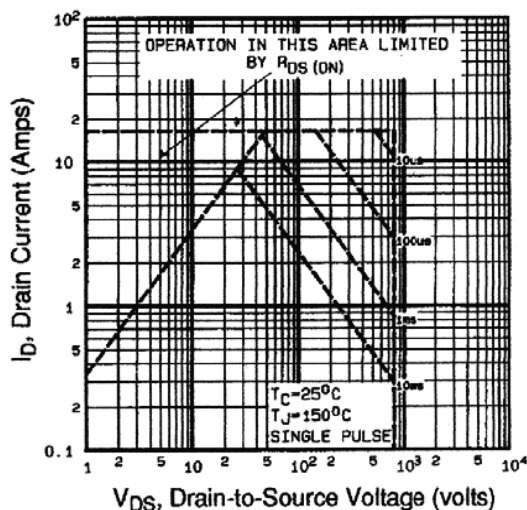


Fig. 8 - Maximum Safe Operating Area

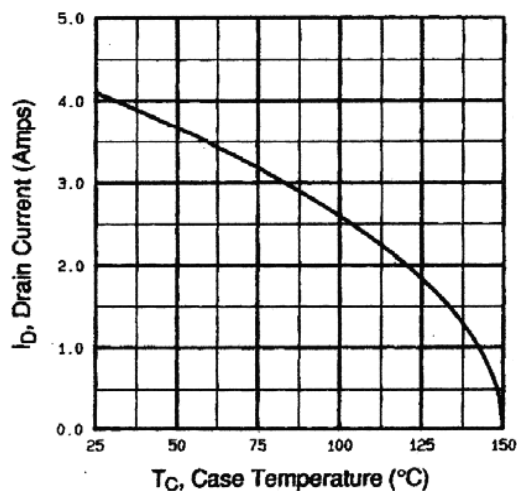


Fig. 9 - Maximum Drain Current vs. Case Temperature

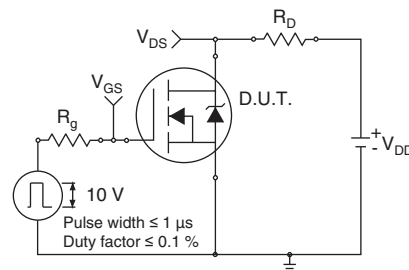


Fig. 10a - Switching Time Test Circuit

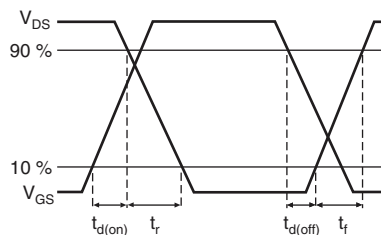


Fig. 10b - Switching Time Waveforms

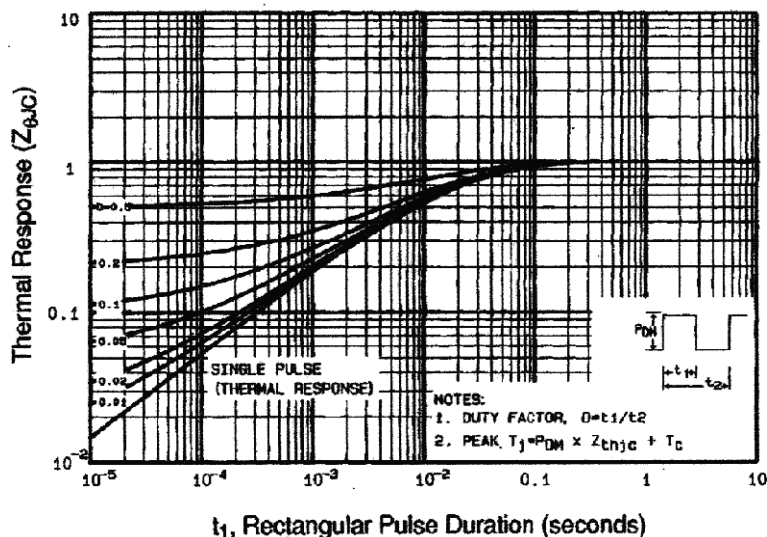


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

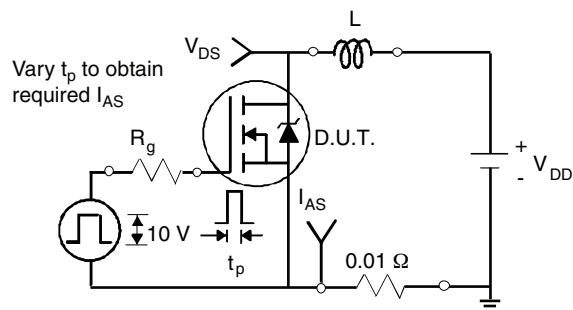


Fig. 12a - Unclamped Inductive Test Circuit

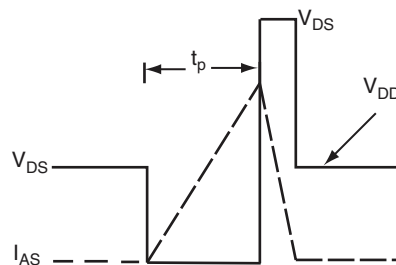


Fig. 12b - Unclamped Inductive Waveforms

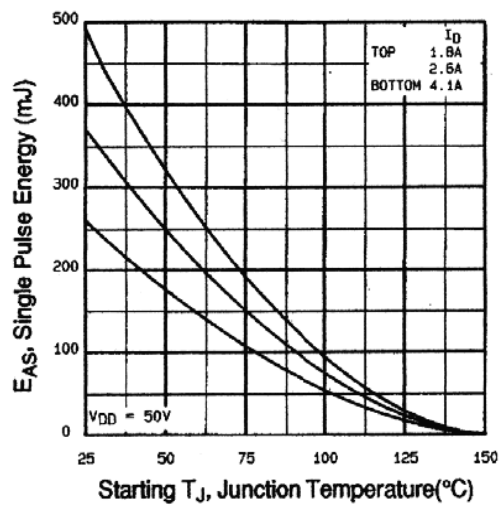


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

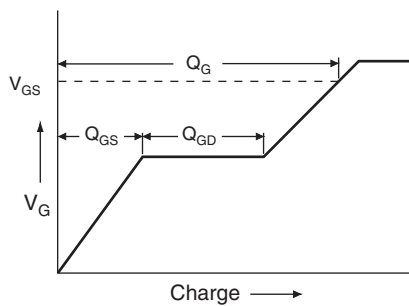


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

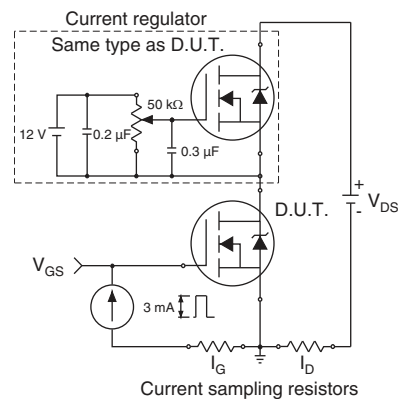
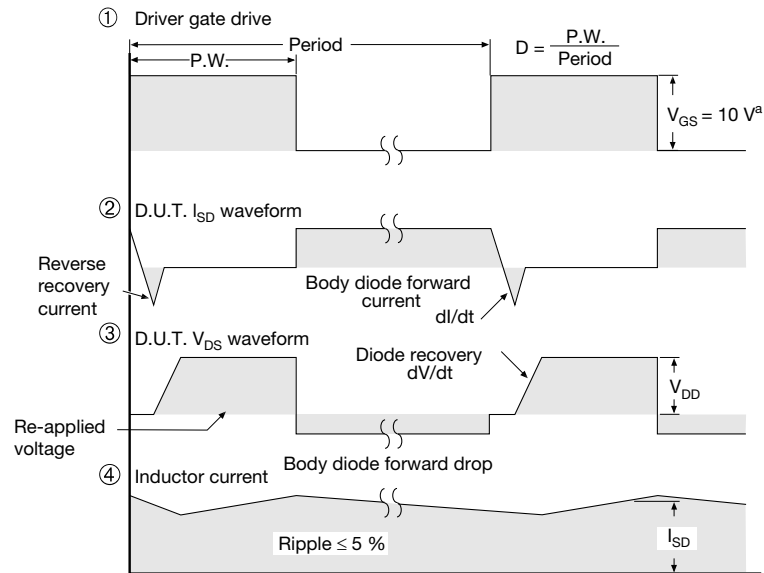
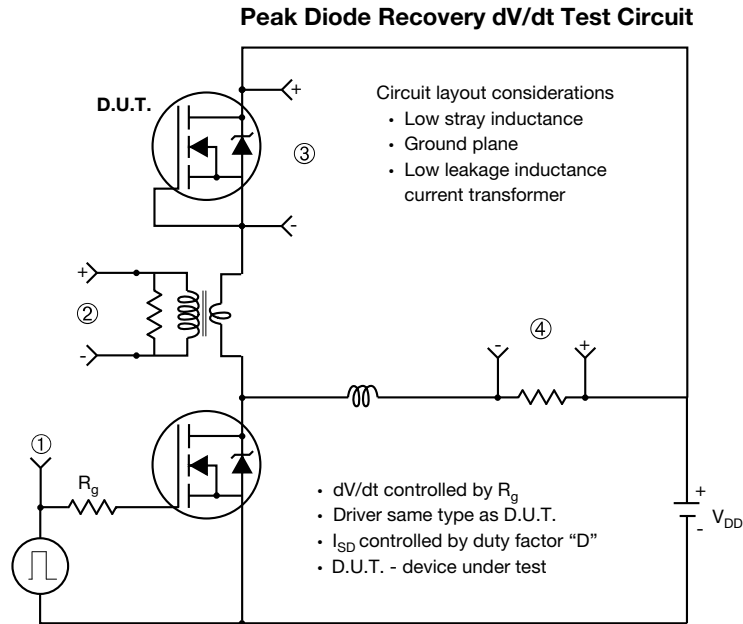


Fig. 13b - Gate Charge Test Circuit

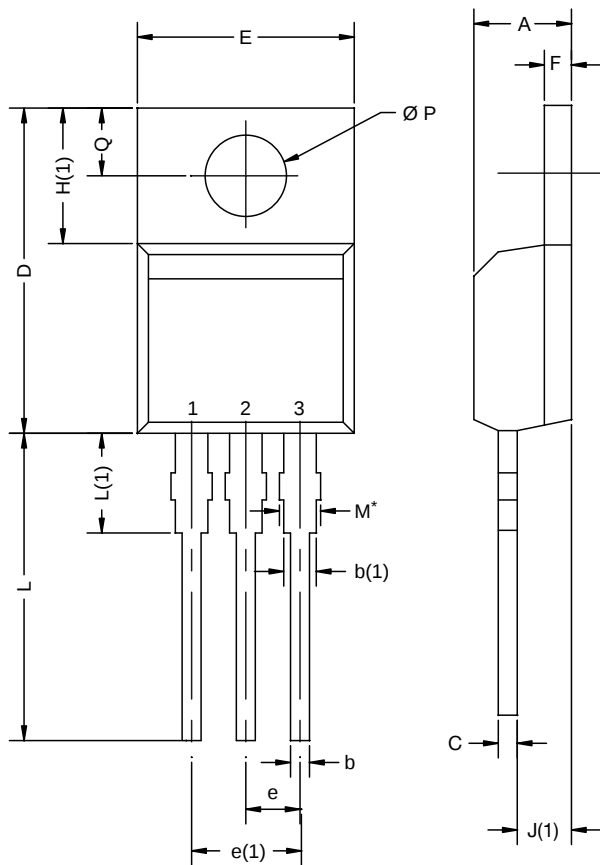


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12
 DWG: 5471

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
 Heatsink hole for HVM

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