



Description

The IRLML9301TRPBF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V.

This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = -30V, I_D = -4.1A$

$R_{DS(ON)} < 56m\Omega @ V_{GS}=10V$

Application

High power and current handing capability

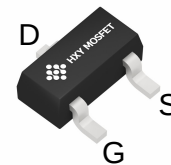
Lead free product is acquired

Surface mount package

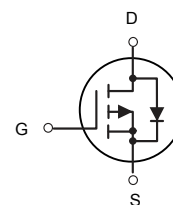
PWM applications

Load switch

Power management



SOT-23



P-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
IRLML9301TRPBF	SOT-23	3407 XXXX	3000PCS

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous	-4.1	A
I_{DM}	Drain Current-Pulsed (Note 1)	-13	A
P_D	Maximum Power Dissipation	1.32	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2)	125	$^{\circ}C/W$



Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=-250\mu A$	-30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=-1mA$	---	-0.02	---	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V$, $I_D=-3A$	---	48	56	$m\Omega$
		$V_{GS}=-4.5V$, $I_D=-1.5A$	---	78	90	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=-250\mu A$	-1.2	-1.5	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.32	---	mV/ $^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-24V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{DS}=-24V$, $V_{GS}=0V$, $T_J=55^\circ\text{C}$	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V$, $I_D=-3A$	---	4.8	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1MHz$	---	24	48	Ω
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-20V$, $V_{GS}=-4.5V$, $I_D=-3A$	---	5.22	7.3	nC
Q_{gs}	Gate-Source Charge		---	1.25	1.8	
Q_{gd}	Gate-Drain Charge		---	2.3	3.2	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V$, $V_{GS}=-10V$, $R_G=3.3\Omega$ $I_D=-1A$	---	18.4	37	ns
T_r	Rise Time		---	11.4	21	
$T_{d(off)}$	Turn-Off Delay Time		---	39.4	79	
T_f	Fall Time		---	5.2	10.4	
C_{iss}	Input Capacitance	$V_{DS}=-15V$, $V_{GS}=0V$, $f=1MHz$	---	463	650	pF
C_{oss}	Output Capacitance		---	82	115	
C_{rss}	Reverse Transfer Capacitance		---	68	95	
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	-3.2	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	-13	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=-1A$, $T_J=25^\circ\text{C}$	---	---	-1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Characteristics

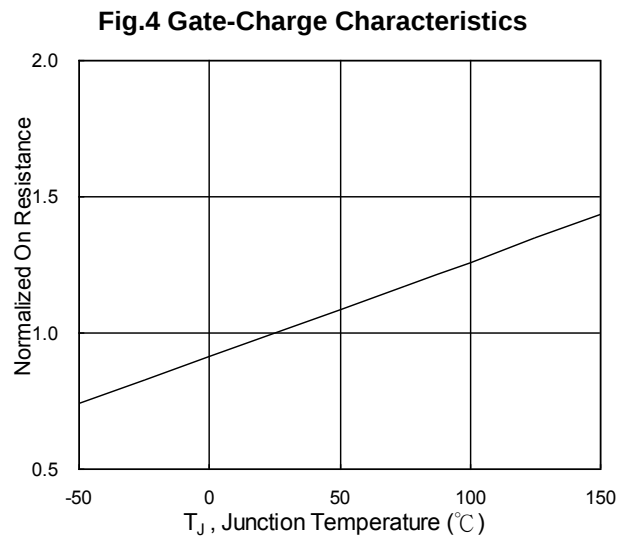
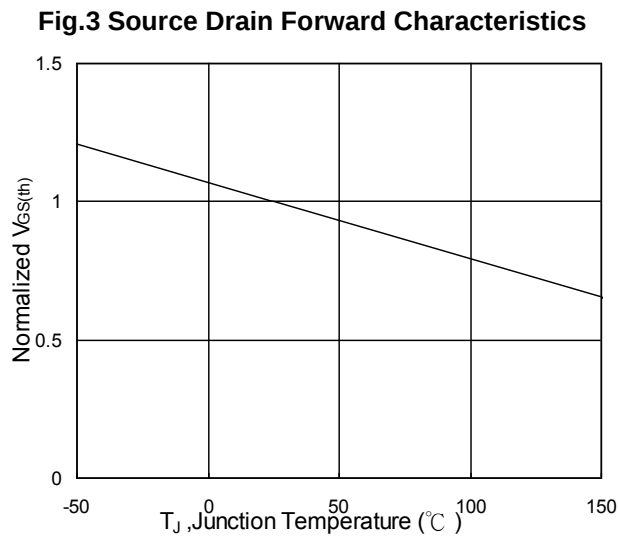
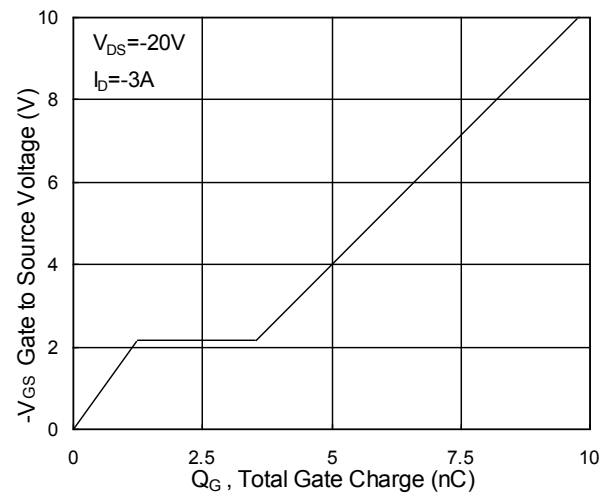
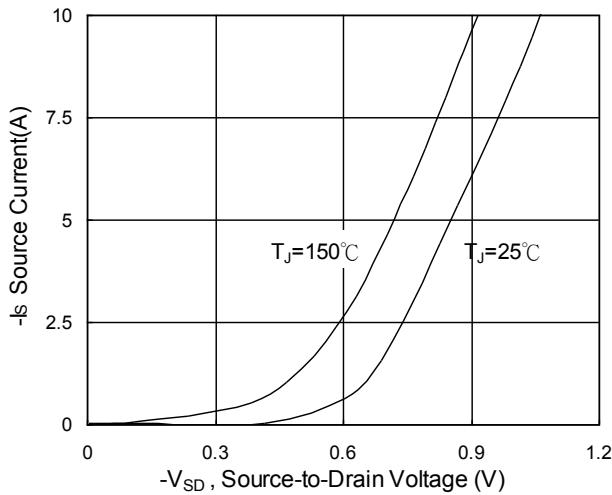
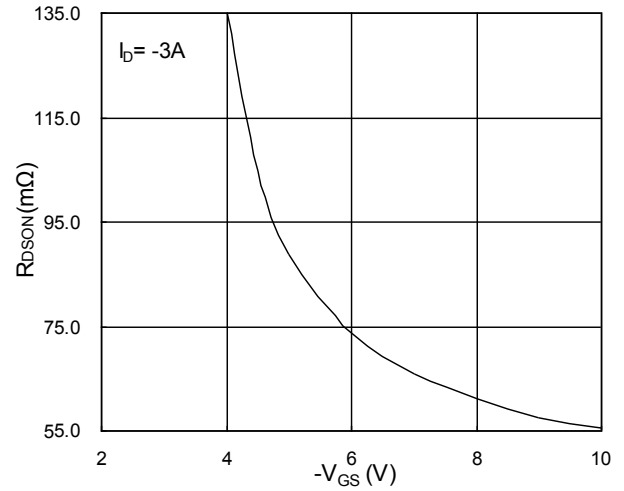
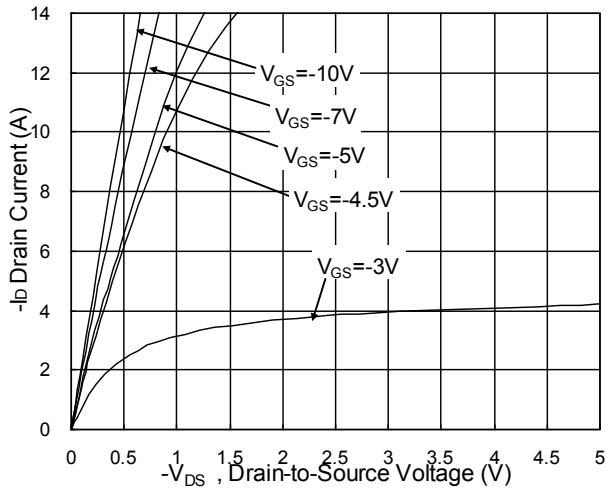




Fig.7 Capacitance



Fig.8 Safe Operating Area



Fig.9 Normalized Maximum Transient Thermal Impedance

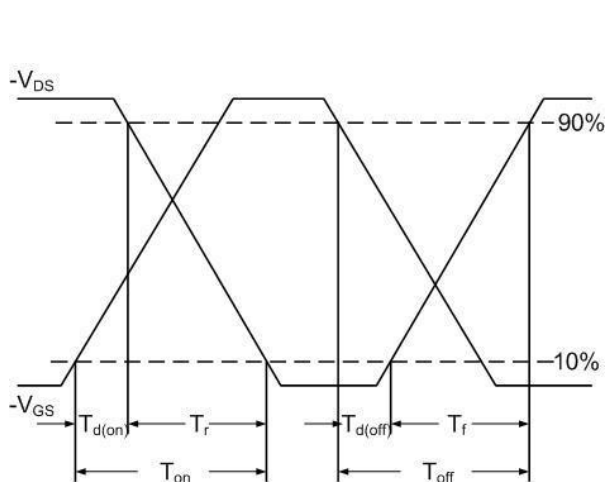


Fig.10 Switching Time Waveform

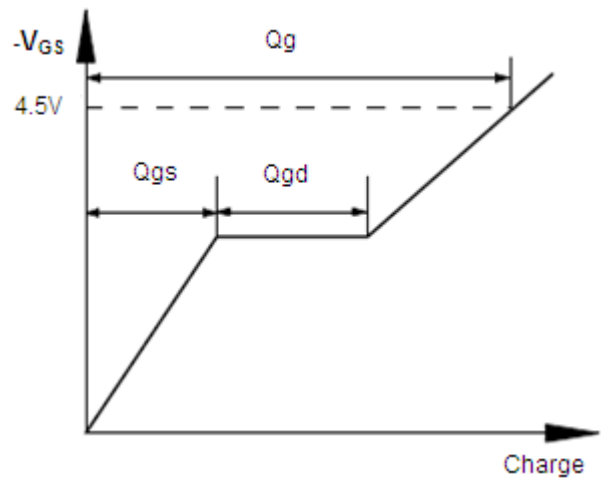
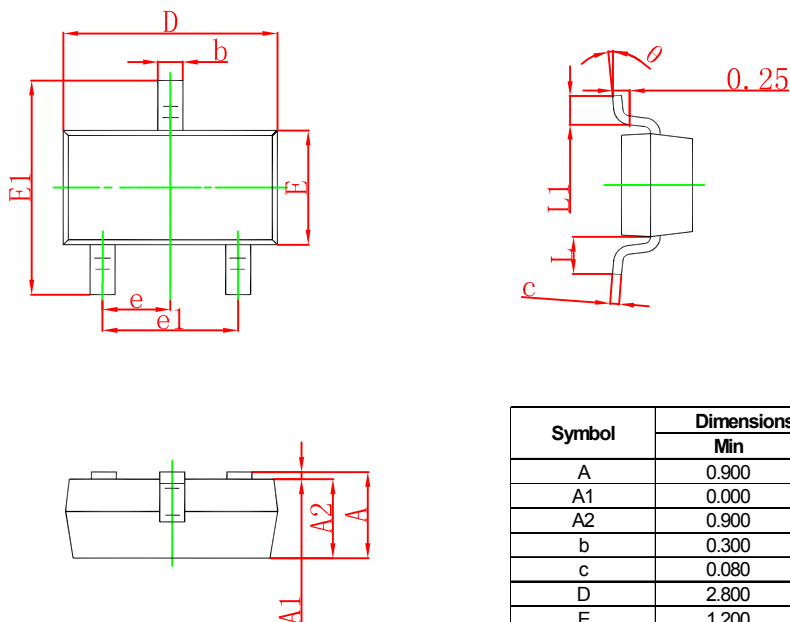


Fig.11 Gate Charge Waveform



SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

SOT-23 Suggested Pad Layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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