OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
EL7566

EL7556D

Integrated Adjustable 6 Amp Synchronous Switcher

FN7339
Rev 1.00
August 1, 2005

The EL7556D is an adjustable synchronous DC:DC switching regulator optimized for a 5V input and 1.0V-3.8V output. By combining integrated NMOS power FETS with a fused-lead package, the EL7556D can supply up to 6A continuous output current without the use of external power devices or discrete heat sinks, thereby minimizing design effort and overall system cost.

On-chip resistorless current sensing is used to achieve stable, highly efficient, current-mode control. The EL7556D also incorporates the VCC2DET function to directly interface with the Intel P54 and P55 microprocessors. Depending on the state of VCC2DET, the output voltage is internally preset to 3.5V or a user-adjustable voltage using two external resistors. In both internal and external feedback modes the active-high PWRGD output indicates when the regulator output is within ±10% of the programmed voltage. An on-board sensor monitors die temperature (OT) for over-temperature conditions and can be connected directly to OUTEN to provide automatic thermal shutdown. Adjustable oscillator frequency and slope compensation allow added flexibility in overall system design.

The EL7556D is available in a 28-pin SO package and is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL7556DCM	28-Pin SO	-	MDP0027
EL7556DCM-T13	28-Pin SO	13”	MDP0027
EL7556DCMZ (See Note)	28-Pin SO (Pb-free)	-	MDP0027
EL7556DCMZ-T13 (See Note)	28-Pin SO (Pb-free)	13”	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

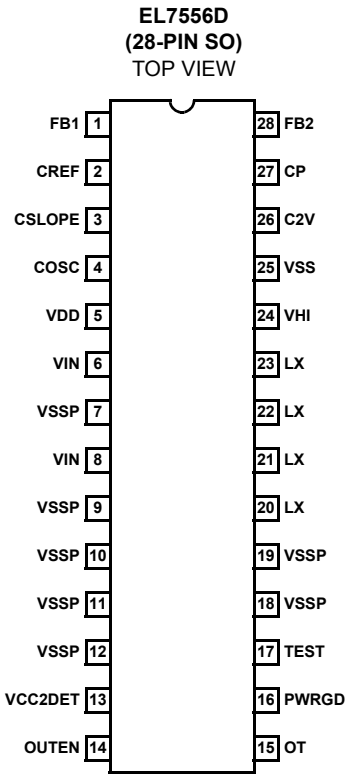
Features

- Improved temperature and voltage ranges
- 6A continuous load current
- Precision internal 1% reference
- 1.0V to 3.8V output voltage
- Internal power MOSFETs
- >90% efficiency
- Synchronous switching
- Adjustable slope compensation
- Over-temperature indicator
- Pulse-by-pulse current limiting
- Operates up to 1MHz
- 1.5% typical output accuracy
- Adjustable oscillator with sync
- Remote enable/disable
- Intel P54- and P55-compatible
- VCC2DET interface
- Internal soft-start
- Pb-free plus anneal available (RoHS compliant)

Applications

- PC motherboards
- Local high power CPU supplies
- 5V to 1.0V DC:DC conversion
- Portable electronics/instruments
- P54 and P55 regulators
- GTL+ Bus power supply

Pinout



Absolute Maximum Ratings (T_A = 25°C)

Storage Temperature Range . . . . . -65°C to +150°C
Supply (V_{IN}) 6.0V
Output Pins . . . . . -0.3V below GND, +0.3V above V_{DD}
Ambient Operating Temperature . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . 135°C
Peak Output Current 9A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

$V_{DD} = V_{IN} = 5V$, $C_{OSC} = 1nF$, $C_{SLOPE} = 470pF$, $T_A = 25°C$, unless otherwise specified.

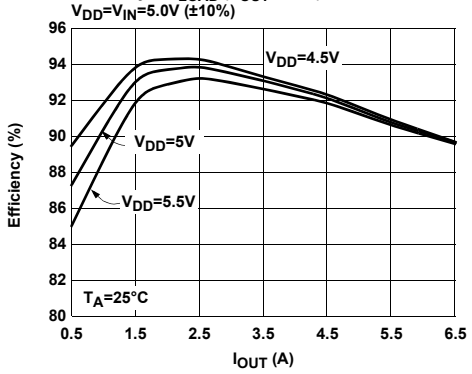
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
I_{DD}	V_{DD} Supply Current	OUTEN = 4V, F_{OSC} = 120kHz		11	25	mA
I_{DDOFF}	V_{DD} Standby Current	OUTEN = 0		0.1		mA
I_{VIN}	V_{IN} No Load Current	OUTEN = 0		3	5	mA
V_{OUT1}	Output Initial Accuracy	VCC2DET = 4V, I_L = 3A (see Fig. 1)	3.450	3.500	3.550	V
V_{OUT2}	Output Initial Accuracy	VCC2DET = 0V, I_L = 3A, R_3 = 150Ω, R_4 = 100Ω (see Fig. 1)	2.450	2.500	2.550	V
$V_{OUTLINE}$	Output Line Regulation	V_{DD} = 5V, ±10%	-1		1	%
$V_{OUTLOAD}$	Output Load Regulation	0A < I_{LOAD} < 6A, relative to I_L = 3A, continuous mode of operation (see Fig.1)	-1		1	%
R_{SHORT}	Short Circuit Load Resistance	IL = 6A, prior to continuous application of R_{SHORT}, OUTEN connected to OT		100		mΩ
$I_{I\ MAX}$	Current Limit			9		A
V_{OUTTC}	Output Tempco	-40°C < T_A < 85°C		±1		%
T_{OT}	Over-temperature Threshold			135		°C
T_{HYS}	Over-temperature Hysteresis			40		°C
V_{PWRGD}	Power Good Threshold Relative to Programmed Output Voltage	VCC2SEL = 4V, V_{OUT} = 3.50V	±6	±10	±14	%
V_{DDOFF}	Minimum V_{DD} for Shutdown		3.15			V
V_{DDON}	Maximum V_{DD} for Startup				4.15	V
V_{HYS}	Input Hysteresis	$V_{HYS} = V_{DDON} - V_{DDOFF}$		0.5		V
M_{ss}	Soft-start Slope			7		V/ms
D_{MAX}	Maximum Duty Cycle			96		%
CONTROLLER - INPUTS						
I_{PUP}	VCC2DET, OUTEN Pull-up Current	VCC2DET, OUTEN = 0	10	14	18	µA
I_{CSLOPE}	C_{SLOPE} Charging Current		23	28.5	34	µA
IFB1	FB1 Input Pull-up Current			2		µA
R_{OT}	Over-temperature Pull-up Resistance	OT = 0V	30	40	50	kΩ
V_{IH}	VCC2DET, OUTEN Input High		4			V
V_{IL}	VCC2DET, OUTEN Input Low				0.8	V
$V_{OH\ PWGD}$	Powergood Drive High	I_{LOAD} = 1mA	3.5			V
$V_{OL\ PWGD}$	Powergood Drive Low	I_{LOAD} = -1mA			1.0	V
CONTROLLER - REFERENCE						
V_{REF}	Reference Accuracy	I_{REF} = 0	1.247	1.260	1.273	V

Electrical Specifications $V_{DD} = V_{IN} = 5V$, $C_{OSC} = 1nF$, $C_{SLOPE} = 470pF$, $T_A = 25°C$, unless otherwise specified. **(Continued)**

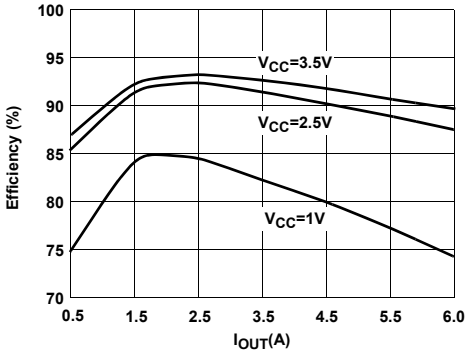
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{REFTC}	Reference Voltage Tempco			50		ppm/°C
$V_{REFLOAD}$	Reference Load Regulation	$0 < I_{LOAD} < 100\mu A$	0.5		0.5	%/°C
CONTROLLER - DOUBLER						
VC2V	Voltage Doubler Output	$V_{DD} = 5V$, $I_{LOAD} = 10mA$	7.5	8.1	8.7	V
CONTROLLER - OSCILLATOR						
F_{RAMP}	Oscillator Ramp Amplitude			1.2		V
$I_{OSC\ CHG}$	Oscillator Charge Current	$0.2V < V_{OSC} < 1.4V$		150		µA
$I_{OSC\ DIS}$	Oscillator Discharge Current	$0.2V < V_{OSC} < 1.4V$		5		mA
F_{OSC}	Oscillator Initial Accuracy		105	125	145	kHz
t_{SYNC}	Minimum Oscillator Sync Width			50		ns
POWER - FET						
I_{LEAK}	L_X Output Leakage to V_{SS}	$L_X = 0V$			100	µA
R_{DSON}	Composite FET Resistance		18		30	mΩ
R_{DSONTC}	R_{DSON} Tempco			0.1		mΩ/°C
t_{BRM}	FET Break Before Make Delay			10		ns
t_{LEB}	High Side FET Minimum on Time (LEB)			140		ns

Typical Performance Curves

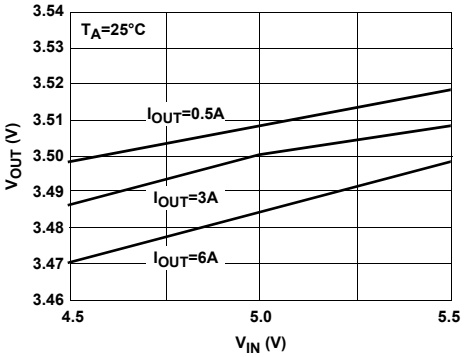
Efficiency vs I_{LOAD} (V_{OUT} =3.5V)
$V_{DD}=V_{IN}$=5.0V (±10%)



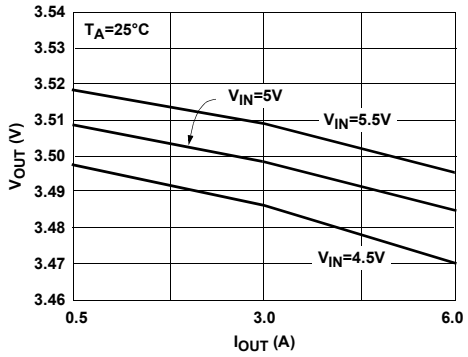
Efficiency vs I_{LOAD} (V_{DD}=5.0V)



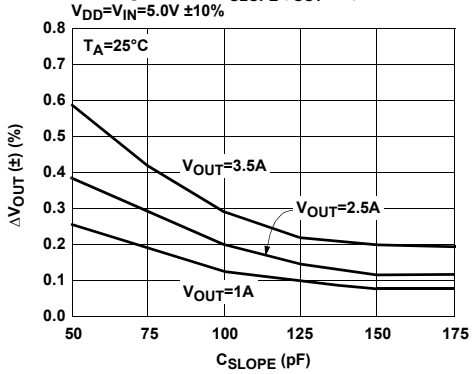
Line Regulation (C_{SLOPE}=100pF)



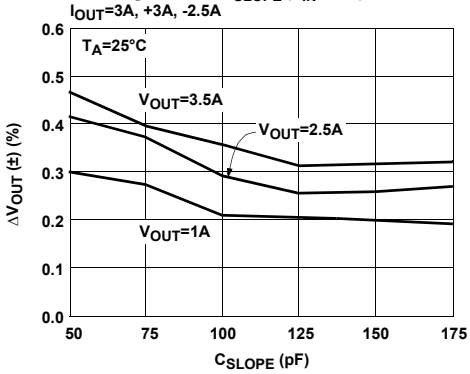
Load Regulation (C_{SLOPE}=100pF)



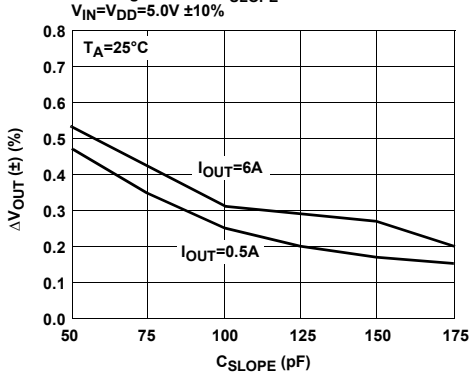
Line Regulation vs C_{SLOPE} (I_{OUT}=3A)
$V_{DD}=V_{IN}$=5.0V ±10%



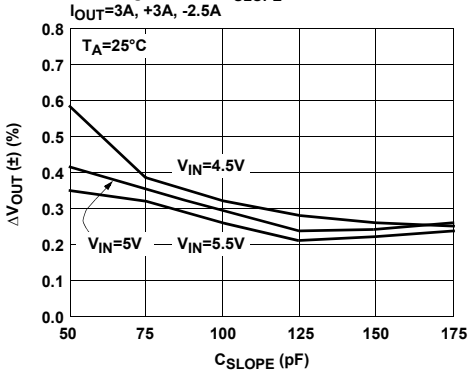
Load Regulation vs C_{SLOPE} (V_{IN}=5.0V)
I_{OUT}=3A, +3A, -2.5A



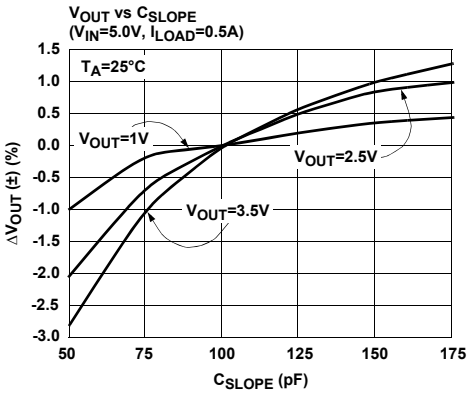
Line Regulation vs C_{SLOPE}
$V_{IN}=V_{DD}$=5.0V ±10%

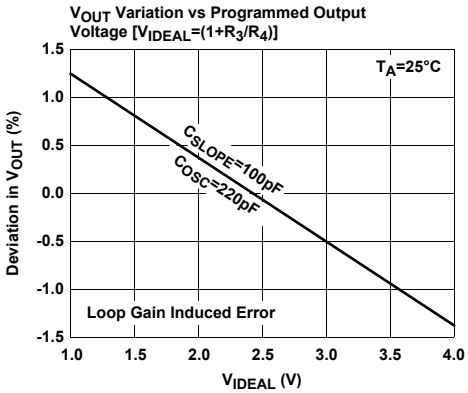


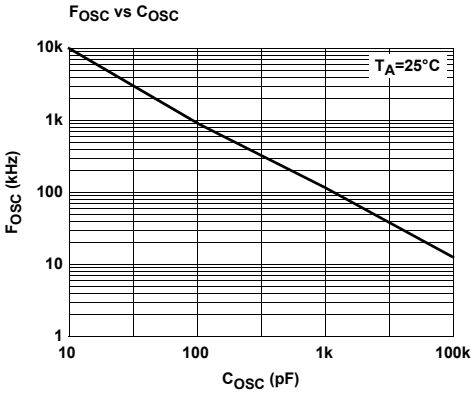
Load Regulation vs C_{SLOPE}
I_{OUT}=3A, +3A, -2.5A

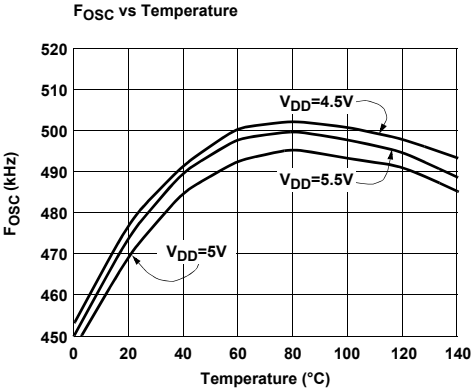


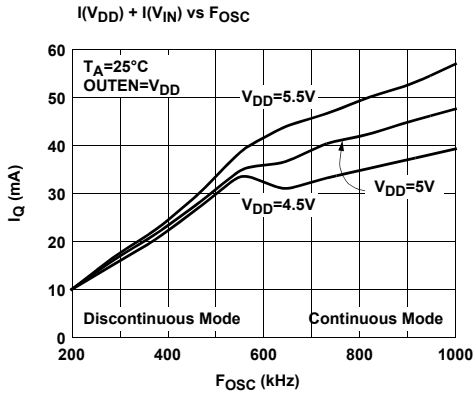
Typical Performance Curves

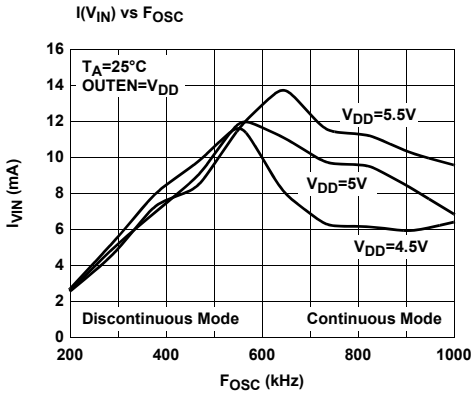


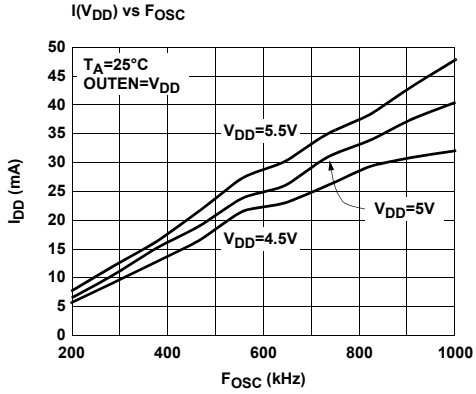


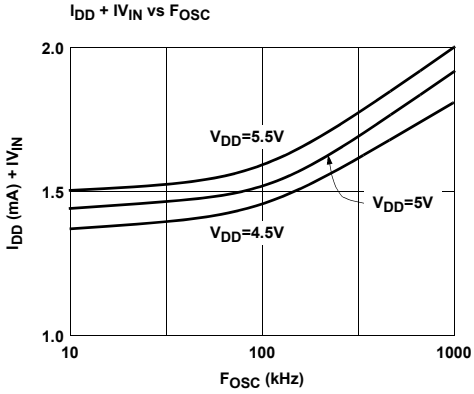






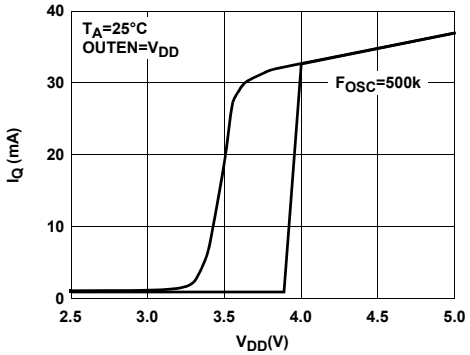




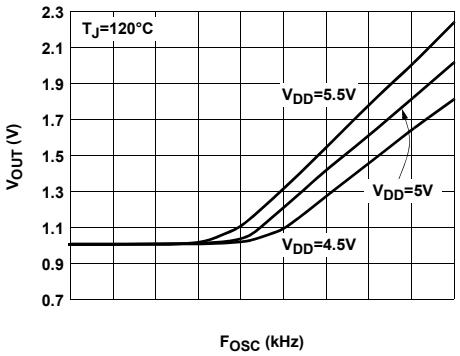


Typical Performance Curves

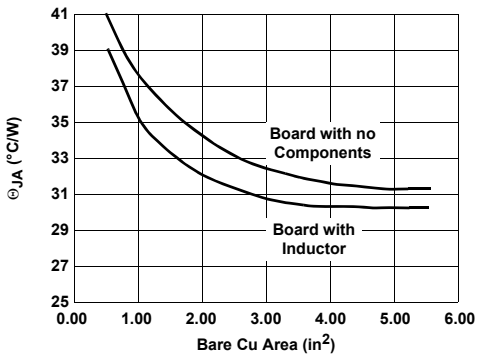
Power On Reset



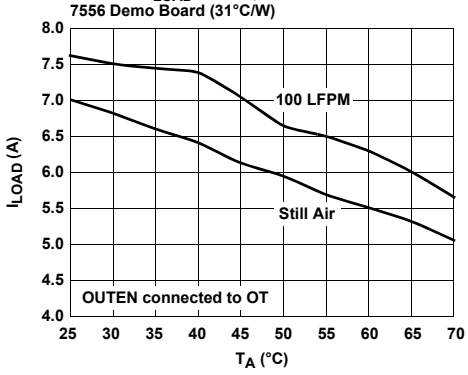
Minimum Output Voltage vs F_{OSC}



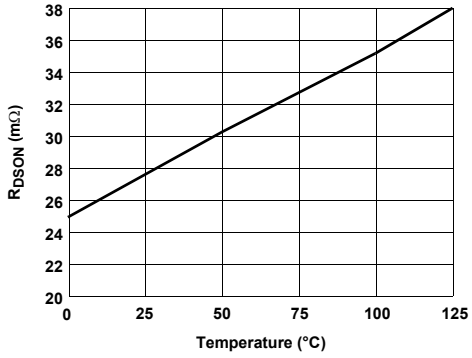
Θ_{JA} vs Cu Area



Maximum I_{LOAD} vs Temperature
7556 Demo Board (31°C/W)



R_{DSON} vs Temperature

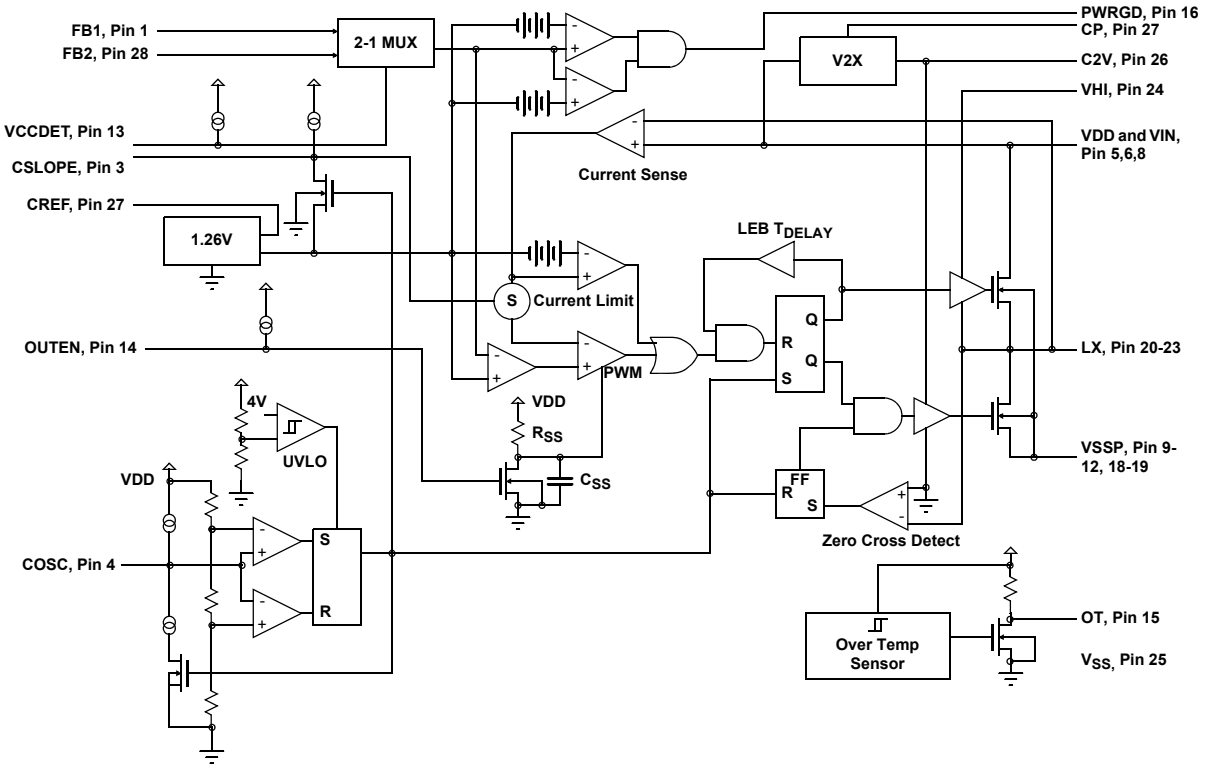


Pin Descriptions

I = Input, O = Output, S = Supply

PIN NUMBER	PIN NAME	PIN TYPE	FUNCTION
1	FB1	I	Voltage feedback pin for the buck regulator. Active when VCC2DET is logic low. Normally connected to external resistor divider between V_{OUT} and GND. A 2µA pull-up current forces V_{OUT} to V_{SS} in the event that FB1 is floating and VCC2DET is inadvertently connected to GND.
2	CREF	I	Bandgap reference bypass capacitor. Typically 0.1µF to V_{SS}.
3	CSLOPE	I	Slope compensation capacitor. Ramp width corresponds to LX duty cycle. C_{SLOPE} to C_{OSC} ratio is normally 1:1.5.
4	COSC	I	Oscillator timing capacitor. F_{OSC}(Hz) can be approximated by: $F_{OSC}(Hz) = 0.0001/C_{OSC}$. C_{OSC} in Farads.
5	VDD	S	Power Supply for PWM control circuitry. Normally the same potential as V_{IN}.
6	VIN	S	Power supply for the buck regulator. Connected to the drain of the high-side NMOS FET.
7	VSSP	S	Ground return for the buck regulator. Connected to the source of the low-side synchronous NMOS FET.
8	VIN	S	Same as pin 6.
9	VSSP	S	Same as pin 7.
10	VSSP	S	Same as pin 7.
11	VSSP	S	Same as pin 7.
12	VSSP	S	Same as pin 7.
13	VCC2DET	I	VCC2DET interface logic input. When driven to logic 1 V_{OUT} = 3.500V. When driven to logic 0 the PWM uses FB1 to determine V_{OUT}: V_{OUT} = 1.0V*(1+R3/R4).
14	OUTEN	I	The switching regulator output is enabled when logic 1. The reference voltage output operates whenever the power supply is qualified (V_{DD}>VPOR) regardless of the state of this pin.
15	OT	O	Over temperature indicator. Normally high. Pulls low when die temperature exceeds 135°C, returns to the high state when die temperature has cooled to 100°C.
16	PWRGD	O	Power good window comparator output. Logic 1 when regulator output is within ±10% of programmed voltage.
17	TEST	I	Test pin. Must be connected to VSSP in normal operation.
18	VSSP	S	Same as pin 7.
19	VSSP	S	Same as pin 7.
20	LX	O	Inductor drive pin. High current switching output whose average voltage equals the regulator output voltage.
21	LX	O	Same as pin 20.
22	LX	O	Same as pin 20.
23	LX	O	Same as pin 20.
24	VHI	I	Gate drive to high-side driver. Bootstrapped from LX with a 0.1µF capacitor.
25	VSS	S	Ground return for the control circuitry.
26	C2V	I	Connected to voltage doubler output. Supplies gate drive to the low-side driver.
27	CP	O	Drives the negative side of charge pump capacitor at one-half the oscillator frequency F_{OSC}.
28	FB2	I	Voltage feedback pin. Active when VCC2DET is logic 1. Internally preset to V_{OUT} = 3.5V.

Block Diagram



Applications Information

Circuit Description

General

The EL7556D is a fixed frequency, current mode controlled DC:DC converter with integrated N-channel power MOSFETS and a high precision reference. The device incorporates all of the active circuitry required to implement a cost effective, user-programmable 6A synchronous buck converter suitable for use in CPU power supplies. By combining fused-lead packaging technology with an efficient synchronous switching architecture, high power outputs (21W) can be realized without the use of discrete external heat sinks.

Theory of Operation

The EL7556D is composed of 7 major blocks:

1. PWM Controller
2. Output Voltage Mode Select
3. NMOS Power FETS and Drive Circuitry
4. Bandgap Reference
5. Oscillator
6. Temperature Sensor
7. Power Good and Power On Reset

PWM Controller

The EL7556D regulates output voltage through the use of current-mode controlled pulse width modulation. The three main elements in a PWM controller are the feedback loop and reference, a pulse width modulator whose duty cycle is controlled by the feedback error signal, and a filter which averages the logic level modulator output. In a step-down (buck) converter, the feedback loop forces the time-averaged output of the modulator to equal the desired output voltage. Unlike pure voltage-mode control systems current-mode control utilizes dual feedback loops to provide both output voltage and inductor current information to the controller. The voltage loop minimizes DC and transient errors in the output voltage by adjusting the PWM duty-cycle in response to changes in line or load conditions. Since the output voltage is equal to the time-average of the modulator output the relatively large LC time constants found in power supply applications generally results in low bandwidth and poor transient response. By directly monitoring changes in inductor current via a series sense resistor the controller's response time is not entirely limited by the output LC filter and can react more quickly to changes in line or load conditions. This feed-forward characteristic also simplifies AC loop compensation since it adds a zero to the overall loop response. Through proper selection of the current-feedback to voltage-feedback ratio, the overall loop response will approach a one pole system. The resulting system offers several advantages over traditional voltage control systems, including simpler loop compensation,

pulse by pulse current limiting, rapid response to line variation and good load step response.

The heart of the controller is a triple-input direct summing comparator which sums voltage feedback, current feedback and slope compensating ramp signals together. Slope compensation is required to prevent system instability which occurs in current-mode topologies operating at duty-cycles greater than 50% and is also used to define the open-loop gain of the overall system. The compensation ramp amplitude is user adjustable and is set using a single external capacitor (C_{SLOPE}). Each comparator input is weighted and determines the load and line regulation characteristics of the system. Current feedback is measured by sensing the inductor current flowing through the high-side switch whenever it is conducting. At the beginning of each oscillator period the high-side NMOS switch is turned on and C_{SLOPE} ramps positively from its reset state (V_{REF} potential). The comparator inputs are gated off for a minimum period of time (LEB) after the high-side switch is turned on to allow the system to settle. The Leading Edge Blanking (LEB) period prevents the detection of erroneous voltages at the comparator inputs due to switching noise. When programming low regulator output voltages the LEB delay will limit the maximum operating frequency of the circuit since the LEB will result in a minimum duty-cycle regardless of the PWM error voltage. This relationship is shown in the performance curves. If the inductor current exceeds the maximum current limit (I_{LMAX}), a secondary over-current comparator will terminate the high-side switch. If I_{LMAX} has not been reached, the regulator output voltage is then compared to the reference voltage V_{REF}. The resultant error voltage is summed with the current feedback and slope compensation ramp. The high-side switch remains on until all three comparator inputs have summed to zero, at which time the high-side switch is turned off and the low-side switch is turned on. In order to eliminate cross-conduction of the high-side and low-side switches a 10ns break-before-make delay is incorporated in the switch driver circuitry. In the continuous mode of operation the low-side switch will remain on until the end of the oscillator period. In order to improve the low current efficiency of the EL7556D, a zero-crossing comparator senses when the inductor transitions through zero. Turning off the low-side switch at zero inductor current prevents forward conduction through the internal clamping diodes (LX to V_{SSP}) when the low-side switch turns off, reducing power dissipation. The output enable (OUTEN) input allows the regulator output to be disabled by an external logic control signal.

Output Voltage Mode Select

The VCC2DET multiplexes the FB1 and FB2 pins to the PWM controller. A logic 1 on VCC2DET selects the FB2 input and forces the output voltage to the internally programmed value of 3.50V. A logic zero on VCC2DET selects FB1 and allows the output to be programmed from 1.0 to 3.8V. In general:

$$V_{OUT} = 1V \times \left(1 + \frac{R_3}{R_4}\right) \times Volt$$

However, due to the relatively low open loop gain of the system, gain errors will occur as the output voltage and loop-gain are changed. This is shown in the performance curves. (The output voltage is factory trimmed to minimize error at a 2.50V output). A 2uA pull-up current from FB1 to V_{IN} forces V_{OUT} to GND in the event that FB1 is not used and the VCC2DET is inadvertently toggled between the internal and external feedback mode of operation.

NMOS Power FETs and Drive Circuitry

The EL7556D integrates low resistance (25mΩ) NMOS FETS to achieve high efficiency at 6A. Gate drive for both the high-side and low-side switches is derived through a charge pump consisting of the CP pin and external components D1-D3 and C5-C6. The CP output is a low resistance inverter driven at one-half the oscillator frequency. This is used in conjunction with D2-D3 to generate a 7.5V (typical) voltage on the C2V pin which provides gate drive to the low-side NMOS switch and associated level shifter. In order to use an NMOS switch for the high-side drive it is necessary to drive the gate voltage above the source voltage (LX). This is accomplished by boot-strapping the V_{HI} pin above the C2V voltage with capacitor C6 and diode D1. When the low-side switch is turned on the LX voltage is close to GND potential and capacitor C6 is charged through diodes D1-D3 to approximately 6.9V. At the beginning of the next cycle the high side switch turns on and the LX pin begins to rise from GND to V_{DD} potential. As the LX pin rises the positive plate of capacitor C6 follows and eventually reaches a value of approximately 11.2V, for V_{DD}=5V. This voltage is then level shifted and used to drive the gate of the high-side FET, via the V_{HI} pin.

Reference

A 1% temperature compensated band gap reference is integrated in the EL7556D. The external C_{REF} capacitor acts as the dominant pole of the amplifier and can be increased in size to maximize transient noise rejection. A value of 0.1uF is recommended.

Oscillator

The system clock is generated by an internal relaxation oscillator with a maximum duty-cycle of approximately 96%. Operating frequency can be adjusted through the C_{OSC} pin or can be driven by an external clock source. If the oscillator is driven by an external source, care must be taken in the selection of C_{SLOPE}. Since the C_{OSC} and C_{SLOPE} values determine the open loop gain of the system, changes to C_{OSC} require corresponding changes to C_{SLOPE}in order to maintain a constant gain ratio. The recommended ratio of C_{OSC} to C_{SLOPE} is 1.5:1

Temperature Sensor

An internal temperature sensor continuously monitors die temperature. In the event that die temperature exceeds the thermal trip-point, the OT pin will output a logic 0. The upper and lower trip points are set to 135°C and 100°C, respectively. To enable thermal shutdown this pin should be tied directly to

OUTEN. Use of this feature is recommended during normal operation

Power Good and Power On Reset

During power up the output regulator will be disabled until V_{IN} reaches a value of approximately 4.0V. Approximately 500mV of hysteresis is present to eliminate noise induced oscillations.

Under-voltage and over-voltage conditions on the regulator output are detected through an internal window comparator. A logic 1 on the PWRGD output indicates that regulated output voltage is within ±10% of the nominally programmed output voltage. Although small, the typical values of the PWRGD threshold will vary with changes to external feedback (and resultant loop gain) of the system. This dependence is shown in the typical performance curves.

Thermal Management

The EL7556D utilizes “fused lead” packaging technology in conjunction with the system board layout to achieve a lower thermal resistance than typically found in standard 28-pin SO packages. By fusing (or connecting) multiple external leads to the die substrate within the package, a very conductive heat path to the outside of the package is created. This conductive heat path MUST then be connected to a heat sinking area on the PCB in order to dissipate heat out and away from the device. The conductive paths for the EL7556D package are the fused leads: # 7, 9, 10, 11, 12, 18, and 19. If a sufficient amount of PCB metal area is connected to the fused package leads, a junction-to-ambient thermal resistance of approximately 31°C/W can be achieved (compared to 78°C/W for a standard SO28 package). The general relationship between PCB heat-sinking metal area and the thermal resistance for this package is shown in the Performance Curves section of this data sheet. It can be readily seen that the thermal resistance for this package approaches an asymptotic value of approximately 31°C/W without any airflow.

Additional information can be found in Application Note #8 (Measuring the Thermal Resistance of Power Surface-Mount Packages).

If the thermal shutdown pin is connected to OUTEN the IC will enter thermal shutdown when the maximum junction temperature is reached. For a thermal shutdown of 135ºC and power dissipation of 2.2W the ambient temperature is limited to a maximum value of 67ºC (typical). The ambient temperature range can be extended with the application of air flow. For example, the addition of 100LFM reduces the thermal resistance by approximately 15% and can extend the operating ambient to 77ºC (typical). Since the thermal performance of the IC is heavily dependent on the board layout, the system designer should exercise care during the design phase to ensure that the IC will operate under the worst-case environmental conditions.