SDLS050 – NOVEMBER 1971 – REVISED MARCH 1988

- **15-mA Constant-Current Outputs**

  For Driving Common-Anode LEDs such as TIL302 or TIL303 Without Series Resistors

- **Universal Logic Capabilities**

  Ripple Blanking of Extraneous Zeros
  Latch Outputs Can Drive Logic Processors Simultaneously

  Decimal Point Driver Is Included

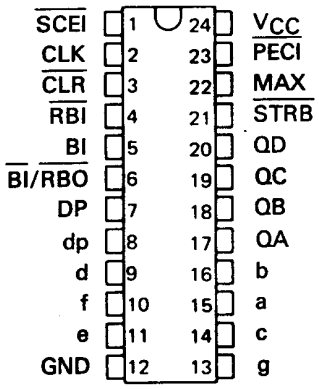
- **Synchronous BCD Counter Capability**

  Cascadable to N-Bits

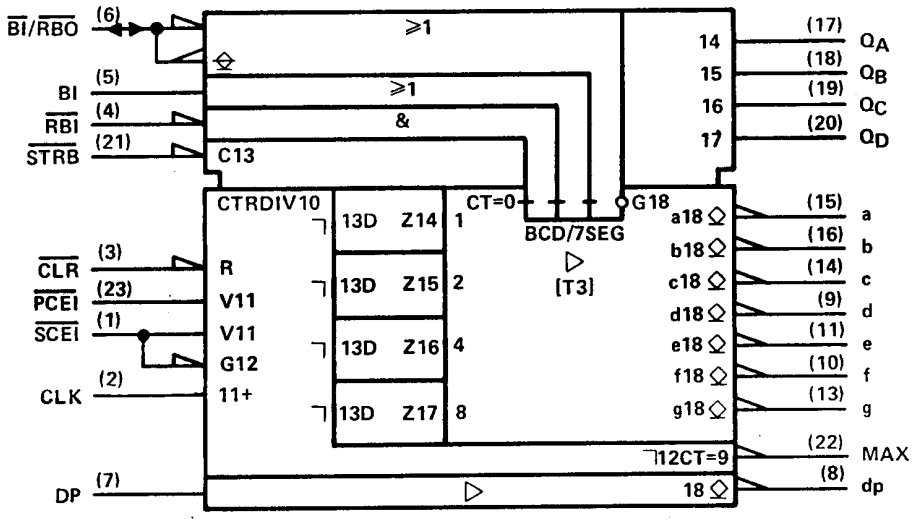
  Look-Ahead-Enable Techniques Minimize Speed Degradation When Cascaded for Large-Word Display

  Direct Clear Input

N PACKAGE
(TOP VIEW)



logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

This TTL MSI circuit contains the equivalent of 86 gates on a single chip. Logic inputs and outputs are completely TTL compatible. The buffered inputs are implemented with relatively large resistors in series with the bases of the input transistors to lower drive-current requirements to one-half of that required for a standard Series 54/74 TTL input. The serial-count-enable, actually two internal emitters, is rated as one standard Series 54/74 load. The logic outputs, except $\overline{RBO}$, have active pull-ups.

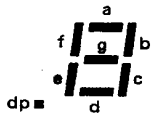
The SN74143 driver output is designed specifically to maintain a relatively constant on-level sink current of approximately 15 milliamperes from output "a" through "g" and seven milliamperes from output "dp" over a voltage range from one to five volts. Any number of LED's in series may be driven as long as the output voltage rating is not exceeded.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Maximum clock frequency is typically 18 megahertz and power dissipation is typically 280 milliwatts. The SN74143 is characterized for operation from 0°C to 70°C.

description (continued)

Functions of the inputs and outputs of these devices are as follows:

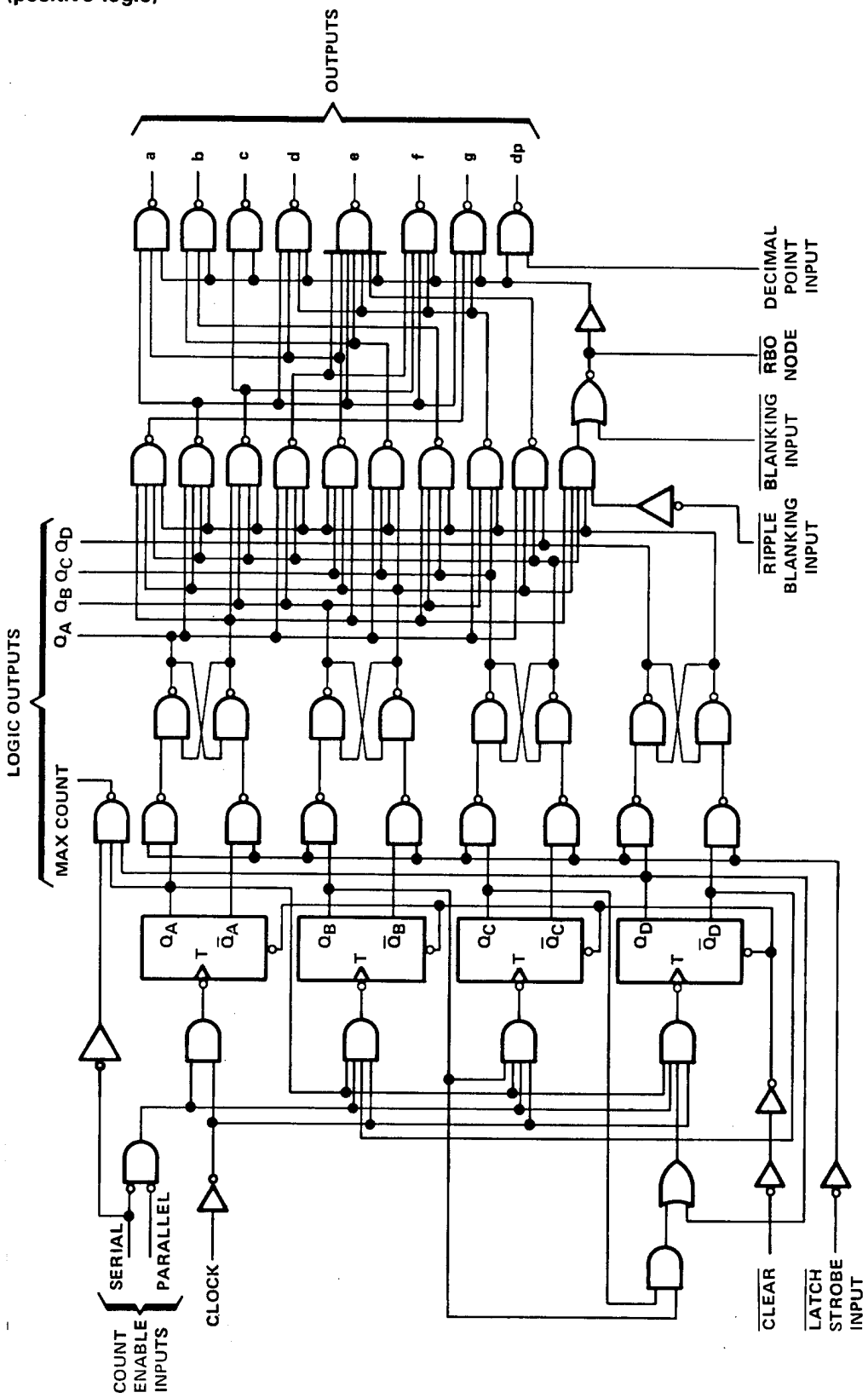
FUNCTION	PIN NO.	DESCRIPTION
CLEAR INPUT	3	When low, resets and holds counter at 0. Must be high for normal counting.
CLOCK INPUT	2	Each positive-going transition will increment the counter provided that the circuit is in the normal counting mode (serial and parallel count enable inputs low, clear input high).
PARALLEL COUNT ENABLE INPUT (PCEI)	23	Must be low for normal counting mode. When high, counter will be inhibited. Logic level must not be changed when the clock is low.
SERIAL COUNT ENABLE INPUT (SCEI)	1	Must be low for normal counting mode, also must be low to enable maximum count output to go low. When high, counter will be inhibited and maximum count output will be driven high. Logic level must not be changed when the clock is low.
MAXIMUM COUNT OUTPUT	22	Will go low when the counter is at 9 and serial count enable input is low. Will return high when the counter changes to 0 and will remain high during counts 1 through 8. Will remain high (inhibited) as long as serial count enable input is high.
LATCH STROBE INPUT	21	When low, data in latches follow the data in the counter. When high, the data in the latches are held constant, and the counter may be operated independently.
LATCH OUTPUTS (Q_A, Q_B, Q_C, Q_D)	17, 18, 19, 20	The BCD data that drives the decoder can be stored in the 4-bit latch and is available at these outputs for driving other logic and/or processors. The binary weights of the outputs are: $Q_A = 1$, $Q_B = 2$, $Q_C = 4$, $Q_D = 8$.
DECIMAL POINT INPUT	7	Must be high to display decimal point. The decimal point is not displayed when this input is low or when the display is blanked.
BLANKING INPUT ($\overline{BI}$)	5	When high, will blank (turn off) the entire display and force $\overline{RBO}$ low. Must be low for normal display. May be pulsed to implement intensity control of the display.
RIPPLE-BLANKING INPUT ($\overline{RBI}$)	4	When the data in the latches is BCD 0, a low input will blank the entire display and force the $\overline{RBO}$ low. This input has no effect if the data in the latches is other than 0.
RIPPLE-BLANKING OUTPUT ($\overline{RBO}$)	6	Supplies ripple blanking information for the ripple blanking input of the next decade. Provides a low if $\overline{BI}$ is high, or if $\overline{RBI}$ is low and the data in the latches in BCD 0; otherwise, this output is high. This pin has a resistive pull-up circuit suitable for performing a wire-AND function with any open-collector output. Whenever this pin is low the entire display will be blanked; therefore, this pin may be used as an active-low blanking input.
LED/LAMP DRIVER OUTPUTS (a, b, c, d, e, f, g, dp)	15, 16, 14, 9 11, 10, 13, 8	Outputs for driving seven-segment LED's or lamps and their decimal points. See segment identification and resultant displays on following page.



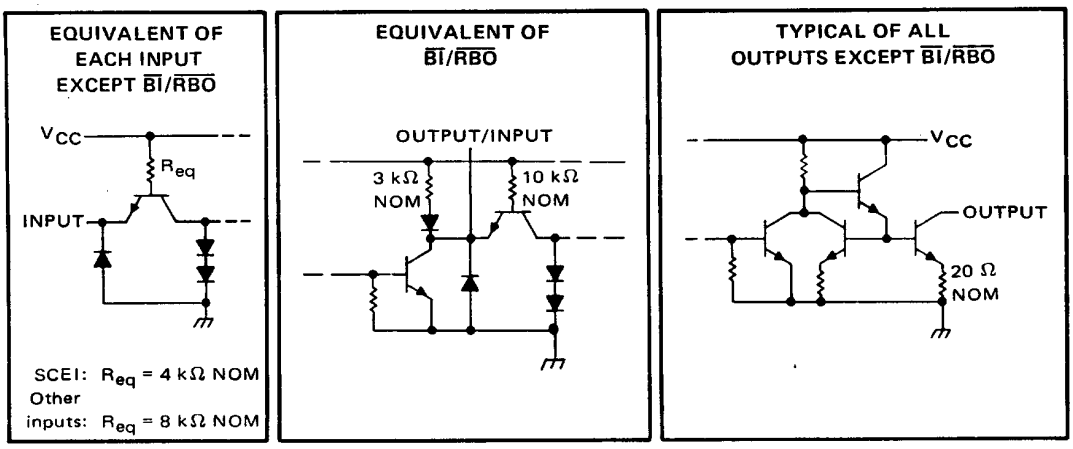
SEGMENT IDENTIFICATION

NUMERICAL DESIGNATIONS–RESULTANT DISPLAYS

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state current at outputs "a" thru "g" and "dp" . . . . . 250 μA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 2) . . . . . 1.4 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
On-state voltage at outputs a thru g and dp ('143 only)		1		5	V
High-level output current, I_{OH}	Q_A, Q_B, Q_C, Q_D			−240	μA
	Maximum count			−560	
	$\overline{RBO}$			−120	
Low-level output current, I_{OL}	Q_A, Q_B, Q_C, Q_D, $\overline{RBO}$			4.8	mA
	Maximum count			11.2	
Clock pulse width, $t_{w(clock)}$	High logic level	25			ns
	Low logic level	55			
Clear pulse width, $t_{w(clear)}$		25			ns
Setup time, t_{su}	Serial and parallel carry	30↑			ns
	Clear inactive state	60↑			
Operating free-air temperature, T_A		0		70	°C

↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	$\overline{RBO}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4			V
		Q_A, Q_B, Q_C, Q_D					
		Maximum count					
V_{OL}	Low-level output voltage	Q_A, Q_B, Q_C, $\overline{RBO}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.4	V
		Maximum count					
$V_{O(off)}$	Off-state output voltage	Outputs a thru g, dp	V_{CC} = MAX, I_{OH} = 250 μA	7			V
$V_{O(on)}$	On-state output voltage	Outputs a thru g, dp	V_{CC} = MIN				V
$I_{O(on)}$	On-state output current	Outputs a thru g	V_{CC} = MIN, V_O = 1 V	9	15		mA
			V_{CC} = 5 V, V_O = 2 V		15		
			V_{CC} = MAX, V_O = 5 V		15	22	
		Output dp	V_{CC} = MIN, V_O = 1 V	4.5	7		
			V_{CC} = 5 V, V_O = 2 V		7		
			V_{CC} = MAX, V_O = 5 V		7	12	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Serial carry	V_{CC} = MAX, V_I = 2.4 V			40	μA
		$\overline{RBO}$ node		−0.12	−0.5		mA
		Other inputs				20	μA
I_{IL}	Low-level input current	Serial carry	V_{CC} = MAX, V_I = 0.4 V, See Note 3			−1.6	
		$\overline{RBO}$ node			−1.5	−2.4	mA
		Other inputs				−0.8	
I_{OS}	Short-circuit output current	Q_A, Q_B, Q_C, Q_D	V_{CC} = MAX	−9		−27.5	mA
		Maximum count		−15		−55	
I_{CC}	Supply current		V_{CC} = MAX, See Note 4		56	93	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 3. I_{IL} at $\overline{RBO}$ node is tested with $\overline{BI}$ grounded and RBI at 4.5 V.

4. I_{CC} is measured after the following conditions are established:
   a) $\overline{Strobe}$ = $\overline{RBI}$ = DP = 4.5 V
   b) Parallel count enable = serial count enable = $\overline{BI}$ = GND
   c) Clear ( ) then clock until all outputs are on ( )
   d) Outputs "a" through "g" and "dp" at 2.5 V, all other outputs open.

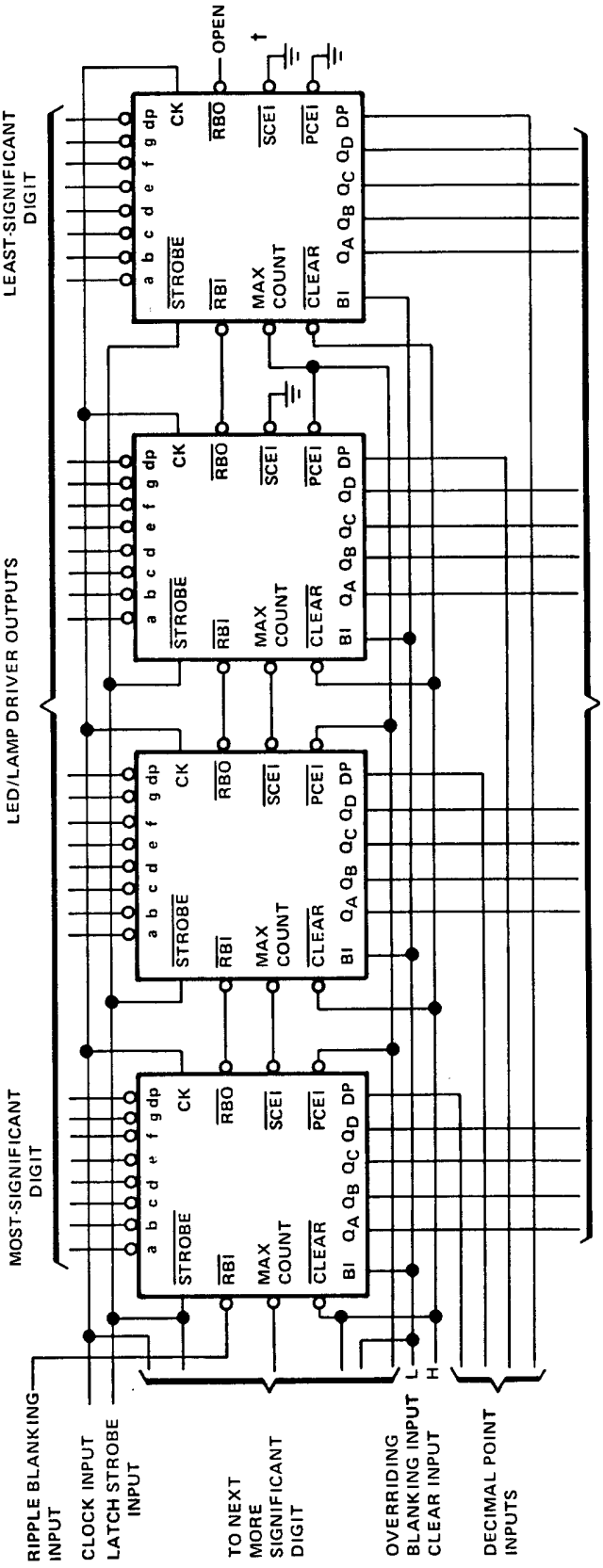
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				12	18		MHz
t_{PLH}	Serial look-ahead	Maximum count	C_L = 15 pF, R_L = 560 Ω, See Note 5		12	20	ns
t_{PHL}					23	35	
t_{PLH}	Clock	Maximum count			26	40	ns
t_{PHL}					29	45	
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D	C_L = 15 pF, R_L = 1.2 kΩ,		28	45	ns
t_{PHL}							

TYPICAL APPLICATION DATA

This application demonstrates how the drivers may be cascaded for N-bit display applications. It features:

- Synchronous, look-ahead counting
- Ripple blanking of leading zeros; blanking of trailing zeros (not illustrated) can also be implemented
- Overriding blanking for total suppression or intensity modulation of display
- Direct parallel clear
- Latch strobe permits counter to acquire next display while viewing current display



†The serial count-enable input of the least-significant digit is normally grounded; however, it may be used as a count-enable control for the entire counter (high to disable, low to count) provided the logic level on this pin is not changed while the clock line is low or false counting may result.

FUNCTION TABLE

FUNCTION	CLOCK PULSE	INPUTS							OUTPUTS												TYPICAL DISPLAY	NOTES
		CLEAR	LATCH STROBE	RBI	BI	DECIMAL INPUT	SERIAL CARRY	PARALLEL CARRY	RBI/RBO	MAXIMUM COUNT OUTPUT	LATCH Q_D Q_C Q_B Q_A	a	b	c	d	e	f	g	dp		
Clear/Ripple Blank		L	L	L	X	X	X	X	L	H	L L L L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	None	A, E
Blank		H	L	X	H	X	X	X	L	H	L L L L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	None	A, D, E
Decimal	0	H	L	H	L	H	L	L	H	H	L L L L	ON	ON	ON	ON	ON	ON	OFF	ON		B
	1	H	L	H	L	L	L	L	H	H	L L L H	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF		B
	2	H	L	H	L	L	L	L	H	H	L L H L	ON	ON	OFF	ON	ON	OFF	ON	OFF		B
	3	H	L	H	L	L	L	L	H	H	L L H H	ON	ON	ON	ON	OFF	OFF	ON	OFF		B
	4	H	L	H	L	L	L	L	H	H	L H L L	OFF	ON	ON	OFF	OFF	ON	ON	OFF		B
	5	H	L	H	L	L	L	L	H	H	L H L H	ON	OFF	ON	ON	OFF	ON	ON	OFF		B
	6	H	L	H	L	L	L	L	H	H	L H H L	ON	ON	OFF	ON	ON	OFF	ON	OFF		B
	7	H	L	H	L	L	L	L	H	H	L H H H	ON	ON	ON	OFF	OFF	OFF	OFF	OFF		B
	8	H	L	H	L	L	L	L	H	H	H L L L	ON	ON	ON	ON	ON	ON	ON	OFF		B
	9	H	L	H	L	L	L	L	H	L	H L L H	ON	ON	ON	ON	OFF	ON	ON	OFF		B
	0	H	L	H	L	L	L	L	H	H	L L L L	ON	ON	ON	ON	ON	ON	OFF	OFF		B, C
	1	H	L	H	L	L	L	L	H	H	L L L H	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF		B
	2	H	L	H	L	L	L	L	H	H	L L H L	ON	ON	OFF	ON	ON	OFF	ON	OFF		B
	3	H	L	H	L	L	L	L	H	H	L L H H	ON	ON	ON	ON	OFF	OFF	ON	OFF		B
	4	H	L	H	L	L	L	L	H	H	L H L L	OFF	ON	ON	OFF	OFF	ON	ON	OFF		B
	5	H	H	H	L	L	L	L	H	H	L H L H	ON	OFF	ON	ON	OFF	ON	ON	OFF		B
Latch	6	H	H	H	L	L	L	L	H	H	L H H L	ON	OFF	ON	ON	OFF	ON	ON	OFF		B
Latch	7	H	H	H	L	L	L	L	H	H	L H H H	ON	OFF	ON	ON	OFF	ON	ON	OFF		B
	8	H	L	H	L	L	L	L	H	H	H L L L	ON	ON	ON	ON	ON	ON	ON	OFF		B
	9	H	L	H	L	L	L	L	H	L	H L L H	ON	ON	ON	ON	OFF	ON	ON	OFF		B
Ripple Blank	0	H	L	L	X	L	L	L	L	H	L L L L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	None	A, B, E

NOTES:
A. $\overline{RBI}/\overline{RBO}$ is wire-AND logic serving as ripple blanking input ($\overline{RBI}$) and/or ripple blanking output ($\overline{RBO}$).
B. The blanking input ($\overline{BI}$) must be low when functions DECIMAL/0 through 20/RIPPLE BLANK are desired.
C. The ripple-blanking input ($\overline{RBI}$) must be open or high to display a zero during the decimal 0 input.
D. When a high logic level is applied directly to the blanking input ($\overline{BI}$) all segment outputs are off regardless of any other input condition.
E. When the ripple-blanking input ($\overline{RBI}$) and outputs Q_A through Q_D are at a low logic level, all segment outputs are off and the ripple-blanking output ($\overline{RBO}$) goes to a low logic level (response condition).

SEGMENT IDENTIFICATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74143N	OBSOLETE	PDIP	N	24		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

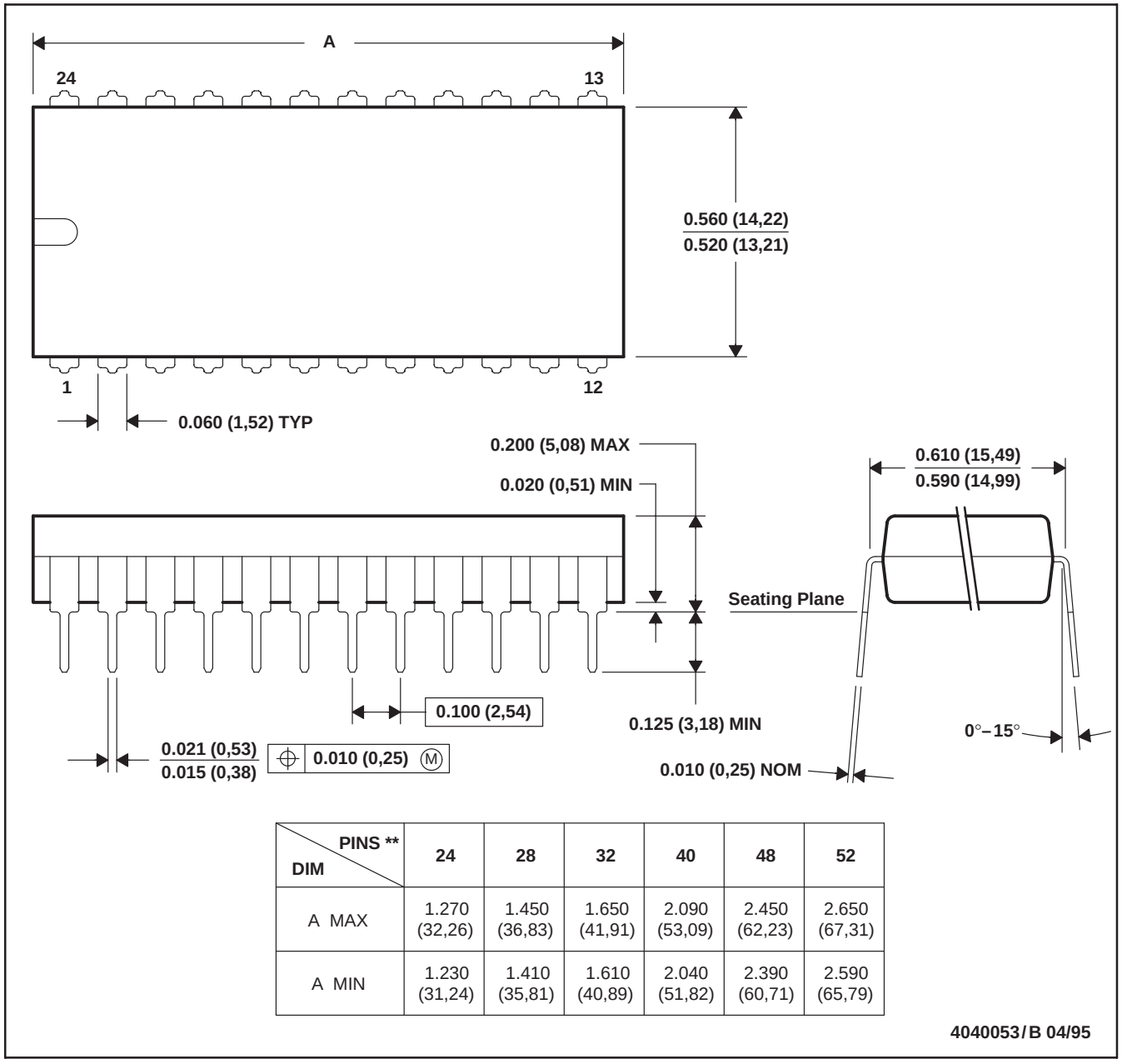
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

MPDI008 – OCTOBER 1994

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

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