CY7C1021BN, CY7C10211BN

1 Mbit (64K x 16) Static RAM

Features

- Temperature ranges
  - Commercial: 0 °C to 70 °C
  - Industrial: –40 °C to 85 °C
  - Automotive-A: –40 °C to 85 °C
  - Automotive-E: –40 °C to 125 °C
- High speed
  - t_{AA} = 10 ns (Commercial)
  - t_{AA} = 15 ns (Automotive)
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Low active power
  - 825 mW (maximum)
- Automatic power down when deselected
- Independent control of upper and lower bits
- Available in Pb-free and non Pb-free 44-pin TSOP II and 44-pin 400-mil-wide SOJ

Functional Description

The CY7C1021BN/CY7C10211BN[1] is a high performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

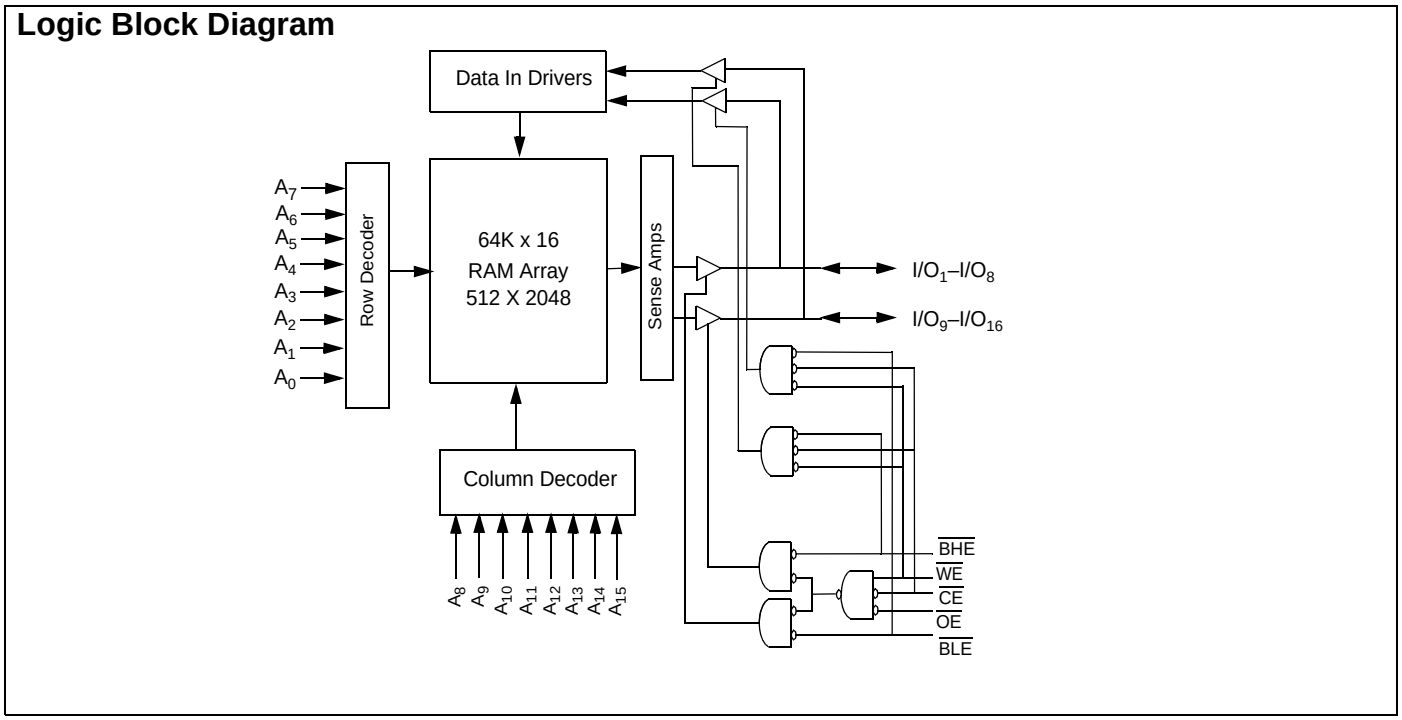
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the input/output (I/O) pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking $\overline{CE}$ and Output Enable ($\overline{OE}$) LOW while forcing $\overline{WE}$ HIGH. If $\overline{BLE}$ is LOW, then data from the memory location specified by the address pins appears on I/O_1 to I/O_8. If $\overline{BHE}$ is LOW, then data from memory appears on I/O_9 to I/O_{16}. See the Truth Table on page 9 for a complete description of read and write modes.

The I/O pins (I/O_1 through I/O_{16}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, $\overline{WE}$ LOW).

The CY7C1021BN/CY7C10211BN is available in standard 44-pin TSOP type II and 44-pin 400-mil-wide SOJ packages. Use part number CY7C10211BN when ordering parts with 10 ns t_{AA} and CY7C1021BN when ordering 12 ns and 15 ns t_{AA}.

Logic Block Diagram



Note

1. For best practice recommendations, refer to the Cypress application note, SRAM System Design Guidelines-AN1064.

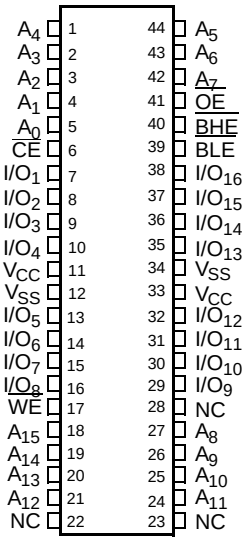
Contents

Selection Guide

Description		CY7C10211B-10	CY7C1021B-12	CY7C1021B-15
Maximum access time (ns)		10	12	15
Maximum operating current (mA)	Commercial/Industrial	150	140	130
	Automotive-A	-	-	130
	Automotive-E	-	-	130
Maximum CMOS standby current (mA)	Commercial/Industrial	10	10	10
	Commercial/Industrial (L version)	0.5	0.5	0.5
	Automotive-A (L version)	-	-	0.5
	Automotive-E	-	-	15

Pin Configuration

Figure 1. 44-Pin SOJ/TSOP II (Top View)



Pin Definitions

Pin Name	Pin Number	I/O Type	Description
A_0–A_{15}	1–5,18–21, 24–27, 42–44	Input	Address inputs used to select one of the address locations.
I/O_1–I/O_{16}	7–10, 13–16, 29–32, 35–38	Input/Output	Bidirectional data I/O lines. Used as input or output lines depending on operation.
NC	22, 23, 28	No Connect	Not connected to the die.
$\overline{WE}$	17	Input/Control	Write enable input, active LOW. When selected LOW, a write is conducted. When deselected HIGH, a read is conducted.
$\overline{CE}$	6	Input/Control	Chip enable input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{BHE}$, $\overline{BLE}$	40, 39	Input/Control	Byte enable select inputs, active LOW. $\overline{BHE}$ controls I/O_{16}–I/O_9, $\overline{BLE}$ controls I/O_8–I/O_1.
$\overline{OE}$	41	Input/Control	Output enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins.
V_{SS}	12, 34	Ground	Ground for the device. Should be connected to ground of the system.
V_{CC}	11, 33	Power Supply	Power supply inputs to the device.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND[2].....–0.5 V to +7.0 V

DC voltage applied to outputs in High Z state[2] .....–0.5 V to V_{CC}+0.5 V

DC input voltage[2].....–0.5 V to V_{CC}+0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage.....>2001 V (per MIL-STD-883, Method 3015)

Latch-up current .....>200 mA

Operating Range

Range	Ambient Temperature (T_A)[3]	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	–40 °C to +85 °C	
Automotive-A	–40 °C to +85 °C	
Automotive-E	–40 °C to +125 °C	

Electrical Characteristics Over the operating range

Parameter	Description	Test Conditions		-10		-12		-15		Unit
				Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	-	2.4	-	2.4	-	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA		-	0.4	-	0.4	-	0.4	V
V_{IH}	Input HIGH voltage			2.2	6.0	2.2	6.0	2.2	6.0	V
V_{IL}	Input LOW voltage[2]			–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}	Commercial/Industrial	–1	+1	–1	+1	–1	+1	µA
			Automotive-A	-	-	-	-	–1	+1	µA
			Automotive-E	-	-	-	-	–4	+4	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{CC}, Output Disabled	Commercial/Industrial	–1	+1	–1	+1	–1	+1	µA
			Automotive-A	-	-	-	-	–1	+1	µA
			Automotive-E	-	-	-	-	–4	+4	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Commercial/Industrial	-	150	-	140	-	130	mA
			Automotive-A	-	-	-	-	-	130	
			Automotive-E	-	-	-	-	-	130	
I_{SB1}	Automatic CE power down current—TTL inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Commercial/Industrial	-	40	-	40	-	40	mA
			Automotive-A	-	-	-	-	-	40	
			Automotive-E	-	-	-	-	-	50	
I_{SB2}	Automatic CE power down current—CMOS inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	Commercial/Industrial	-	10	-	10	-	10	mA
			Commercial/Industrial (L)	-	0.5	-	0.5	-	0.5	
			Automotive-A (L)	-	-	-	-	-	0.5	
			Automotive-E	-	-	-	-	-	15	

Notes
2. V_{IL} (min.) = –2.0 V and V_{IH}(max) = V_{CC} + 0.5 V for pulse durations of less than 20 ns.
3. T_A is the “Instant On” case temperature.

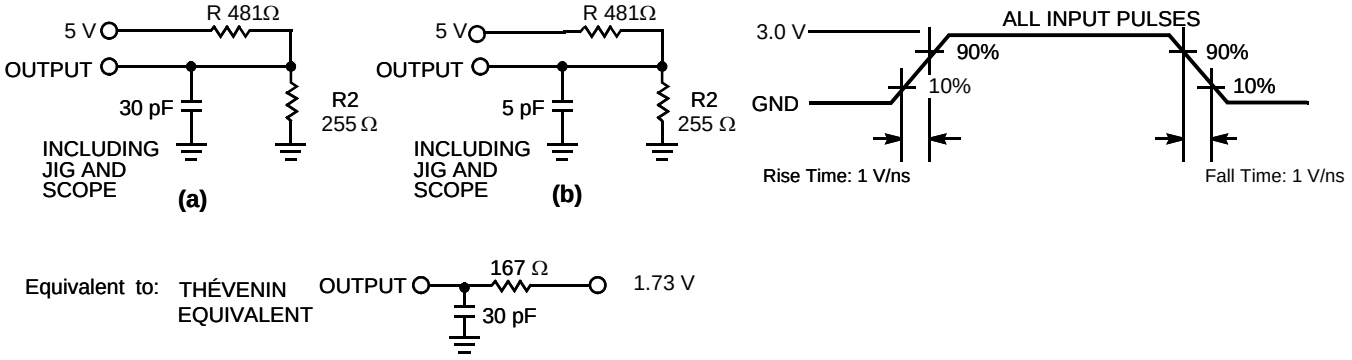
Capacitance

Parameter[4]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	8	pF
C_{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter[4]	Description	Test Conditions	44-Pin SOJ	44-Pin TSOP-II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	64.32	76.89	°C/W
Θ_{JC}	Thermal resistance (junction to case)		31.03	14.28	°C/W

Figure 2. AC Test Loads and Waveforms



Note
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics[5] Over the operating range

Parameter	Description	CY7C10211B-10		CY7C1021B-12		CY7C1021B-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{RC}	Read cycle time	10	-	12	-	15	-	ns
t_{AA}	Address to data valid	-	10	-	12	-	15	ns
t_{OHA}	Data hold from address change	3	-	3	-	3	-	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	-	10	-	12	-	15	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	-	5	-	6	-	7	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z[5]	0	-	0	-	0	-	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z[6, 7]	-	5	-	6	-	7	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z[6]	3	-	3	-	3	-	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z[6, 7]	-	5	-	6	-	7	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	-	0	-	0	-	ns
t_{PD}	$\overline{CE}$ HIGH to power down	-	10	-	12	-	15	ns
t_{DBE}	Byte enable to data valid	-	5	-	6	-	7	ns
t_{LZBE}	Byte enable to low Z[6]	0	-	0	-	0	-	ns
t_{HZBE}	Byte disable to high Z[6, 7]	-	5	-	6	-	7	ns
Write Cycle[8]								
t_{WC}	Write cycle time	10	-	12	-	15	-	ns
t_{SCE}	$\overline{CE}$ LOW to write end	8	-	9	-	10	-	ns
t_{AW}	Address setup to write end	7	-	8	-	10	-	ns
t_{HA}	Address hold from write end	0	-	0	-	0	-	ns
t_{SA}	Address setup to write start	0	-	0	-	0	-	ns
t_{SD}	Data setup to write end	5	-	6	-	8	-	ns
t_{HD}	Data hold from write end	0	-	0	-	0	-	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z[6]	3	-	3	-	3	-	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z[6, 7]	-	5	-	6	-	7	ns
t_{BW}	Byte enable to write end	7	-	8	-	9	-	ns

Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZBE} is less than t_{LZBE}, and t_{HZWE} is less than t_{LZWE} for any device.
7. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW, and $\overline{BHE}$ / $\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$, and $\overline{BHE}$ / $\overline{BLE}$ must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Waveforms

Figure 3. Read Cycle No. 1[9, 10]

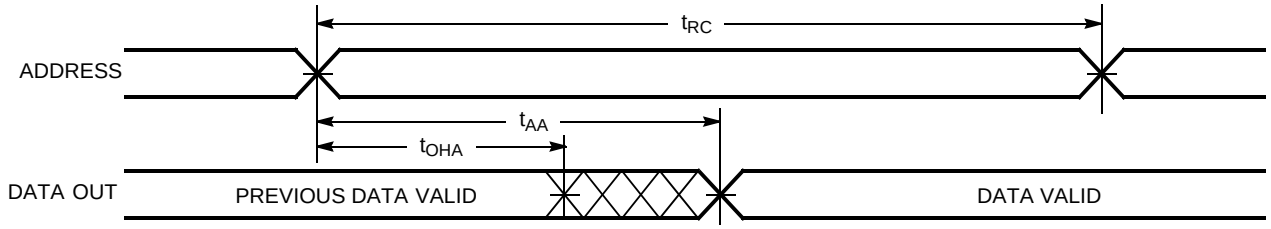
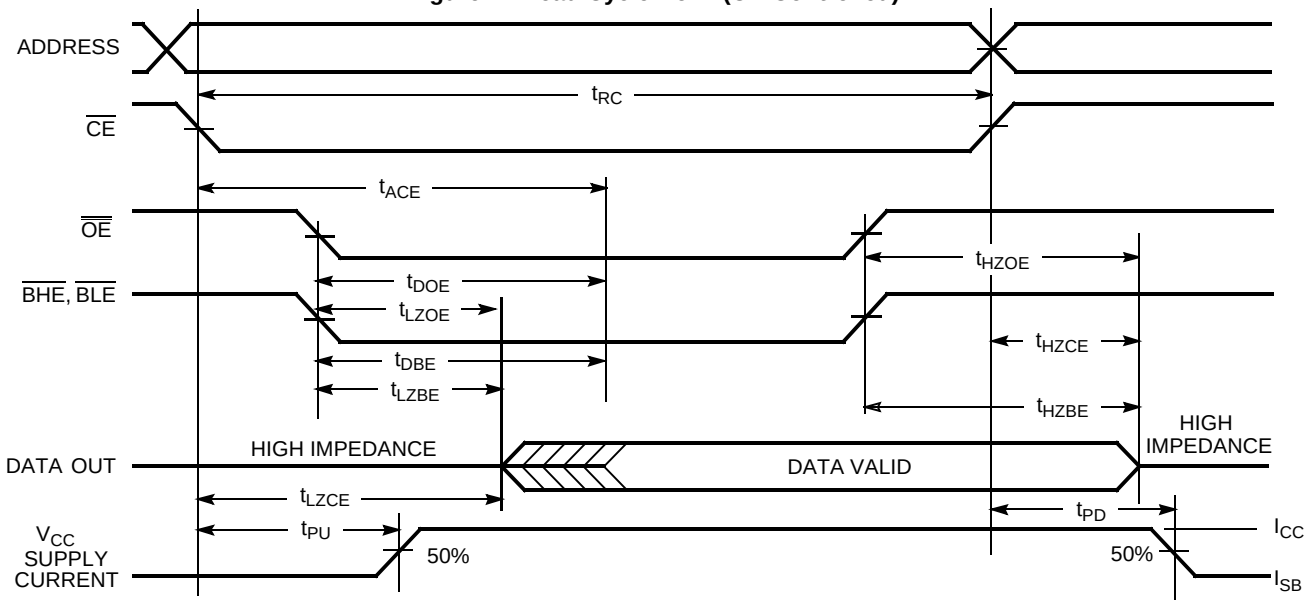


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled)[10, 11]



Notes
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and $\overline{BHE}$ = V_{IL}.
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Figure 5. Write Cycle No. 1 ($\overline{CE}$ Controlled)[12, 13]

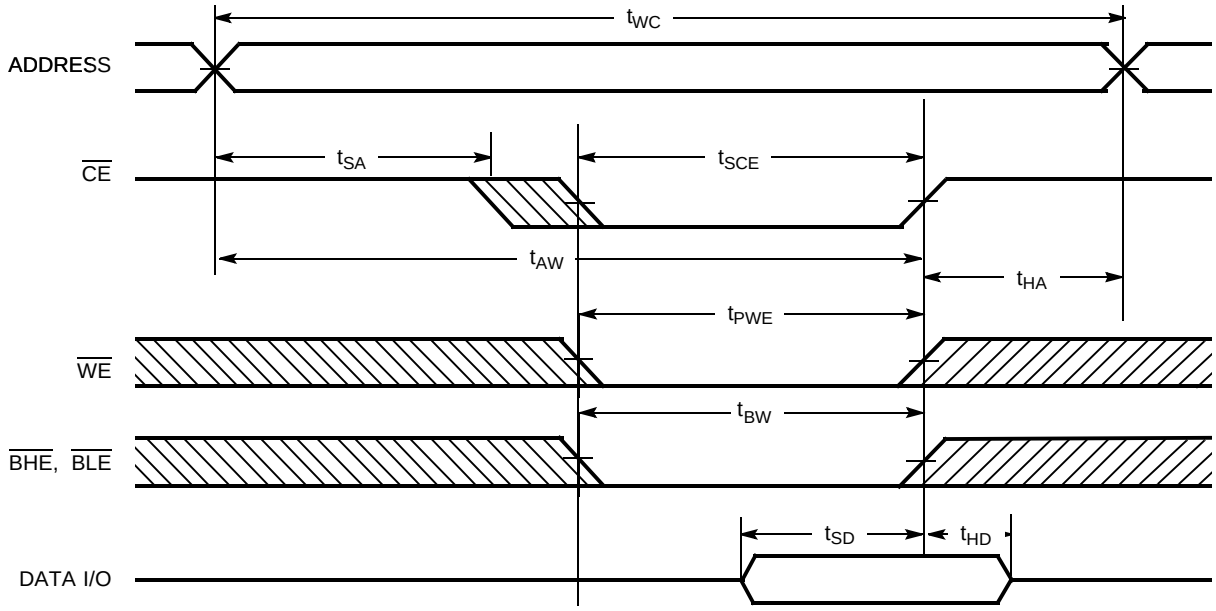
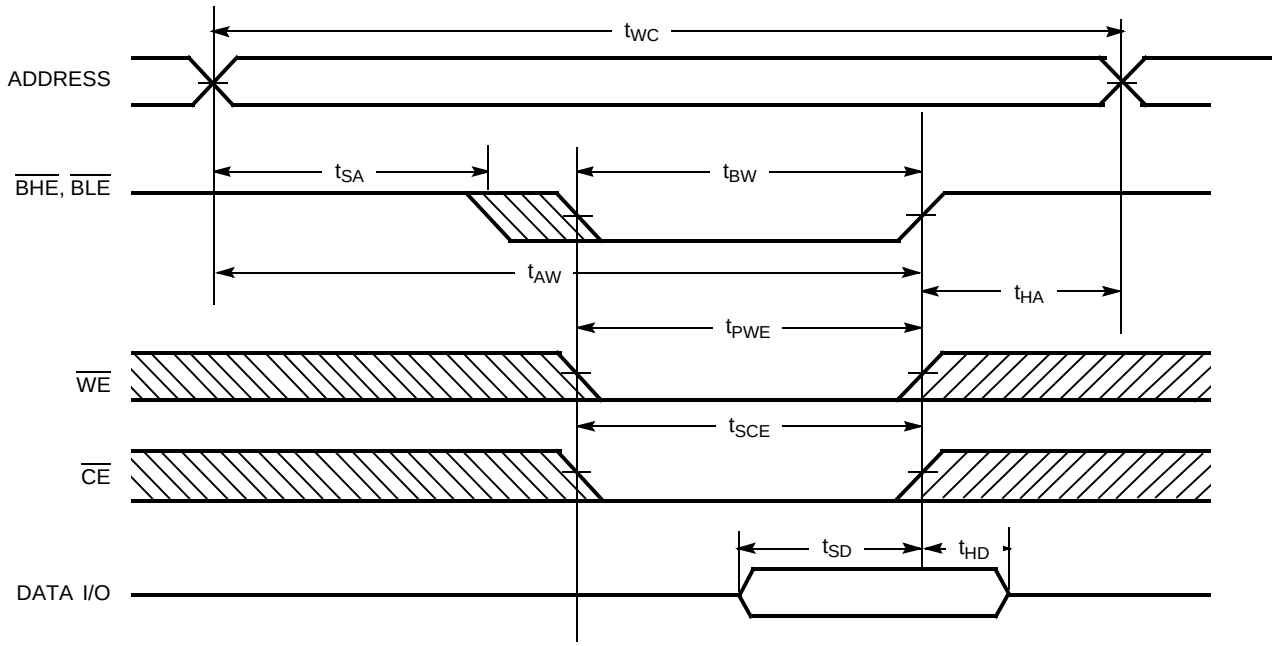
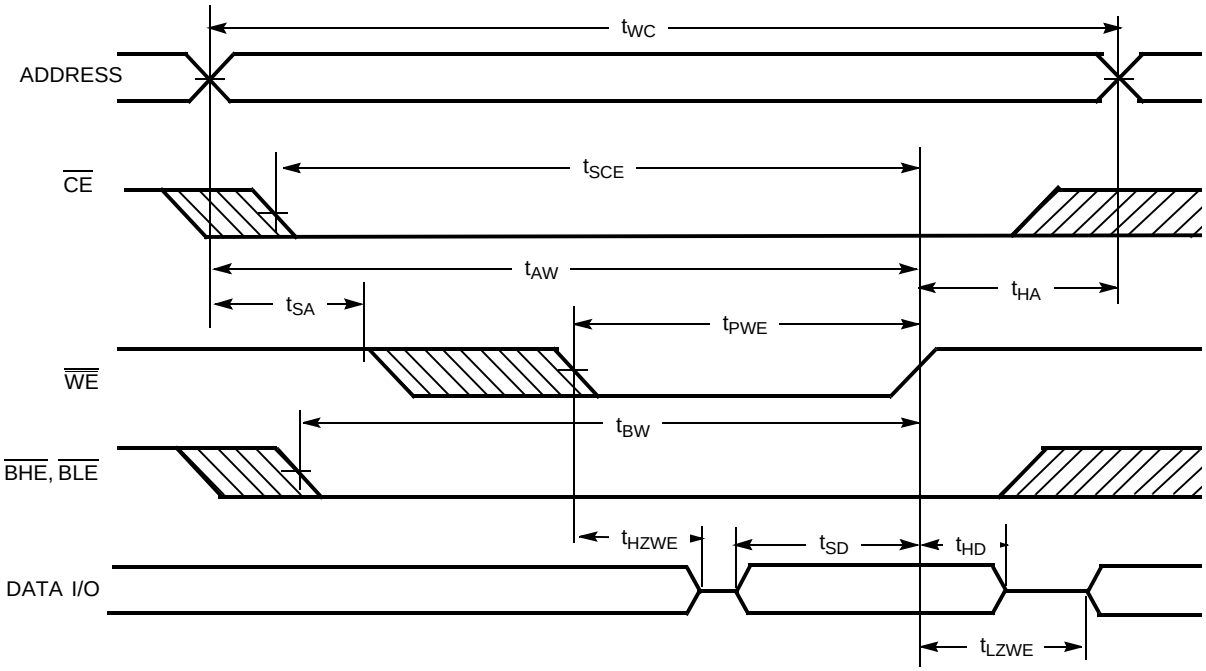


Figure 6. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
12. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= V_{IH}.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Figure 7. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_1–I/O_8	I/O_9–I/O_{16}	Mode	Power
H	X	X	X	X	High Z	High Z	Power down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read - All bits	Active (I_{CC})
			L	H	Data out	High Z	Read - Lower bits only	Active (I_{CC})
			H	L	High Z	Data out	Read - Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write - All bits	Active (I_{CC})
			L	H	Data In	High Z	Write - Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write - Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

Ordering Information

Cypress offers other versions of this product type in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

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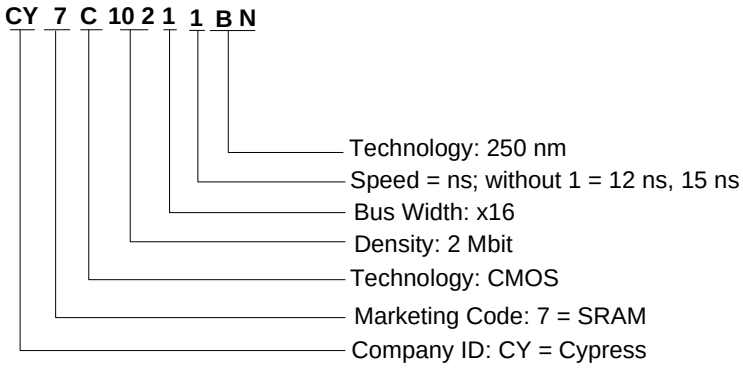
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1021BN-12ZXC	51-85082	44-pin TSOP type II (Pb-free)	Commercial
15	CY7C1021BNL-15VXC	51-85082	44-pin (400-mil) molded SOJ (Pb-free)	Commercial
	CY7C1021BN-15ZXC	51-85087	44-pin TSOP type II (Pb-free)	Commercial
	CY7C1021BN-15ZXI	51-85087	44-pin TSOP type II (Pb-free)	Industrial
	CY7C1021BNL-15ZXI	51-85087	44-pin TSOP type II (Pb-free)	Industrial
	CY7C1021BNL-15ZSXA	51-85087	44-pin TSOP type II (Pb-free)	Automotive-A
	CY7C1021BN-15VXE	51-85082	44-pin (400-mil) molded SOJ (Pb-free)	Automotive-E
	CY7C1021BN-15ZSXE	51-85087	44-pin TSOP type II (Pb-free)	Automotive-E

Ordering Code Definition



Package Diagrams

Figure 8. 44-Pin (400-Mil) Molded SOJ

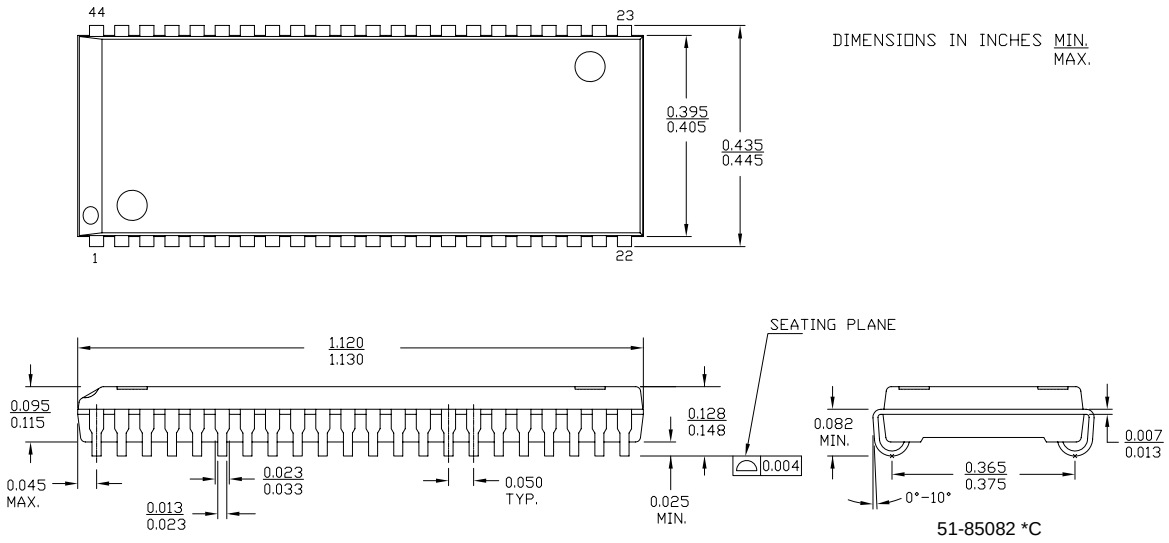
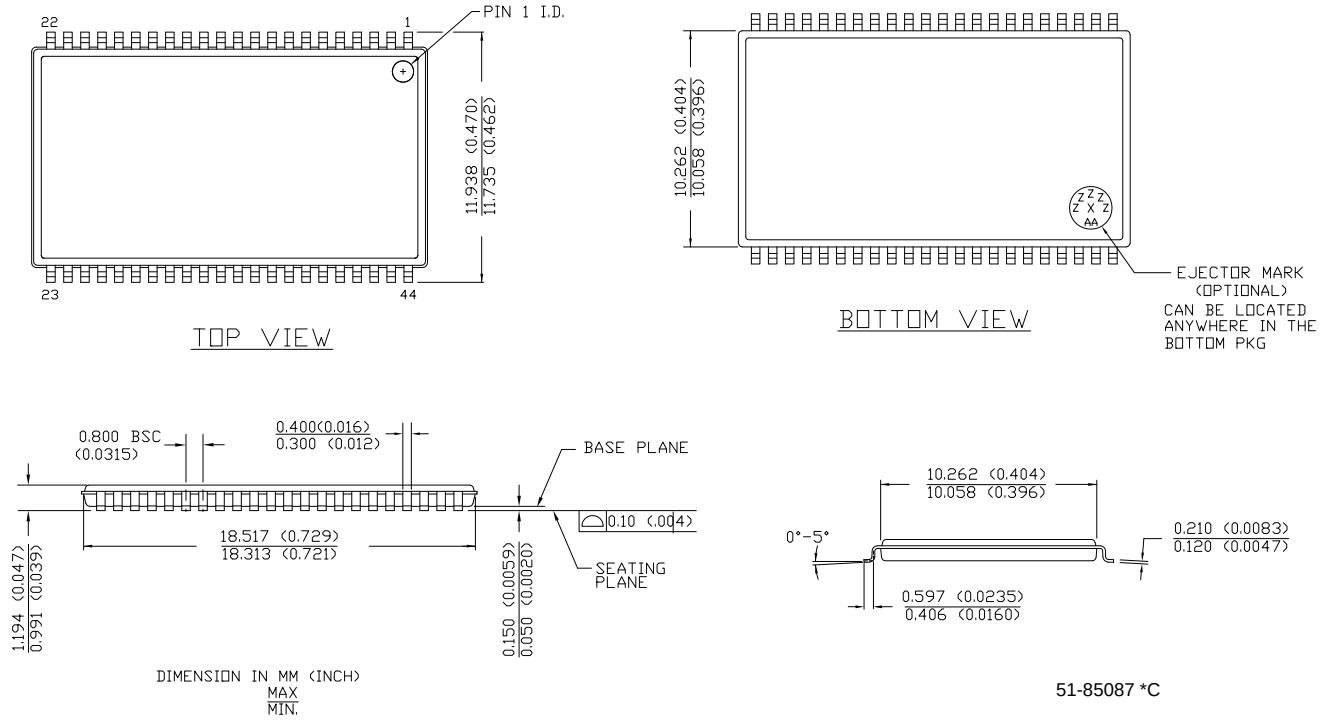


Figure 9. 44-Pin TSOP II



Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
BHE	Byte high enable
BLE	Byte low enable
CE	Chip enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
OE	Output enable
SRAM	Static random access memory
TSOP	Thin small outline package
WE	Write enable

Document History Page

Document Title: CY7C1021BN, CY7C10211BN 1 Mbit (64K x 16) Static RAM Document Number: 001-06494				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	423877	See ECN	NXR	New datasheet
*A	505726	See ECN	NXR	Removed I_{OS} parameter from DC Electrical Characteristics table. Added Automotive products Updated ordering Information table
*B	2897061	03/22/10	AJU	Removed obsolete parts from ordering information table Updated package diagrams
*C	2947254	06/08/10	RAME	Corrected 'Byte write select inputs' to 'Byte Enable select inputs' on page 2. Added ohm (Ω)symbol inThevenin equivalent circuit on page 4. Included T_{HZBE} and T_{LZBE} to Switching Characteristics table footnote 2 Included operating range for CY7C1021BNL-15ZXI in ordering information table.

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