



General Description

- Trench Power AlphaMOS (αMOS LV) technology
- Low $R_{SS(ON)}$
- Fully protected AlphaDFN package
- With ESD protection to improve battery performance and safety
- Common drain configuration for design simplicity
- RoHS and Halogen-Free Compliant

Applications

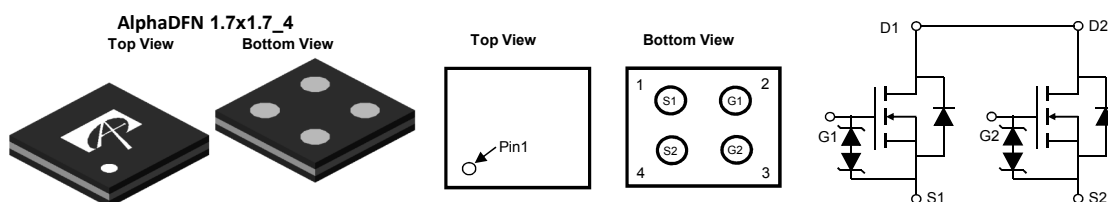
- Battery protection switch
- Mobile device battery charging and discharging

Product Summary

V_{SS}	20V
$R_{SS(ON)}$ (at $V_{GS}=4.5V$)	< 11.9mΩ
$R_{SS(ON)}$ (at $V_{GS}=4.0V$)	< 12.5mΩ
$R_{SS(ON)}$ (at $V_{GS}=3.7V$)	< 14mΩ
$R_{SS(ON)}$ (at $V_{GS}=3.1V$)	< 15.5mΩ
$R_{SS(ON)}$ (at $V_{GS}=2.5V$)	< 20mΩ

Typical ESD protection

HBM Class 3A



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOC2870	AlphaDFN 1.7x1.7_4	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Source-Source Voltage	V_{SS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Source Current(DC) ^{Note1}	I_S	10	A
Source Current(Pulse) ^{Note2}	I_{SM}	50	
Power Dissipation ^{Note1}	P_D	1.4	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typical	Units
Maximum Junction-to-Ambient $t \leq 10s$	$R_{\theta JA}$	81	$^\circ\text{C/W}$
Maximum Junction-to-Ambient Steady-State		90	$^\circ\text{C/W}$

Note 1. I_S rated value is based on bare silicon. Mounted on 70mmx70mm FR-4 board.

Note 2. PW <10 μs pulses, duty cycle 1% max.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{SSS}	Source-Source Breakdown Voltage	I _S =250μA, V _{GS} =0V Test Circuit 6	20			V
I _{SSS}	Zero Gate Voltage Source Current	V _{SS} =20V, V _{GS} =0V Test Circuit 1 T _J =55°C			1 5	μA
I _{GSS}	Gate leakage current	V _{SS} =0V, V _{GS} =±10V Test Circuit 2			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{SS} =V _{GS} , I _S =250μA Test Circuit 3	0.5	0.9	1.3	V
R _{SS(ON)}	Static Source to Source On-Resistance	V _{GS} =4.5V, I _S =3A Test Circuit 4 T _J =125°C	7.0	9.4	11.9	mΩ
			9.8	13.2	16.8	
		V _{GS} =4.0V, I _S =3A Test Circuit 4	7.2	9.8	12.5	mΩ
		V _{GS} =3.7V, I _S =3A Test Circuit 4	7.4	10.2	14.0	mΩ
		V _{GS} =3.1V, I _S =3A Test Circuit 4	8.0	11.1	15.5	mΩ
g _{FS}	Forward Transconductance	V _{SS} =5V, I _S =3A Test Circuit 3		30		S
V _{FSS}	Forward Source to Source Voltage	I _S =1A, V _{GS} =0V Test Circuit 5		0.68	1	V
DYNAMIC PARAMETERS						
R _g	Gate resistance	f=1MHz		2		KΩ
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{G1S1} =4.5V, V _{SS} =10V, I _S =3A		11.5		nC
t _{D(on)}	Turn-On DelayTime	V _{G1S1} =4.5V, V _{SS} =10V, R _L =3.3Ω, R _{GEN} =3Ω Test Circuit8		1.5		μs
t _r	Turn-On Rise Time			3.0		μs
t _{D(off)}	Turn-Off DelayTime			2.0		μs
t _f	Turn-Off Fall Time			6.0		μs

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

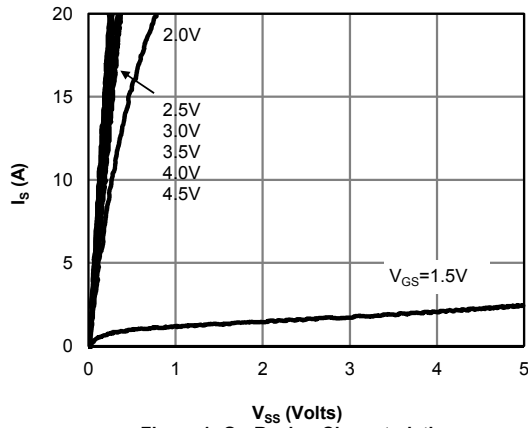


Figure 1: On-Region Characteristics

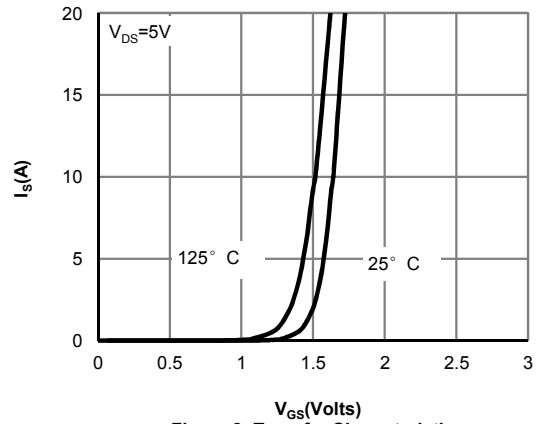


Figure 2: Transfer Characteristics

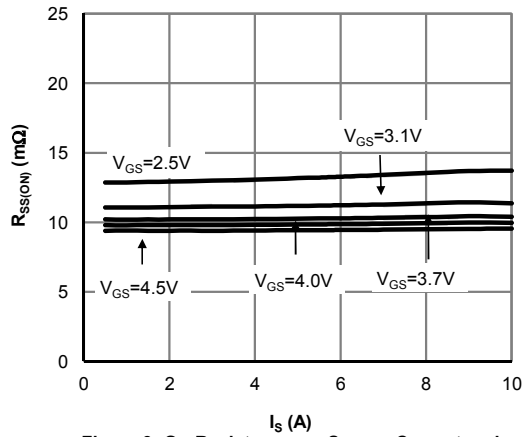


Figure 3: On-Resistance vs. Source Current and Gate Voltage

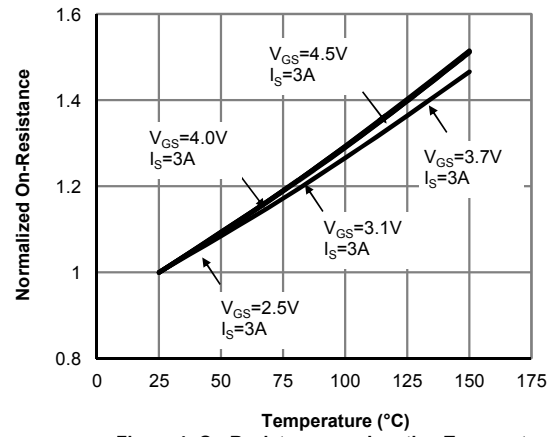


Figure 4: On-Resistance vs. Junction Temperature

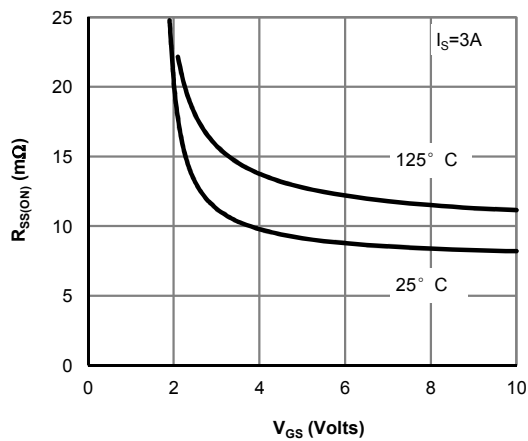


Figure 5: On-Resistance vs. Gate-Source Voltage

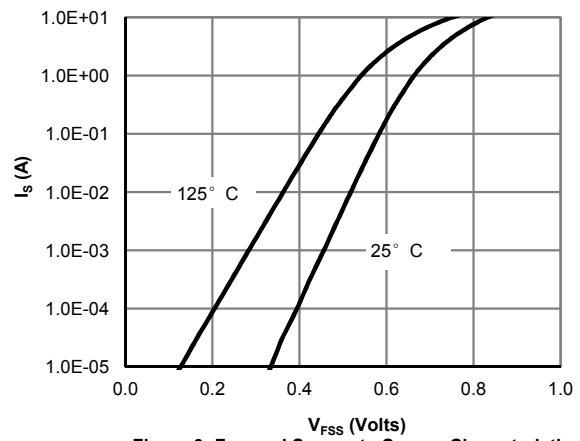


Figure 6: Forward Source to Source Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

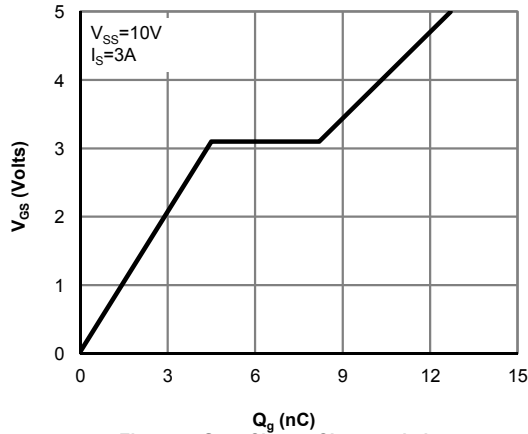


Figure 7: Gate-Charge Characteristics

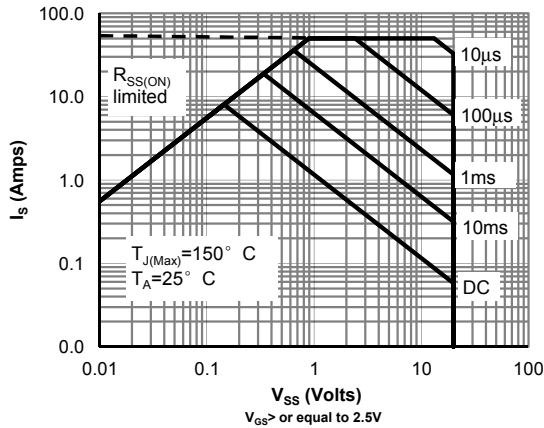


Figure 9: Maximum Forward Biased Safe Operating Area (Note1)

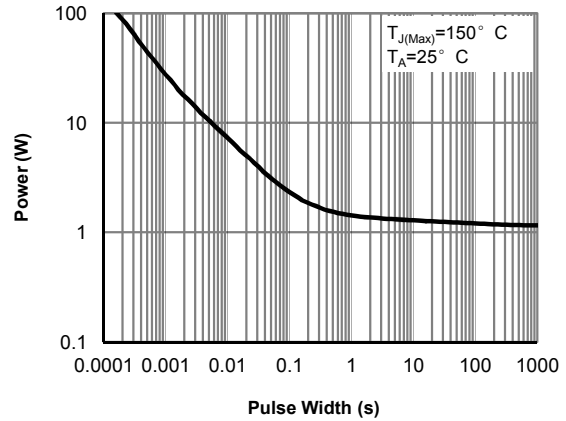


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note1)

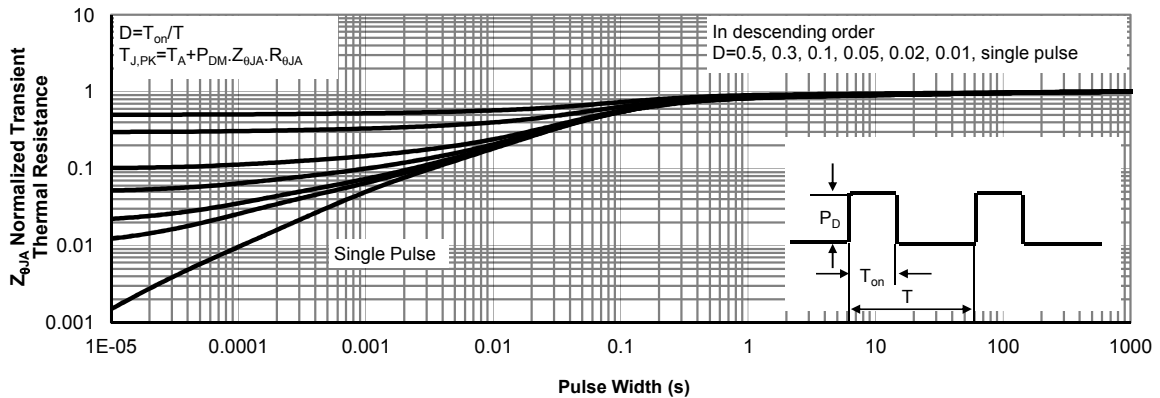
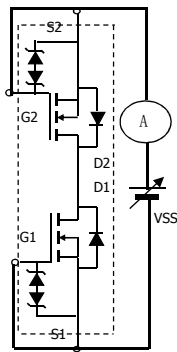


Figure 11: Normalized Maximum Transient Thermal Impedance (Note1)

TEST CIRCUIT 1 I_{SSS}

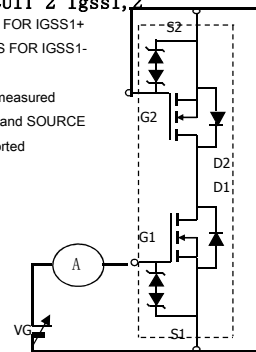
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 2 $I_{gss1,2}$

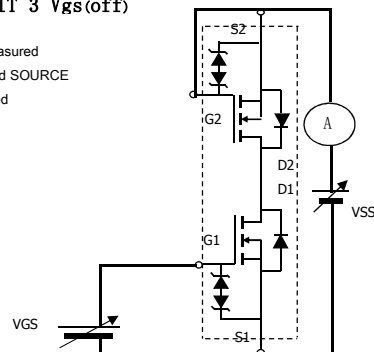
POSITIVE VGS FOR IGSS1+
NEGATIVE VGS FOR IGSS1-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



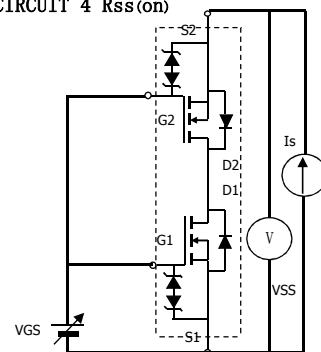
TEST CIRCUIT 3 $V_{gs(off)}$

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



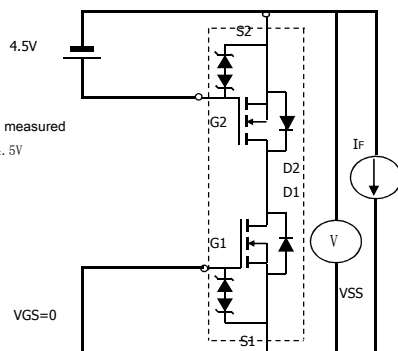
TEST CIRCUIT 4 $R_{ss(on)}$

Vss/Is



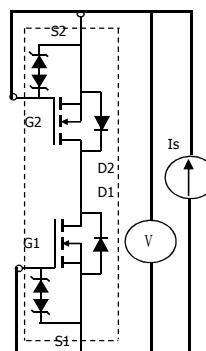
TEST CIRCUIT 5 $V_{F(SS)1,2}$

When FET1 measured
FET2 $V_{GS}=4.5V$



TEST CIRCUIT 6 BV_{DSS}

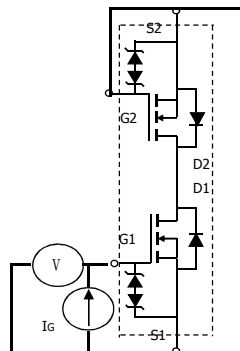
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 7 $BV_{GS01,2}$

POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



TEST CIRCUIT 8

Switching time

