

PM5461-KIT

PAX/PSX/PFX/PFX-I/PFX-L 96/80/64×G3 PCIe® Switch HD Evaluation Kit

Summary

The PSX/PFX/PFX-I/PFX-L 96/80/64×G3 PCIe Switch HD Evaluation Kit evaluates and tests device functionality and measures signal integrity. The kit comes with a PSX Software Development Kit (SDK).

The kit includes the PM8556 PAX 96×G3 that contains a superset of features over and above the PAX, PSX, PFX, PFX-I and PFX-L. For more information, please consult the device specifications. In the context of these device differences, this kit can be used to evaluate the following devices:

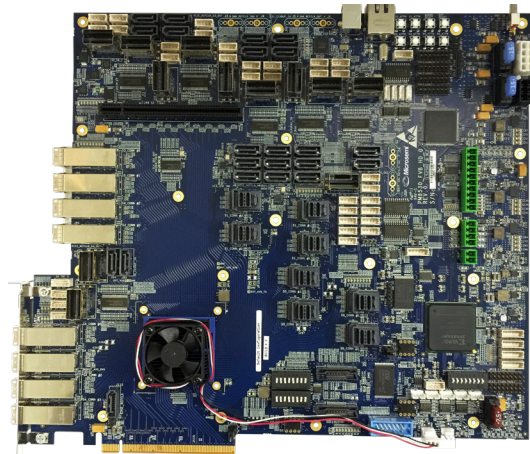
- PM857x PFX-I nxG3 (n = 96, 80, 64, 48, 32, 24) PCIe Gen3 fanout switch
- PM856x PFX-L nxG3 (n = 96, 80, 64, 48, 32, 24) Fanout-Lite PCIe Gen3 switch
- PM855x PAX nxG3 (n = 96, 80, 64, 48, 32, 24) Advanced fabric switch
- PM854x PSX nxG3 (n = 96, 80, 64, 48, 32, 24) PCIe Gen3 storage switch
- PM853x PFX nxG3 (n = 96, 80, 64, 48, 32, 24) PCIe Gen3 fanout switch

The PSX, PFX, PFX-I and PFX-L families of devices are configurable and managed through external interfaces. Each uses an embedded processor running turnkey firmware stored in Flash memory. Enhancements can be provided through firmware updates. The PSX firmware is customizable using the PSX SDK available for download from Microchip. Similarly, the PAX firmware is customizable using the PAX SDK available for download from Microchip.

The kit contains an evaluation card, cables, turnkey firmware and ChipLink diagnostic tools software. ChipLink is a convenient and easy-to-use Windows®/Mac OS®/Linux®-based GUI that provides access to all hardware functions and status information.

The kit operates with a PCIe host and supports the connection of multiple host entities to multiple endpoint devices.

PM5461-KIT



Highlights

PCIe Interface

- 1 ×16 edge connector for connection to a host
- 1 ×16 slot connector for add-in cards

Mini-SAS HD

- 8 SFF-8644 external mini-SAS HD connectors
- 8 SFF-8643 internal mini-SAS HD connectors

PCIe Clock Interface

- Common reference clock with or without spread spectrum clocking (SSC)
- Separate reference clock no SSC (SRNS)
- Separate reference clock with independent SSC (SRIS)

Serial Peripheral Interfaces (SPI)

- 2 quad SPI buses
- 128 Mb on-board SPI Flash for bootup and initialization

Peripheral I/O Interfaces

- 11 two-wire (TWI)/SMBus interfaces
- 128 Kbps EEPROM for storage and PCIe switch configuration
- TWI bus access and connectivity to the temperature sensor, fan controller, voltage monitor, GPIO and TWI expanders, PCIe connectors, iPass Sideband and FPGA
- 109 GPIOs with 3 dedicated as GPIOs and 106 GPIOs are multiplexed to provide TWI, SPI, SGPIO, Ethernet and UART interfaces
- UART access using USB Type B and 3-pin connector header
- 14-pin EJTAG connector header for Green Hills Software probe connectivity
- 10/100 Mbps Ethernet supporting MII and RMII

FPGA and CPLD Functionality

- Drive board status LEDs
- Monitor interrupts from I/O expanders and PCIe SFF cables
- Provide Adaptive Voltage Scaling (AVS) control signal to device and regulators
- Control and monitor power regulator output
- Manage board and switch reset

Local Bus Interface (LBI)—PSX Only

- 4 chip selects mapping to a unique 16 MB memory interface
- 128 Mb of on-board NOR flash memory for storage of firmware image
- 16 Mb of on-board SRAM for extended command/data RAM

Power Supply

- 0.925 V and 1.8 V power rails supplied by on-board regulators
- PCIe switch sense points for monitoring and measuring power rail voltages
- 12V power provided through 8-pin CPU power connector or 6-pin PCIe connector or PCIe edge connector (add-in card)

PSX Software Development Kit

- The PSX software development kit allows development and test of custom PCIe switch functionality
- The PSX SDK relies on the Green Hills MULTI® development environment available directly from Green Hills Software
- The EJTAG debugger supports test and debug of custom PSX firmware

ChipLink Diagnostic Tools

The ChipLink diagnostic tools software provides the following:

- Access to registers in the PCIe switch

Ordering Information

Part Number	Device	Ports	PCIe Connector Interface/PCIe Slot Logical				Max. USP NTB	Max. DSP
			PCIe Edge x16	x16	x8 (x16 Physical Connector)	PCIe HD x4		
PM5461-KIT	96xG3	48	1	1	0	16	48	47

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- Configuration of high-speed analog settings for signal integrity evaluation

- Monitoring of status and mode indicators

Note: For PFX-I, only functional evaluation is possible because commercial temperature parts are populated on the evaluation board.

Kit Contents

The following contents are included with the PM5461-KIT:

- PSX/PFX/PFX-I/PFX-L Gen3 PCIe Switch HD Eval Board
- SFF-8644 (x4) external to SFF-8639 multi-link 1 m cable
- SFF-8643 (x4) internal to SFF-8639 multi-link 1 m cable
- SFF-8644 (x4) external to SFF-8644 (x4) external 1 m cable
- SFF-8643 (x4) internal to SFF-8644 (x4) external 1 m cable
- iPass internal-to-internal 1 m cable and SATA-to-SATA cable
- 3-wire to serial 1 m UART cable
- Evaluation kit software installation files and user's guide
- Power supply and USB-RS232 cable

Kit Requirements (Supplied Separately)

Required for operation of the kit and must be supplied separately:

- Personal computer running Windows, Linux, or Mac OS
- ATX 750 W power supply, 1 x 6-pin PCIe connect and one 8-pin CPU power connector (Microchip recommends a Corsair CX750M ATX power supply)

Optional (Supplied Separately)

The following optional items must be supplied separately:

- NVMe/PCIe SSD
- High-speed oscilloscope for performing eye-diagram measurements
- Jitter analyzer for analyzing jitter components
- For PSX only: Green Hills MULTI development environment and EJTAG debugger for firmware development

Optional Evaluation Kit Adapter Cards

Not included with the kit but available as separate purchases:

- ADP_1x16SLOT_4x4HD: PCIe Gen3 1x16 slot to 4x4 HD
- ADP_EDGE4: PCIe Gen3/Gen4 1x16 Edge to 4x4 OcuLink Adapter Board Converts a x16 Edge PCIe Interface to an OCuLink PCIe interface or vice-versa
- ADP_SLOT4: PCIe Gen3/Gen4 1x16 Slot to 4x4 OcuLink Adapter Board Converts a x16 Slot PCIe Interface to an OCuLink PCIe Interface or vice-versa