

MSKSEMI

SEMICONDUCTOR



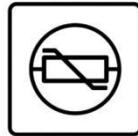
ESD



TVS



TSS



MOV

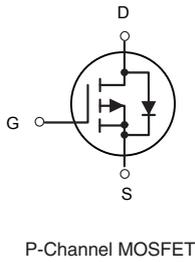
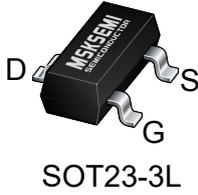


GDT



PLED

Product data sheet



Description

The SI2333CDS-T1-MS uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = -18V, I_D = -7A$

$R_{DS(ON)} < 22m\Omega @ V_{GS}=4.5V$

Application

- High power and current handling capability
- Lead free product is acquired
- Surface mount package
- PWM applications
- Load switch
- Power management

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	-18	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current-Continuous	-7	A
I_{DM}	Drain Current-Pulsed ^(Note 1)	-18.8	A
P_D	Maximum Power Dissipation	1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient ^(Note 2)	125	$^\circ C/W$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-18	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.01	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-4.5V, I _D =-6.5A	---	18	22	mΩ
		V _{GS} =-2.5V, I _D =-5A	---	25	39	
		V _{GS} =-1.8V, I _D =-1.5A	---	---	---	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-0.6	-0.8	-1.4	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	---	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-20V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-16V, V _{GS} =0V, T _J =55°C	---	---	---	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±12V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-3A	---	10	---	S
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-10V, V _{GS} =-4.5V, I _D =-6.5A	---	10	---	nC
Q _{gs}	Gate-Source Charge		---	1.5	---	
Q _{gd}	Gate-Drain Charge		---	3	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-10V, V _{GS} =-4.5V, R _G =6.0Ω I _D =-1A	---	30	---	ns
T _r	Rise Time		---	25	---	
T _{d(off)}	Turn-Off Delay Time		---	70	---	
T _f	Fall Time		---	50	---	
C _{iss}	Input Capacitance	V _{DS} =-10V, V _{GS} =0V, f=1MHz	---	1210	---	pF
C _{oss}	Output Capacitance		---	310	---	
C _{rss}	Reverse Transfer Capacitance		---	290	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	-7.0	A
I _{SM}	Pulsed Source Current ^{2,4}		---	---	-18.8	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1	V
t _{rr}	Reverse Recovery Time	I _F =-4A, dI/dt=100A/μs, T _J =25°C	---	52	---	nS
Q _{rr}	Reverse Recovery Charge		---	28	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
3. The power dissipation is limited by 150°C junction temperature
4. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

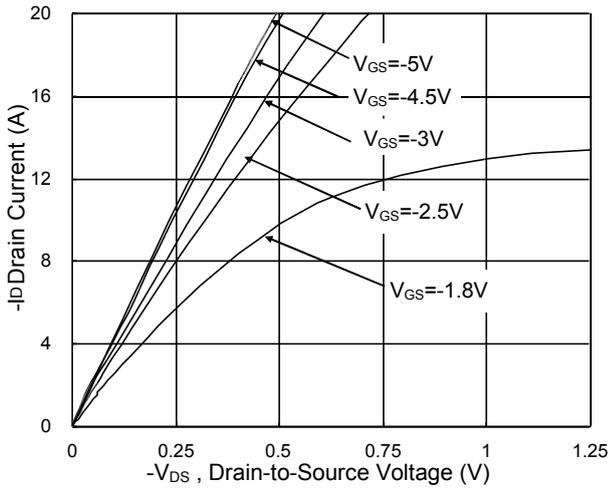


Fig.1 Typical Output Characteristics

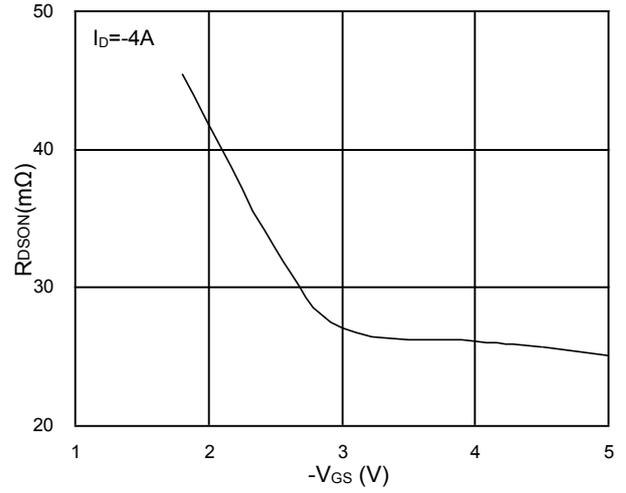


Fig.2 On-Resistance vs. Gate-Source

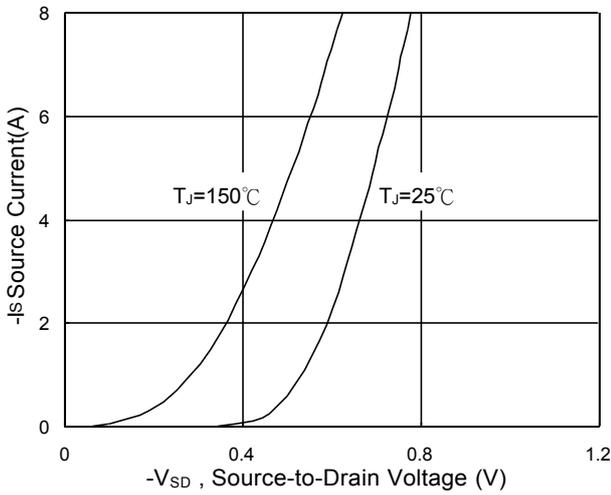


Fig.3 Forward Characteristics Of Reverse

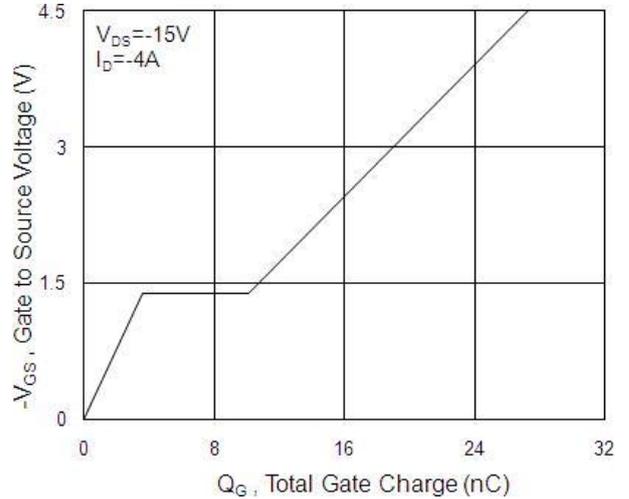


Fig.4 Gate-Charge Characteristics

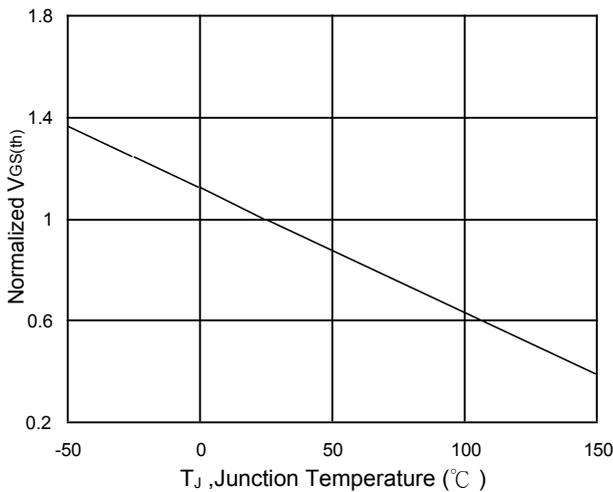


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

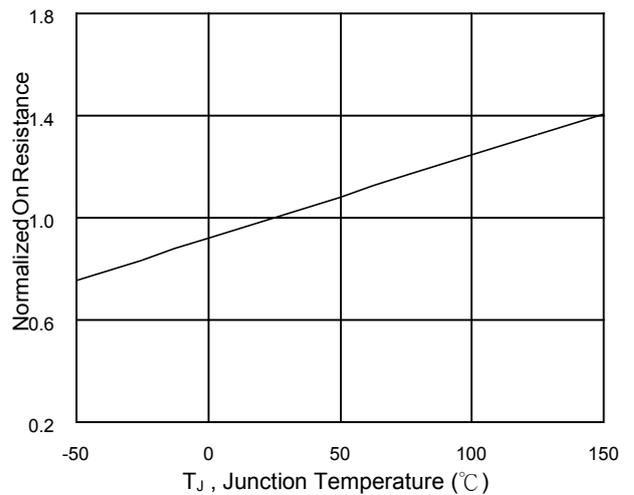


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

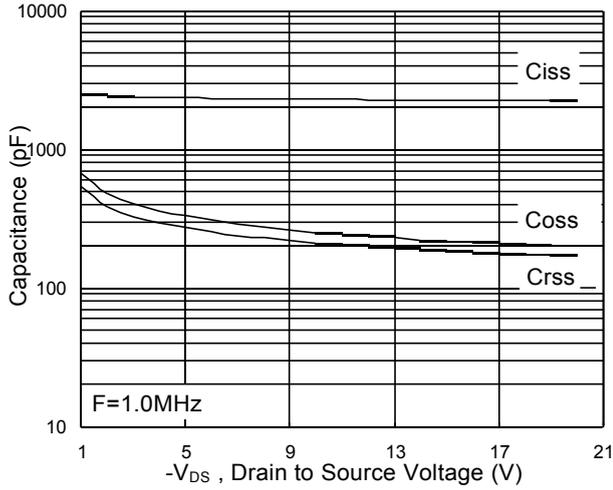


Fig.7 Capacitance

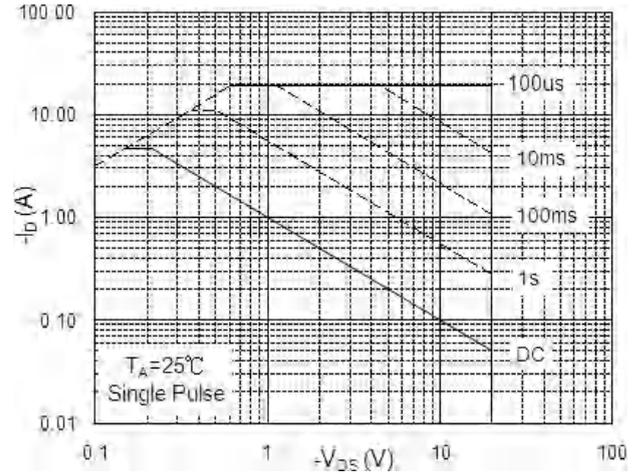


Fig.8 Safe Operating Area

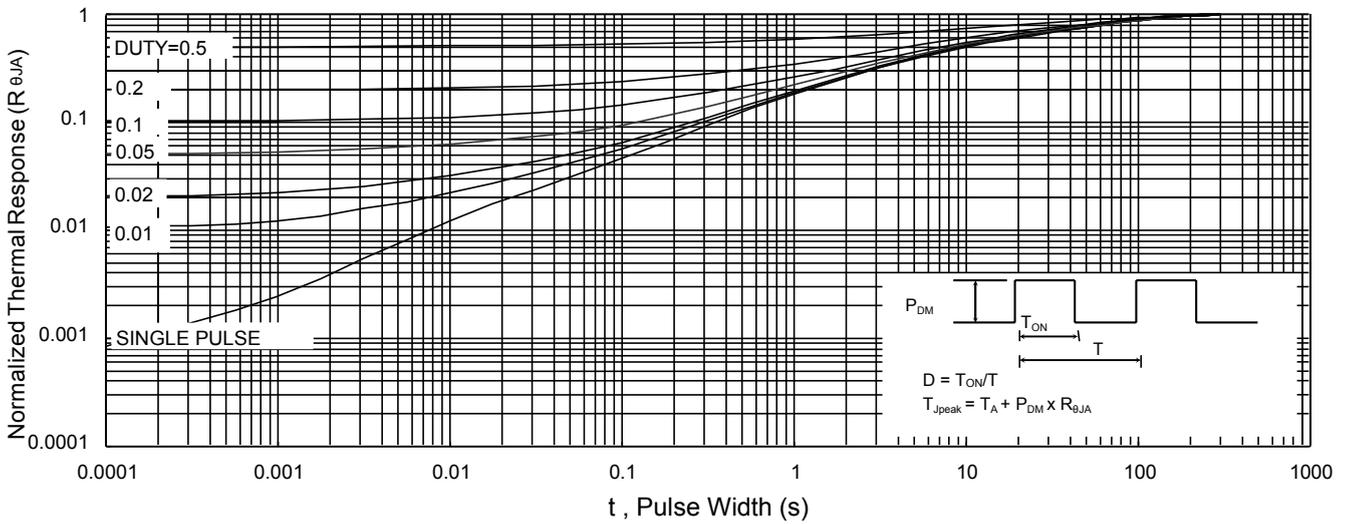


Fig.9 Normalized Maximum Transient Thermal Impedance

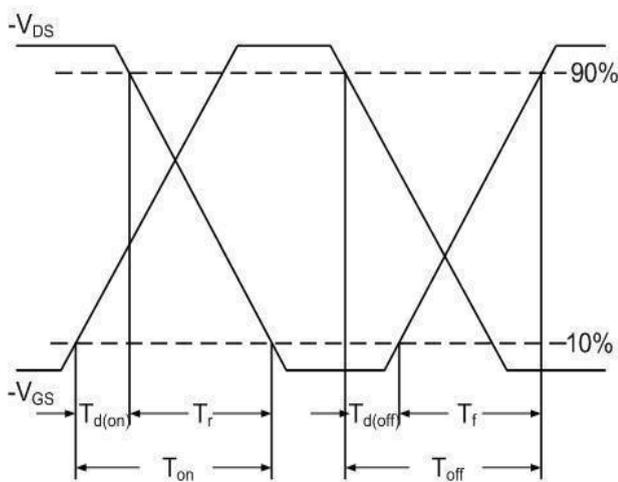


Fig.10 Switching Time Waveform

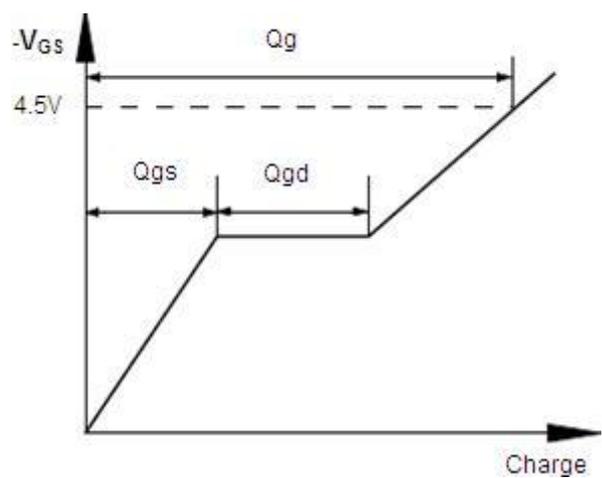
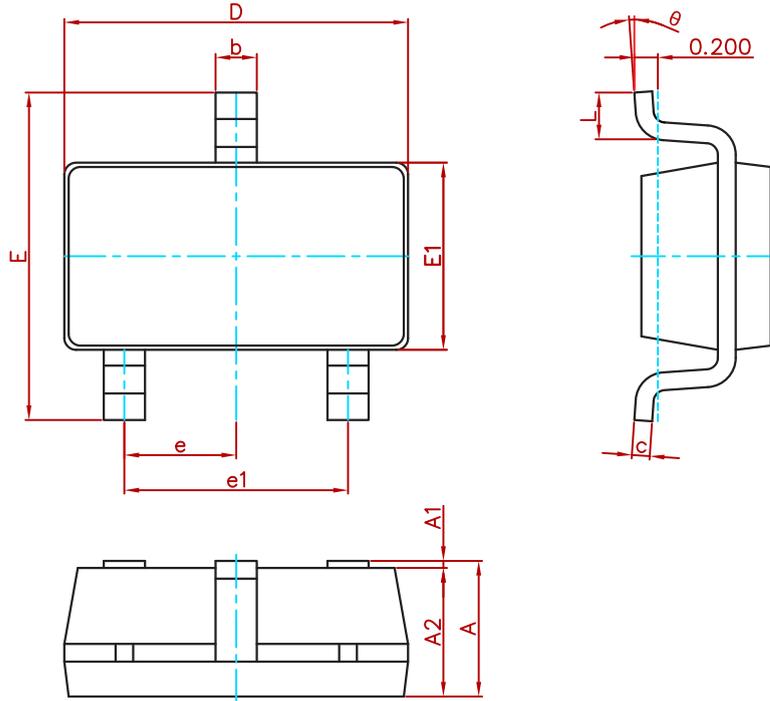


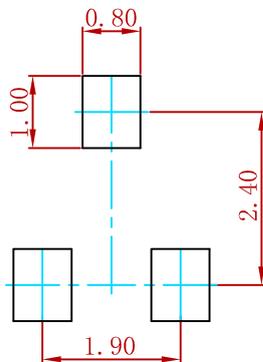
Fig.11 Gate Charge Waveform

PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Suggested Pad Layout



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.

REEL SPECIFICATION

P/N	PKG	QTY
SI2333CDS-T1-MS	SOT-23-3L	3000

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