AOTE SEMICONDUCTOR

智能栅极驱动光耦
Gate Drive OptocoupIer

AT316J

product Data Sheet

AOTE DCC
RELEASE

台湾奥特半导体科技有限公司

TAIWAN AOTE SEMICONDUCTOR TECHNOLOGY CO.,LTD

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概述 Description

AT316J 是一款高度集成的功率控制器件 ，它将具有故障保护和反馈的完整、 隔离的 IGBT 门极驱动电路所需的所有组件集成到一个 SOP16 封装中。TTL 输入逻辑电平允许与微控制器直接接口 ，光隔离功率输出级可驱动 150A/1200V 的 IGBTs。输出 IC 为 IGBT 提供局部保护 ，以防止过流期间产生损坏 ，第二个光链路为微控制器提供完全隔离的故障状态反馈信号。 内置“看门狗”电路监测电源电压 ，以防止 IGBT 出现栅极驱动电压不足的现象。这种集成 IGBT 栅极驱动器旨在提高电机驱动器的性能和可靠性。

The AT316J is a highly integrated power control device that incorporates all the necessary components for a complete, isolated IGBT gate drive circuit with fault protection and feedback into one SOP16 package.TTL input logic levels allow direct interface with a microcontroller, and an optically isolated power output stage drives IGBTs with power ratings of up to 150 A and 1200 V. An output IC provides local protection for the IGBT to prevent damage during over currents, and a second optical link provides a fully isolated fault status feedback signal for the microcontroller. A built in “watchdog” circuit monitors the power stage supply voltage to prevent IGBT caused by insufficient gate drive voltages. This integrated IGBT gate driver is designed to increase the performance and reliability of a motor drive.

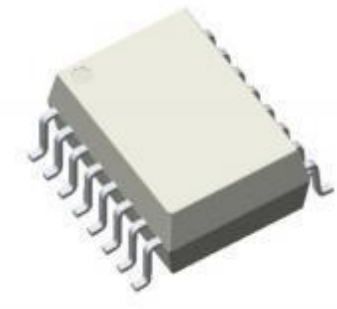
特性 Features

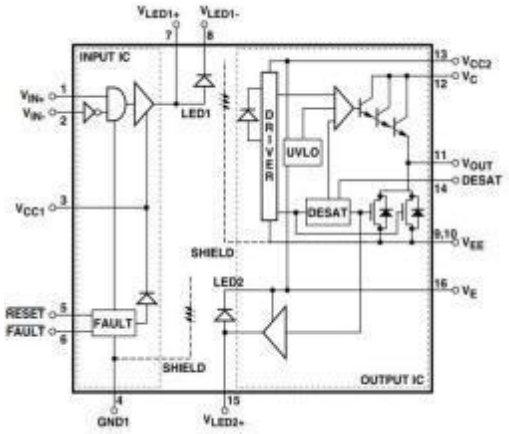
- 最大峰值输出电流: 2.5A
  2.5 A maximum peak output current
- ICBTs 驱动高达 I_C = 150 A, V_{CE} = 1200 V
  Drive IGBTs up to I_C = 150 A, V_{CE} = 1200 V
- 光隔离 ，故障状态反馈
  Optically isolated, FAULT status feedback
- $I_{DD(MAX)}$ <5mA 最大脉冲宽度失真(PWD
  $I_{DD(MAX)}$ < 5mA maximum pulse width distortion (PWD)
- CMOS / TTL 兼容
  CMOS/TTL compatible
- 最大传播延迟为 500ns
  500ns maximum propagation delay
- IGBT 软关断
  “Soft” IGBT turn-off
- 集成故障安全 IGBT 保护
  Integrated fail-safe IGBT protection
  — Desat (V_{CE})检测
  — Desat (V_{CE}) detection
  —低电压锁定保护(UVLO)
  — Under Voltage Lock-Out protection (UVLO)
- 宽工作 V_{CC} 范围:15 至 30V
  Wide operating V_{CC} range: 15 to 30 Volts
- 工作温度 :-40。C ~ +110。C
  Operating Temperature: -40。C to +110。C
- V_{CM} = 1500V 时 ，共模抑制最小值为 15 kV/μs(CMR)
  15 kV/μs minimum Common Mode Rejection (CMR) atV_{CM} = 1500V
- 输入输出瞬时耐受电压:V_{ISO} =5000 V_{rms}
  Input-Output Momentary Withstand Voltage: V_{ISO} =5000

应用 APPIications

- 隔离 IGBT/功率 MOSFET 栅极驱动
  Isolated IGBT/Power MOSFET gate drive
- 交流和无刷式直流电机驱动器
  AC and brushless DC motor drive
- 可再生能源逆变器
  Renewable energy inverters
- 工业逆变器
  Industrial inverter
- 感应加热
  Induction heating
- 开关式电源(SMPS)
  Switch Mode Power Supply (SMPS)
- 不间断电源(uPS)
  uninterruptible power supply (uPS)

封装和原理图 package and schematic Diagram





引脚说明 pin Description

脚 pin	符号 symbol	描述 Description	
1	VIN+	非反相门驱动电压输出(VOUT)控制输入	Noninverting gate drive voltage output (VOUT) control input
2	VIN-	反相门驱动电压输出(VOUT ）控制输入	Inverting gate drive voltage output (VOUT) control input
3	VCC1	正向输入电源电压。(4.5 V 至 5.5 V)	positive input supply voltage. (4.5 V to 5.5 V)
4	GND1	输入地	Input Ground
5	$\overline{\text{RESET}}$	FAULT 复位输入。逻辑低输入至少 0.1μs ，异步复位 FAULT 输出高 ，并启用 VIN。需要同步控制 RESET 相对于 VIN。RESET 不受 UVLO 影响。在 VOUT 高时断言 RESET 不会影响 VOUT。	$\overline{\text{FAULT}}$ reset input. A logic low input for at least 0.1 μs , asynchronously resets FAULT output high and enables VIN. Synchronous control of RESET relative to VIN is required. RESET is not affected by UVLO. Asserting RESET while VOUT is high does not affect VOUT.
6	$\overline{\text{FAULT}}$	错误输出。当 DESAT 脚超出内部参考电压 7V 时 ，FAULT 脚将输出一个集电极开路的信号 ，在 5us 内 FAULT 脚将从高阻状态转变成一个逻辑低电平。FAULT 输出一直很低 ，直到 RESET 值降低。AT316J 的 FAULT 输出是一个集电极开路 ，在同一电路的单个的 FAULT 脚以 “或” 逻辑连接成一条母线到单片机。	$\overline{\text{FAULT}}$ output. $\overline{\text{FAULT}}$ changes from a high impedance state to a logic low output within 5μs of the voltage on the DESAT pin exceeding an internal reference voltage of 7V. $\overline{\text{FAULT}}$ output remains low until RESET is brought low. $\overline{\text{FAULT}}$ output is an open collector which allows the FAULT outputs from all AT316J in a circuit to be connected together in a “wired OR” forming a single fault bus for interfacing directly to the micro-controller.
7	VLED1+	LED1 阳极。为了保证数据手册的性能 ，此引脚必须保持不连接。(仅用于光耦测试)	LED1 anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only.)
8	VLED1-	LED1 阴极。该引脚必须与接地相连接。	LED1 cathode. This pin must be connected to ground.
9	VEE	输出电源电压	Output supply voltage
10	VEE	输出电源电压	Output supply voltage
11	VOUT	栅极驱动电压输出	Gate drive voltage output
12	VC	输出电源电压。	positive output supply voltage
13	VCC2	正输出电源电压	positive output supply voltage
14	DESAT	去饱和电压输入引脚。当 DESAT 脚电压在 IGBT 导通时超过内部参考电压 7V ，故障输出端将在 5us 内从高阻状态转变成一个逻辑低电平。	Desaturation voltage input. when the voltage on DESAT exceeds an internal reference voltage of 7V while the IGBT is on , FAULT output is changed from a high impedance state to a logic low state within 5 μs.
15	VLED2+	LED2 阳极。为了保证数据手册的性能 ，此引脚必须保持不连接。(仅用于光耦测试)	LED2 anode. This pin must be left unconnected for guaranteed data sheet performance. (For optical coupling testing only.)
16	VE	公共(IGBT 发射极)输出电源电压。	Common (IGBT emitter) output supply voltage

产品型号命名规则 Order code

AT 316J - UNY - W (V) (ZZ)

① ② ③ ④ ⑤ ⑥ ⑦

① 公司代码 company code（AT：奥特 AOTE ）

② 产品系列 product series（316J：316J ）

③ 框架类型 Lead Frame（cu：铜框架 copper ）

④ 树脂类型 EpoXy Type（H：无卤 Halogen-free，L：有卤/无铅 Halogen/Lead-free ）

⑤ 封装形式 package（s：sOp ）

⑥ 器件工作温度范围 Device Operating Temperature Range（特殊范围需填或者空白 special Range need to be filled in or left blank）

⑦ 内部补充代码 Internal supplementary code（数字或者空白 Number or None ）

印字信息 Marking Information

. 印字中“ ”为奥特品牌
LOGO “ ” denotes LOGO

. 印字中“y”代表年份 :A(2018)，B(2019)，c(2020)…… “y” denotes yEAR:A(2018)，B(2019)，c(2020)……

. 印字中“ww”代表周号
“ww” denotes week,s number

. 印字中“E”代表内部代码
“E” denotes Internal code

. 印字中的“H”代表无卤 ,而当产品有卤/无铅时 ,此 处空白
“H” denotes Halogen-free, when the product has halogen/lead-free, leave this blank.

绝缘和安规信息 InsuIation and safety reIated specifications

项目 Item	符号 Symbol	数值 Value	单位 Unit	备注 Remark
爬电距离 creepage Distance	L	8.3	mm	从输入端到输出端 ,沿本体最短距离路径 Measured from input terminals to output terminals, shortest distance path along body.
电气间隙 clearance Distance	L	8.3	mm	从输入端到输出端 ,通过空气的最短距离 Measured from input terminals to output terminals, shortest distance through air.
绝缘距离 Insulation Thickness	DTI	0.5	mm	发射器和探测器之间的绝缘厚度 Insulation thickness between emitter and detector.
峰值隔离电压 peak Isolation voltage	V_{IORM}	1500	V_{peak}	IEc/EN/DIN EN60747-5-5.
瞬态隔离电压 Transient Isolation voltage	V_{IOTM}	8000	V_{peak}	IEc/EN/DIN EN60747-5-5.
隔离电压 Isolation voltage	V_{ISO}	5000	V_{rms}	For 1 minute.

极限参数 AbsoIute Maximum Ratings (T_A =25τ unIess otherwise specified)

参数 Parameter	符号 Symbol	最小值 Min	最大值 Max.	单位 Unit
储存温度 storage Temperature	T_S	-55	125	℃
工作温度 operating Temperature	T_A	-40	110	
输出 Ic 结温度 output Ic Junction Temperature	T_J	-40	125	
峰值输出电流 peak output current	$I_{o(peak)}$	-	2.5	A
故障输出电流 Fault output current	I_{FAULT}	-	10	mA
正输入电源电压 positive Input supply voltage	V_{CC1}	-0.5	5.5	v
输入引脚电压 Input pin voltages	V_{IN+}, V_{IN-} and V_{RESET}	-0.5	5.5	
总输出电源电压 Total output supply voltage	(V_{CC2} - V_{EE})	-0.5	30	
反向输出电源电压 Negative output supply voltage	(V_E - V_{EE})	-0.5	15	
正向输出电源电压 positive output supply voltage	(V_{CC2} - V_E)	-0.5	35 - (V_E - V_{EE})	
栅极驱动输出电压 Gate Drive output voltage	$V_{o(peak)}$	-0.5	V_{CC2}	
集电极电压 collector voltage	V_C	V_{EE} + 5 v	V_{CC2}	
DEsAT 电压 DEsAT voltage	V_{DESAT}	V_E	V_E + 10	

参数 Parameter	符号 Symbol	最小值 Min	最大值 Max.	单位 Unit
输出 IC 功率耗散 output IC Power Dissipation	P_o	-	600	mw
输入 IC 功率耗散 Input IC Power Dissipation	P_I	-	150	mw

推荐的操作条件 Recommended operating conditions

参数 Parameter	符号 Symbol	最小值 Min	最大值 Max.	单位 Unit
工作温度 operating Temperature	T_A	-40	+110	℃
输入电源电压 Input supply Voltage	V_{CC1}	4.5	5.5	V
总输出电源电压 Total output supply Voltage	(V_{CC2} - V_{EE})	15	30	
负输出电源电压 Negative output supply Voltage	(V_E - V_{EE})	-0.5	15	
正输出电源电压 Positive output supply Voltage	(V_{CC2} - V_E)	-0.5	30 - (V_E - V_{EE})	
集电极电压 Collector Voltage	V_C	V_{EE} + 6	V_{CC2}	
峰值高电平输出电流 Peak high-level output current	I_{OPH}	-	2.5	A
峰值低电平输出电流 Peak low-level output current	I_{OPL}	-	2.5	A
DEsAT 电压 DEsAT Voltage	V_{DEsAT}	V_E	V_E + 10	V
输出 IC 功率散 output IC Power Dissipation	P_o	-	600	mw
工作频率 operating frequency	f	-	50	KHz

产品特性参数 EIectro-opticaI Characteristics (DC)

除非另有说明 ，典型值测量值在 T_A = 25。C, V_{CC1} = 5 V, and V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V 测得;
所有的最小/最大规格遵照推荐工作条件。
Unless otherwise noted, all typical values at T_A = 25。C, V_{CC1} = 5 V, and V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V;
All Minimum/Maximum specifications are at Recommended Operating Conditions.

参数 Parameter	符号 Symbol	条件 Condition	最小 Min.	典型 Typ.	最大 Max.	单位 Unit	备注 Note
逻辑低输入电压 Logic Low Input Voltages	V_{IN+L}, V_{IN-L} V_{RESETL}	-	-	-	0.8	V	-
逻辑高输入电压 Logic High Input Voltages	VI_{N+H}, V_{IN-H} V_{RESETH}	-	2.0	-	-		-
逻辑低输入电流 Logic Low Input Current	I_{IN+L}, I_{IN-L} I_{RESETH}	V_{IN} = 0.4 V	-0.5	-0.4	-	mA	-
故障逻辑低输出电流 FAULT Logic Low Output Current	$I_{\overline{FAULTL}}$	V_{FAULT} = 0.4 V	5.0	12	-		25
故障逻辑高输出电流 FAULT Logic High Output Current	$I_{\overline{FAULTH}}$	V_{FAULT} = V_{CC1}	-40	-	-	μA	26
高电平输出电流 High Level Output Current	I_{OH}	V_{OUT} = V_{CC2} - 4V	-0.5	-1.5	-	A	1, 6, 27
		V_{OUT} = V_{CC2} - 15 V	-2.0	-	-		
低电平输出电流 Low Level Output Current	I_{OL}	V_{OUT} = V_{EE} + 1.5 V	1.0	-	-		2, 7, 28
		V_{OUT} = V_{EE} + 4.0 V	2.5	-	-		
故障状态下的低电平输出电流 Low Level Output Current During Fault Condition	I_{OLF}	V_{OUT} - V_{EE} = 14 V	90	140	230	mA	3, 29
高电平输出电压 High Level Output Voltage	V_{OH}	I_{OUT} = -100 mA	V_C -3.5	V_C -2.5	-	V	4, 6, 30
		I_{OUT} = -650 μA	V_C -1.5	V_C - 1	-		
		I_{OUT} = 0	-	-	V_C		-
低电平输出电压 Low Level Output Voltage	V_{OL}	I_{OUT} = 100 mA	-	0.1	0.5		5, 7, 31
高电平输入电源电流 High Level Input Supply Current	I_{CC1H}	V_{IN+} = V_{CC1} = 5.5 V V_{IN-} = 0 V	-	16	22	mA	8, 32, 33
低电平输入电源电流 Low Level Input Supply Current	I_{CC1L}	V_{IN+} = V_{IN-} = 0 V, V_{CC1} = 5.5 V	-	3	11		
输出电源电流 Output Supply Current	I_{CC2}	V_{OUT} = open	-	2.5	5		9, 10, 34, 35
低电平集电极电流 Low Level Collector Current	I_{CL}	I_{OUT} = 0	-	0.3	1.0		13, 54
高电平集电极电流 High Level Collector Current	I_{CH}	I_{OUT} = 0	-	0.3	1.3		13, 53
		I_{OUT} = -650 μA	-	1.8	3.0		13, 52

V_E 低电平供电电流 V_E Low Level Supply current	I_{EL}	-	-0.7	-0.4	0		12, 56
V_E 高电平供电电流 V_E High Level Supply current	I_{EH}	-	-0.5	-0.14	0		12, 35
消隐电容器充电电流 Blanking capacitor charging current	I_{cHG}	V_{DESAT} = 0 - 6 V, V_{DESAT} = 0 - 6 V, T_A = 25。c - 100。c	-0.13	-0.24	-0.33		11, 36
消隐电容器放电电流 Blanking capacitor Discharge current	I_{DScHG}	V_{DESAT} = 7 V	10	30	-		37
UVLO 國值 UVLO Threshold	V_{UVLO+}	I_F =10mA,V_{OUT} > 5 V	11.6	12.3	13.5	V	38
	V_{UVLO-}	I_F =10mA,V_{OUT} < 5 V	9.2	11.1	12.4		
UVLO 滞后 UVLO Hysteresis	V_{UVLO+} - V_{UVLO-}	-	-	1.2	-		
DESAT 國值 DESAT Threshold	V_{DESAT}	V_{cc2} - V_E > V_{UVLO-}	6.0	6.7	7.5		14, 39
输入國值电流从低到高 Threshold input current Low to high	$I_{F(ON)}$	Io = 0mA, Vo > 5.0V	-	2.0	5.0	mA	-
输入國值电压从高到低 Threshold input voltage High to low	$V_{F(OFF)}$	Io = 0mA, Vo < 5.0V	0.6	-	-	V	-

开关规格 switching specifications (AC)

除非另有说明 ，典型值测量值在 T_A = 25。c, V_{cc1} = 5 V, and V_{cc2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V 测得；
所有的最小/最大规格遵照推荐工作条件。
Unless otherwise noted, all typical values at T_A = 25。c, V_{cc1} = 5 V, and V_{cc2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V;
All Minimum/Maximum specifications are at Recommended Operating conditions.

参数 Parameter	符号 Symbol	条件 Condition	最小 Min.	典型 Typ.	最大 Max.	单位 Unit	备注 Note
V_{IN} 到高水平输出传播延迟时间 V_{IN} to High Level Output propagation Delay Time	t_{pLH}	Rg = 10 Ω, cg = 10 nF, f = 10 kHz, Duty cycle = 50%	0.10	0.30	0.50	μs	15, 16, 17, 18, 19, 20, 40, 49, 50
V_{IN} 到低电平输出 传播延迟时间 V_{IN} to Low Level Output propagation Delay Time	t_{pHL}		0.10	0..32	0.50		
脉冲宽度失真 pulse Width Distortion	pWD		-300	20	300	ns	-
任意两个部分之间的传播延迟差 propagation Delay Difference Between Any Two parts	pDD		-100	-	100		-
10%至 90%的上升时间 10% to 90% Rise Time	t_r		-	50	-		40
90%到 10%的下降时间 90% to 10% Fall Time	t_f		-	50	-		

DESAT 意义到 90%的 VOUT 延迟 DESAT Sense to 90% VOUT Delay	$t_{DESAT(90\%)}$	Rg = 10 Ω, Cg = 10 nF		0.3	0.5	μs	21, 51
DESAT 意义到 10%的 VOUT 延迟 DESAT Sense to 10% VOUT Delay	$t_{DESAT(10\%)}$	V_{CC2} - V_{EE} = 30 V		2.0	3.0		22, 41, 51
DESAT 检测到低电平故障信号延迟 DESAT Sense to Low Level $\overline{FAULT}$ Signal Delay	$t_{DESAT(\overline{FAULT})}$	-	-	1.8	5		42, 51
DESAT 翻转到 DESAT 低电平传播延迟时间 DESAT Sense to DESAT Low propagation Delay	$t_{DESAT(LOW)}$	-	0.1	0.25	1.0		51
$\overline{DESAT}$ 翻转到低电平故障信号延迟时间 $\overline{DESET}$ to High Level FAULT Signal Delay	$t_{RESET(\overline{FAULT})}$		3	7	20		23, 51
故障信号脉冲宽度 $\overline{RESET}$ Signal pulse Width	$pW_{\overline{RESET}}$		0.1				
UVLO 到 VOUT 的高延迟 UVLOto VOUT High Delay	$t_{UVLO\ ON}$	V_{CC2} = 1.0 ms ramp	-	5.0			44
UVLO 到 VOUT 的低延迟 UVLOto VOUT Low Delay	$t_{UVLO\ OFF}$		-	5.0			
输出高电平共模瞬态抗扰度 Output High Level Common Mode Transient Immunity	$\lvert CM_H \rvert$	T_A = 25。C, V_{CM} = 1500 V, V_{CC2} = 30 V	15	30	-	kV/μs	45, 46, 47, 48
输出低电平共模瞬态抗扰度 Output Low Level Common Mode Transient Immunity	$\lvert CM_L \rvert$	T_A = 25。C, V_{CM} = 1500 V, V_{CC2} = 30 V	15	30	-		

典型的性能曲线 TypicaI Performance curves

Fig.1 output High current vs. Ambient Temperature

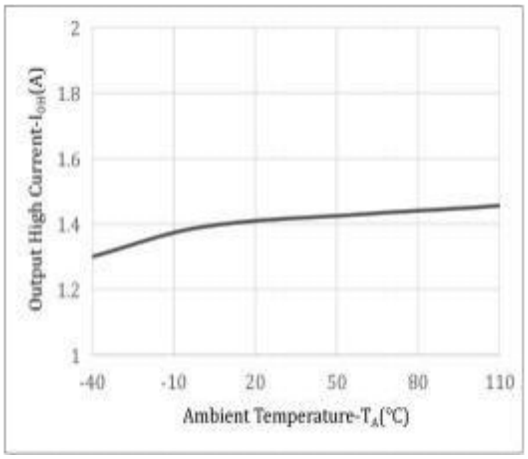


Fig.2 output Low current vs. Ambient Temperature

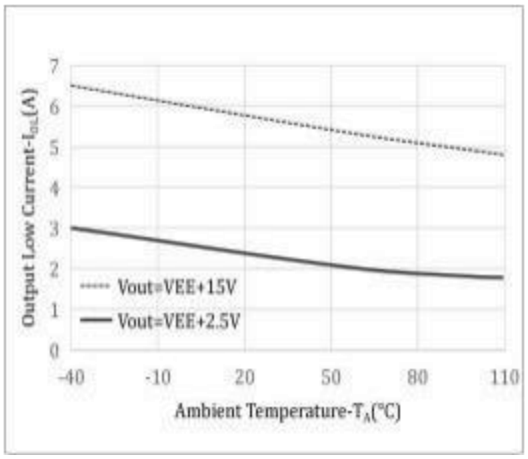


Fig.3 Low Level output current During Fault condition vs. output voltage

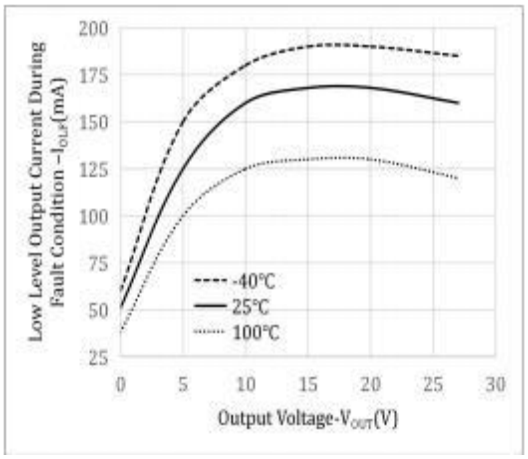


Fig.4 High output voltage Drop vs. Ambient Temperature

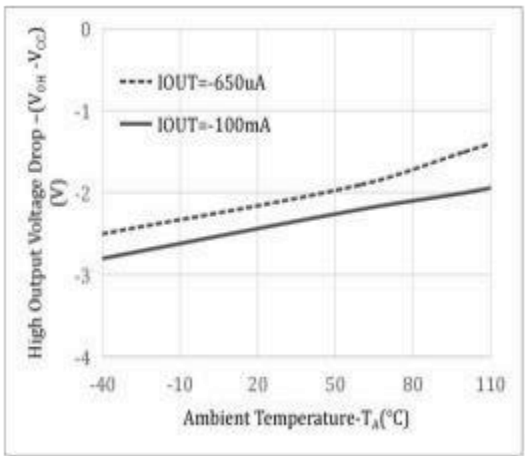


Fig.5 output Low voltage vs. Ambient Temperature

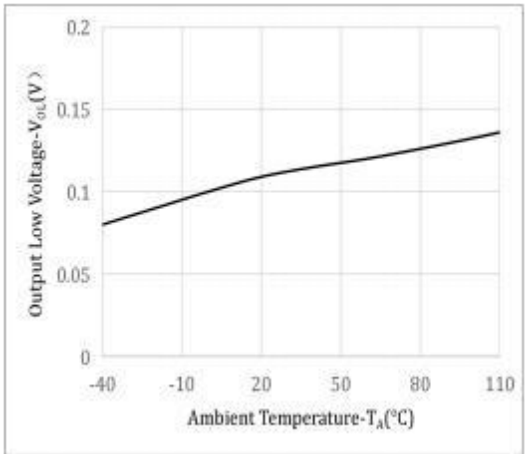


Fig.6 High output voltage vs. output High current

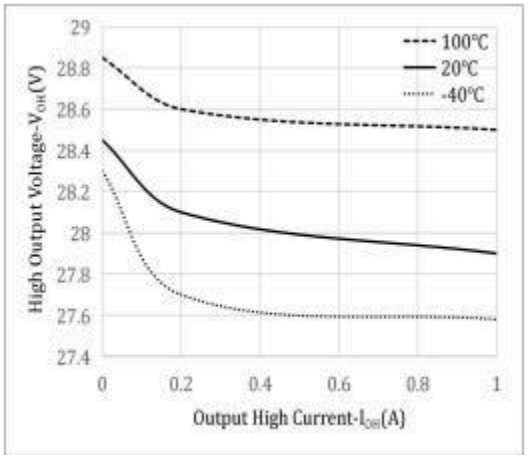


Fig.7 Low output voltage vs. output Low current

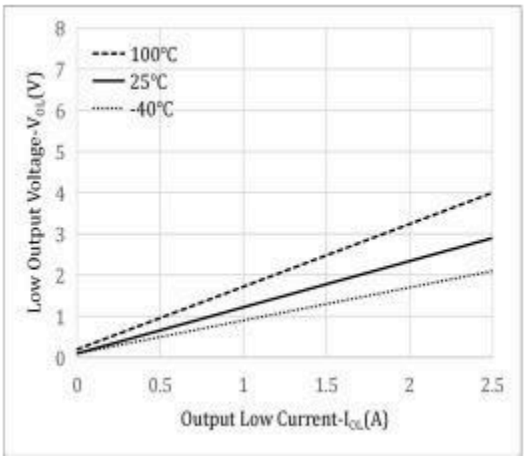


Fig.8 supply current vs. Ambient Temperature.

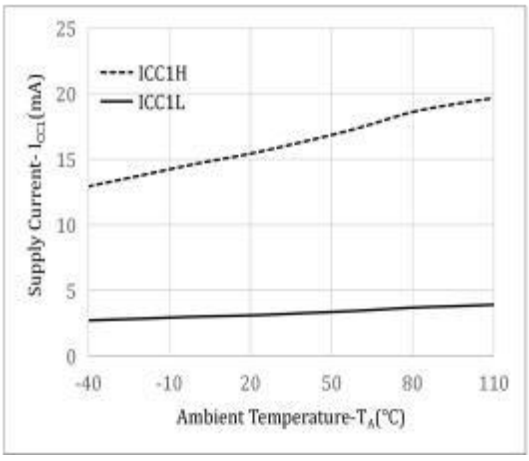


Fig.9 output supply current vs. Ambient Temperature

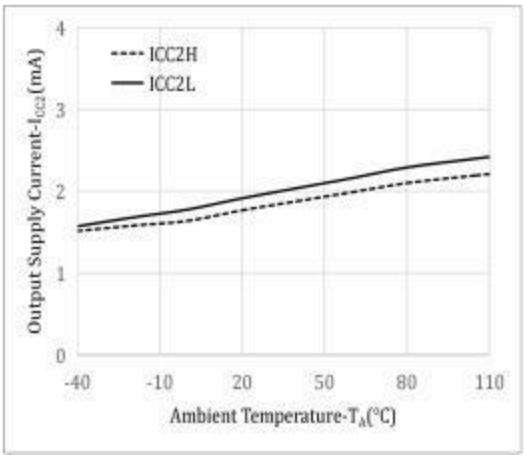


Fig.10 output supply current vs. output supply voltage

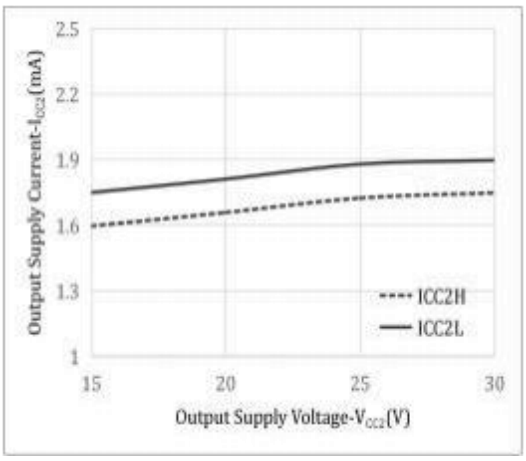


Fig.11 Blanking capacitor charging current vs. Ambient Temperature

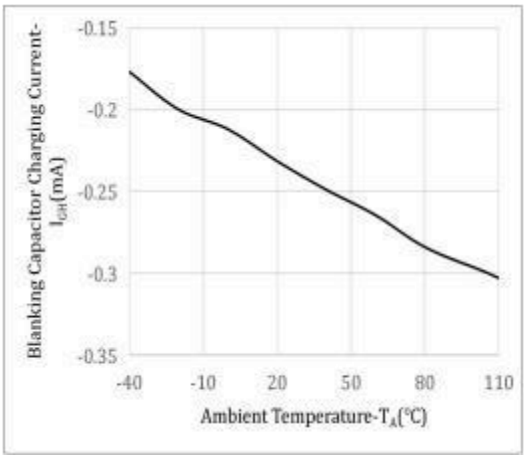


Fig.12 supply current vs. Ambient Temperature

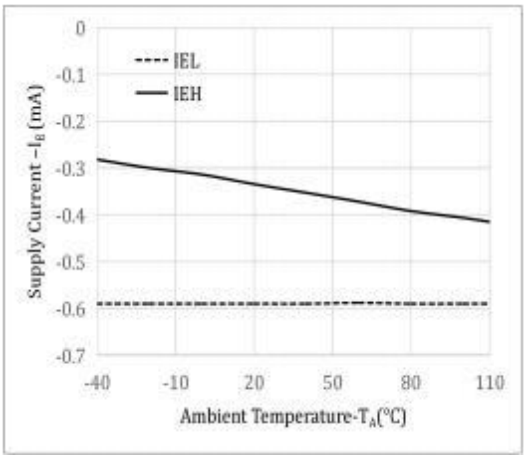


Fig.13 collector current vs. output current

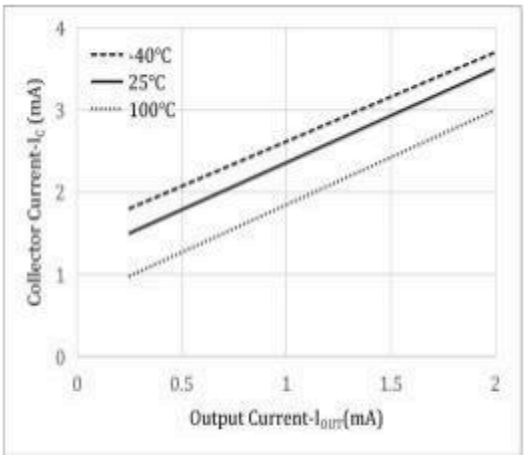


Fig.14 DESAT Threshold vs. Ambient Temperature

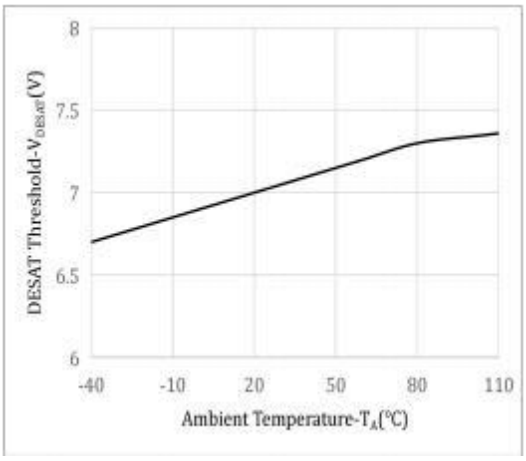


Fig.15 propagation Delay vs. Ambient Temperature

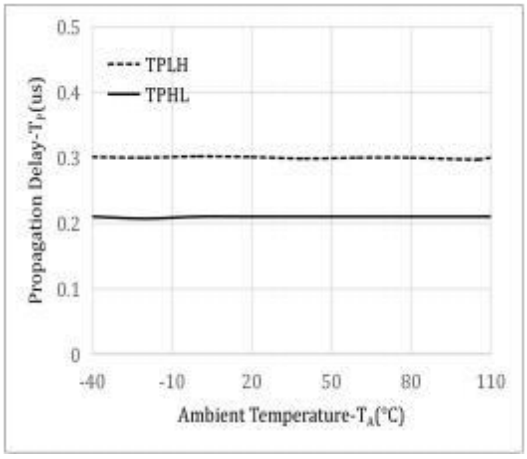


Fig.16 propagation Delay vs. Supply Voltage

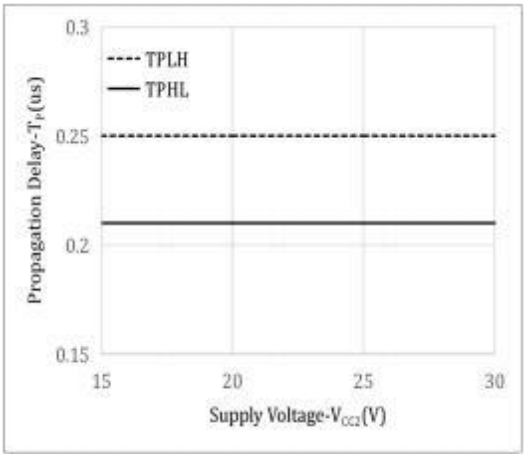


Fig.17 V_{IN} to High propagation Delay vs. Ambient Temperature

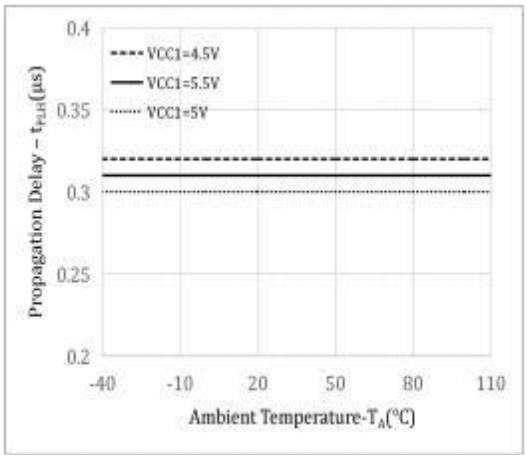


Fig.18 V_{IN} to Low propagation Delay vs. Ambient Temperature

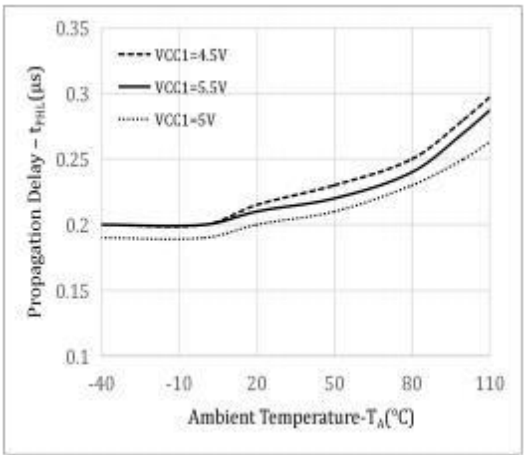


Fig.19 propagation Delay vs. Load capacitance

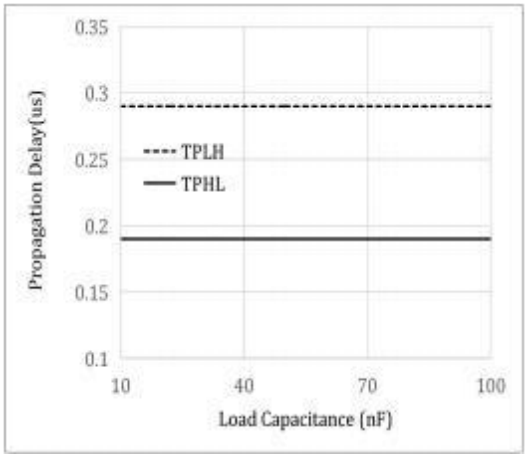


Fig.20 propagation Delay vs. Load Resistance

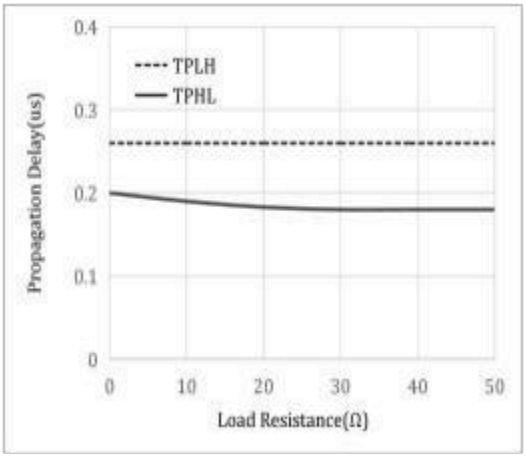


Fig.21 DESAT Sense to 90% VOUT Delay vs. Ambient Temperature

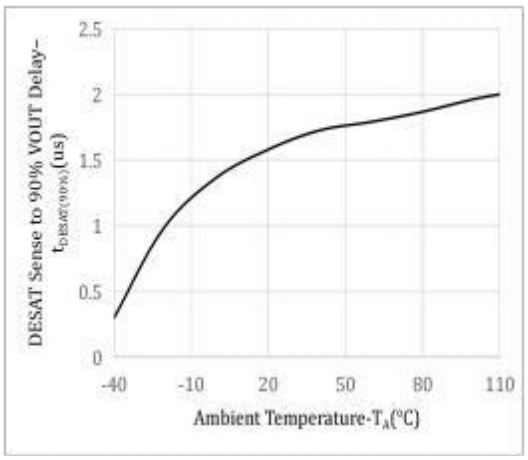


Fig.22 DESAT Sense to 10% VOUT Delay vs. Ambient Temperature

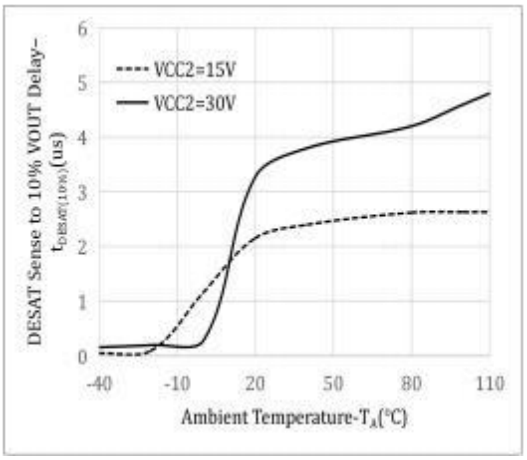


Fig.23 DESAT Sense to 10% VOUT Delay vs. Load capacitance.

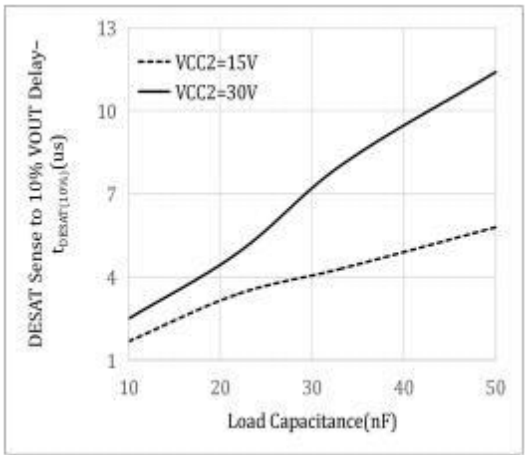
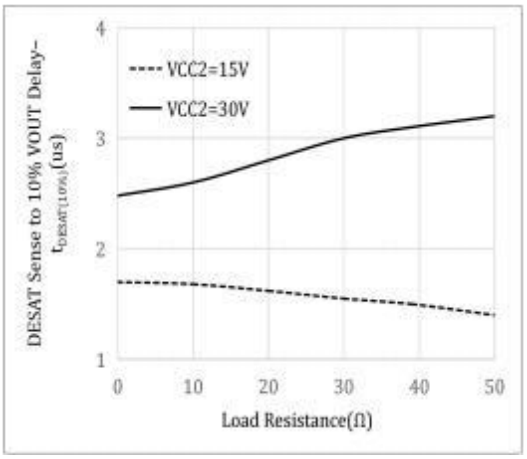


Fig.24 DESAT Sense to 10% VOUT Delay vs. Load Resistance.



测试电路图 Test circuits Diagrams

Figure 25. I_{FAULTL} test circuit

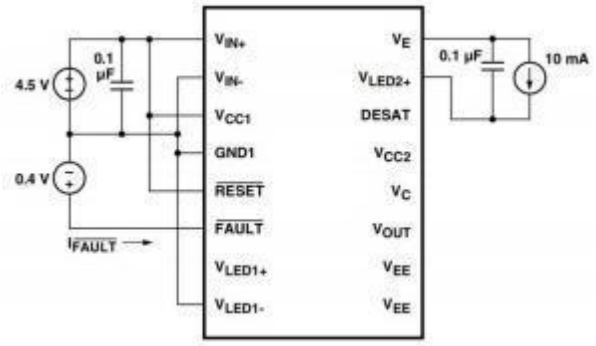


Figure 27. I_{OH} Pulsed test circuit

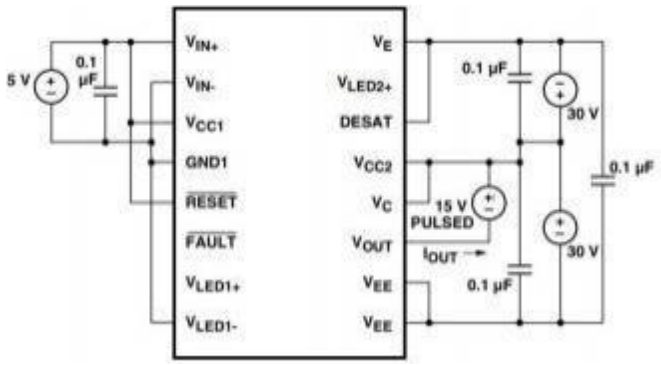


Figure 29. I_{OLF} test circuit.

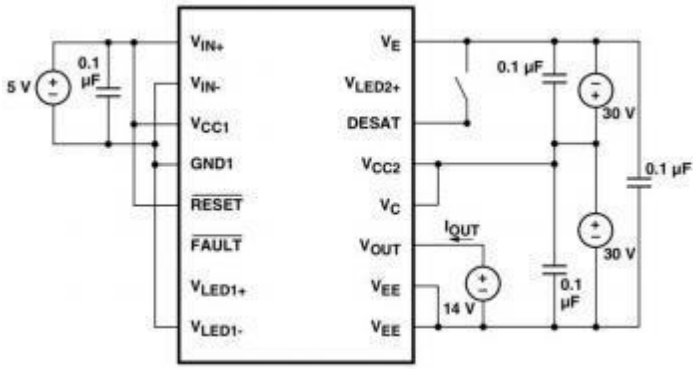


Figure 26. I_{FAULTH} test circuit

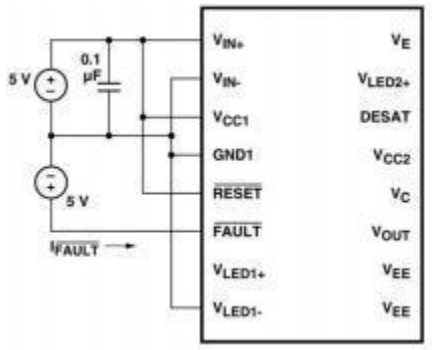


Figure 28. I_{OL} Pulsed test circuit.

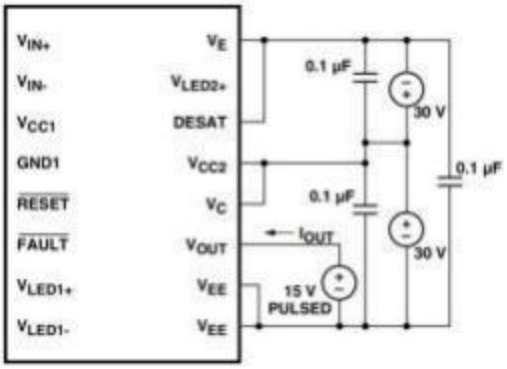


Figure 30. V_{OH} Pulsed test circuit.

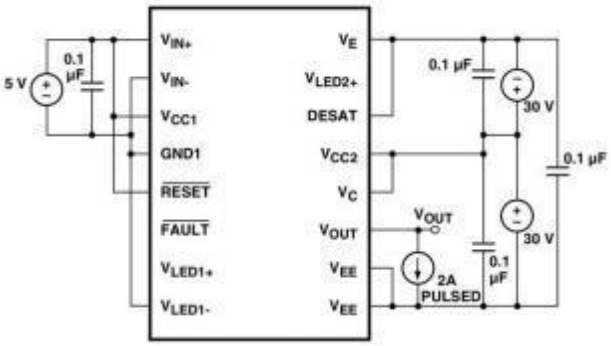


Figure 31. V_{OL} test circuit.

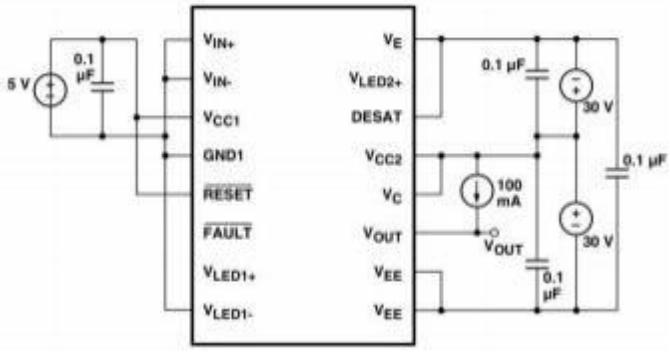


Figure 32. I_{cc1H} test circuit.

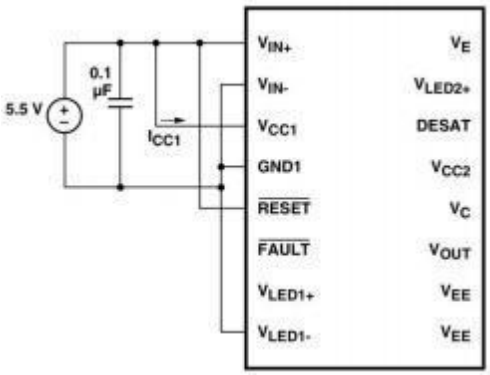


Figure 33. I_{cc1L} test circuit.

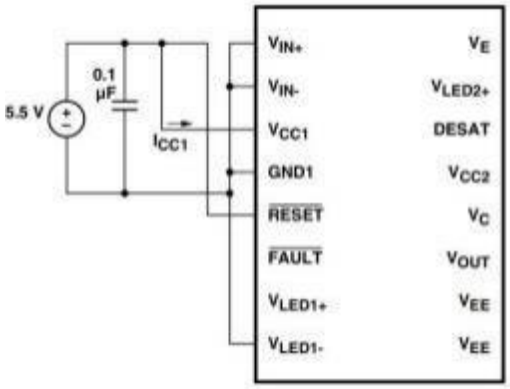


Figure 34. I_{cc2H} test circuit

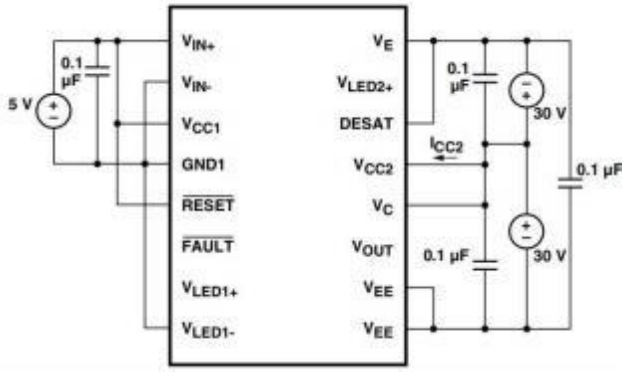


Figure 35. I_{cc2L} test circuit.

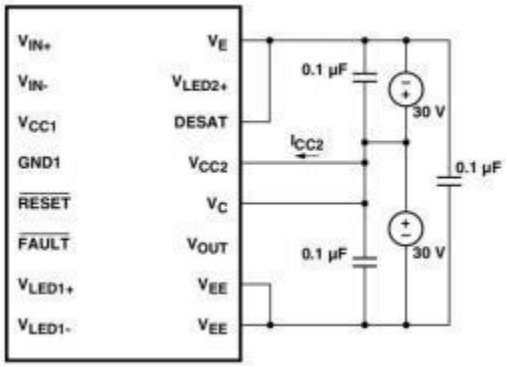


Figure 36. I_{CHG} Pulsed test circuit.

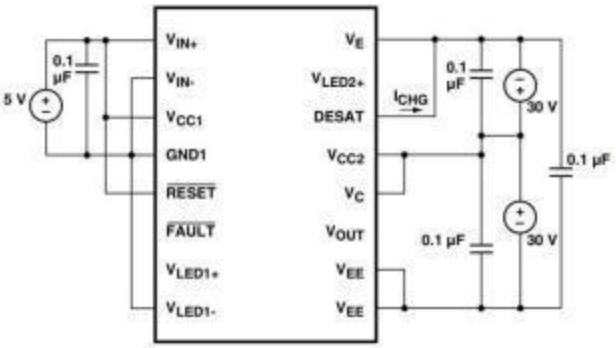


Figure 37. I_{DSCHG} test circuit.

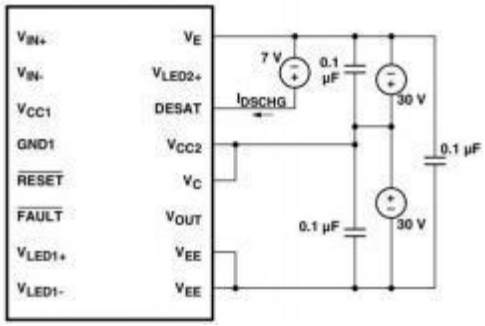


Figure 38. UVLo threshold test circuit

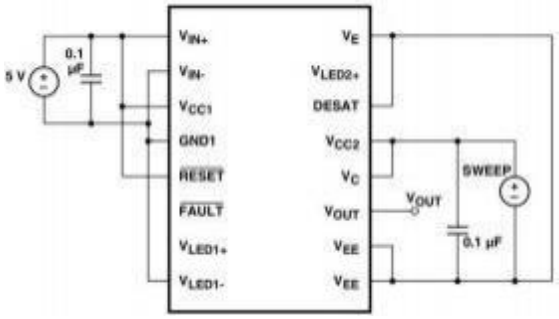


Figure 39. DESAT threshold test circuit.

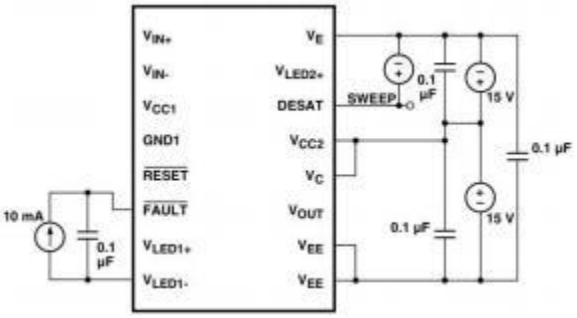


Figure 40. t_{pLH}, t_{pHL}, t_r, t_f test circuit

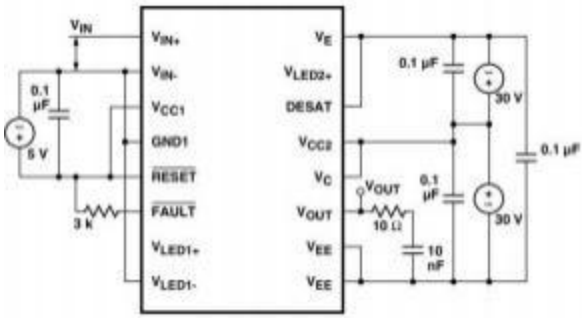


Figure 41. $t_{DESAT(10\%)}$ test circuit

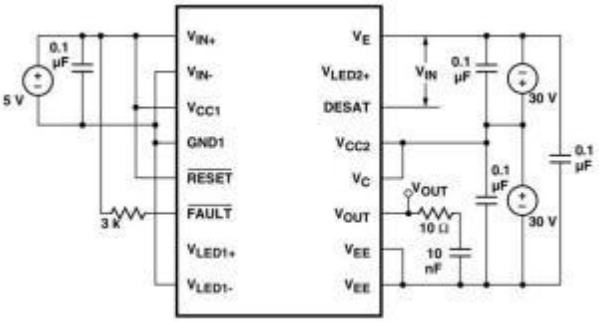


Figure 42. $t_{DESAT(FAULT)}$ test circuit

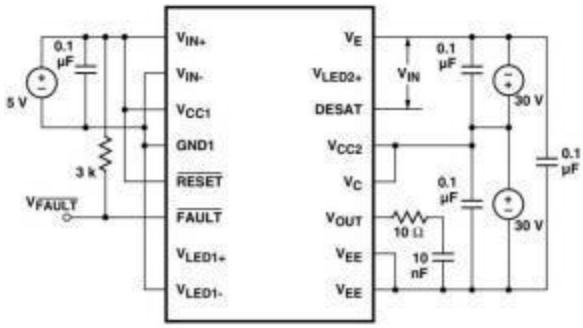


Figure 43. $t_{RESET(FAULT)}$ test circuit.

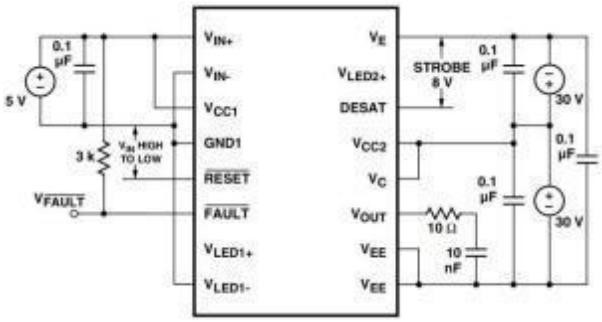


Figure 44. UVLo delay test circuit.

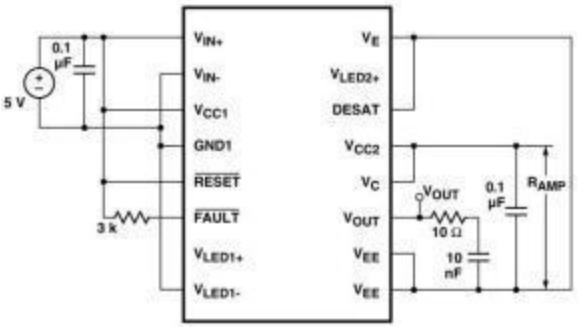


Figure 45. CMR test circuit, LED2 off.

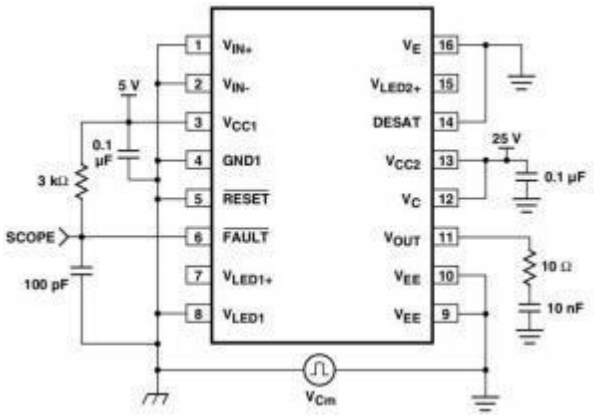


Figure 46. CMR test circuit, LED2 on.

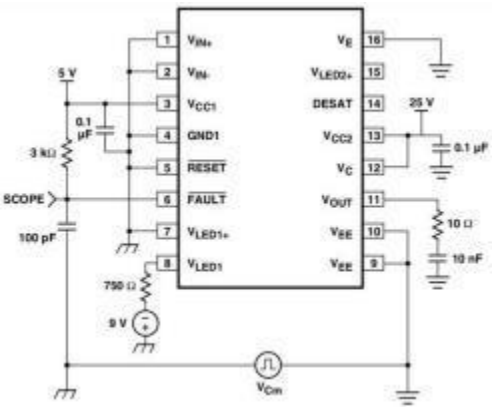


Figure 47. CMR test circuit, LED1 off.

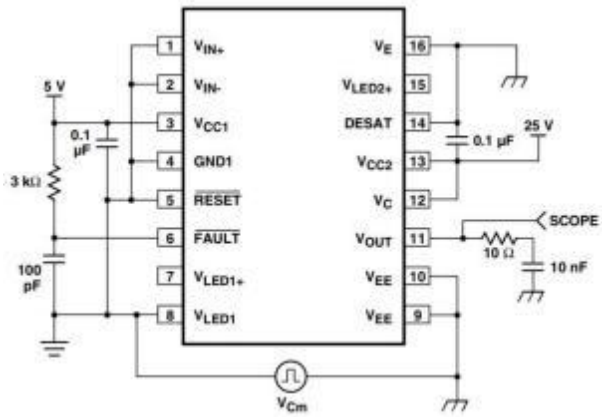


Figure 48. CMR test circuit, LED1 on.

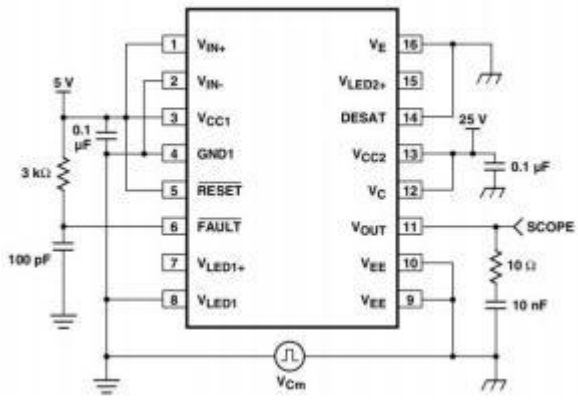


Figure 49. V_{OUT} ProPagation delay waveforms, noninverting configuration.

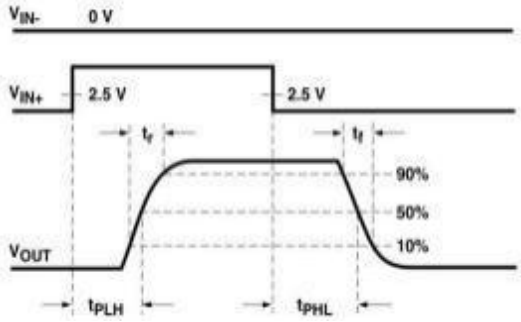


Figure 50. V_{OUT} ProPagation delay waveforms, inverting configuration.

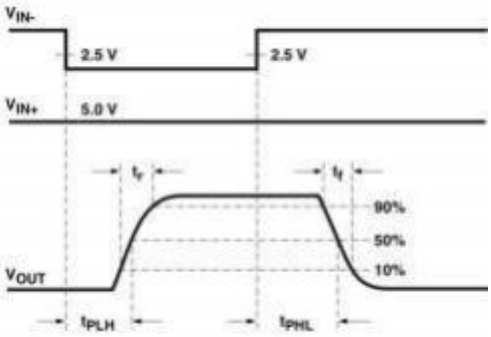


Figure 51. Desat, V_{OUT}, fault, reset delay waveforms.

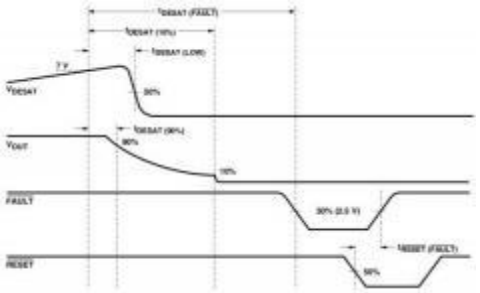


Figure 52. I_{CH} test circuit

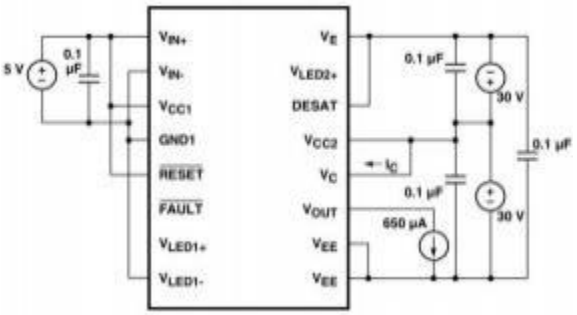


Figure 53. I_{CH} test circuit.

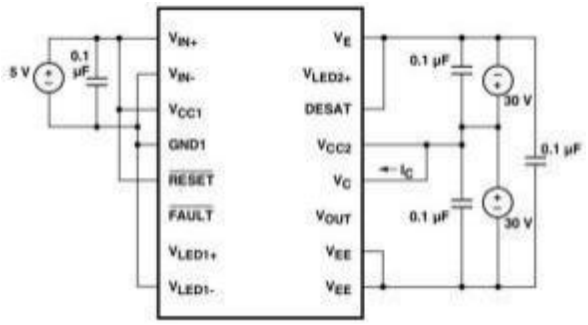


Figure 54. I_{CL} test circuit.

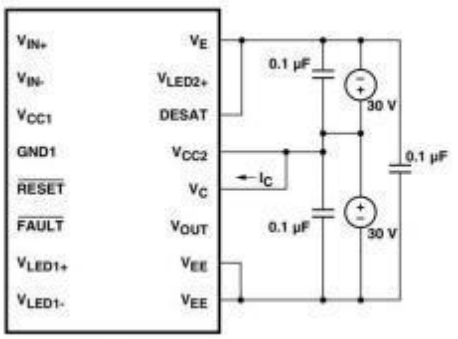


Figure 55. I_{EH} test circuit.

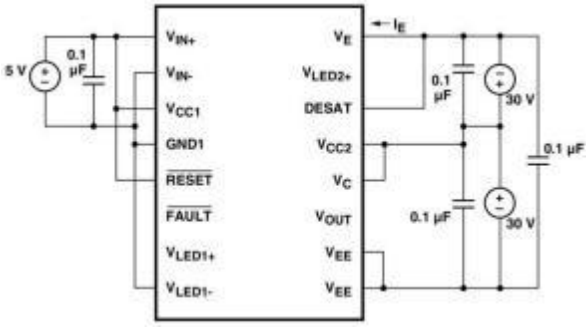
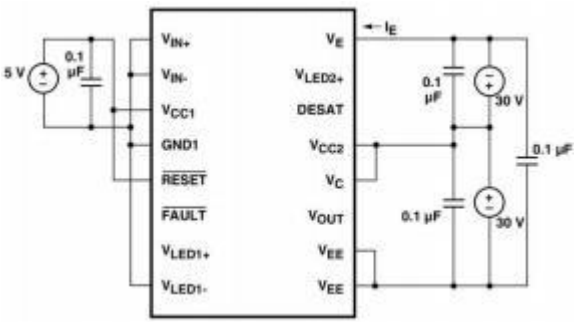
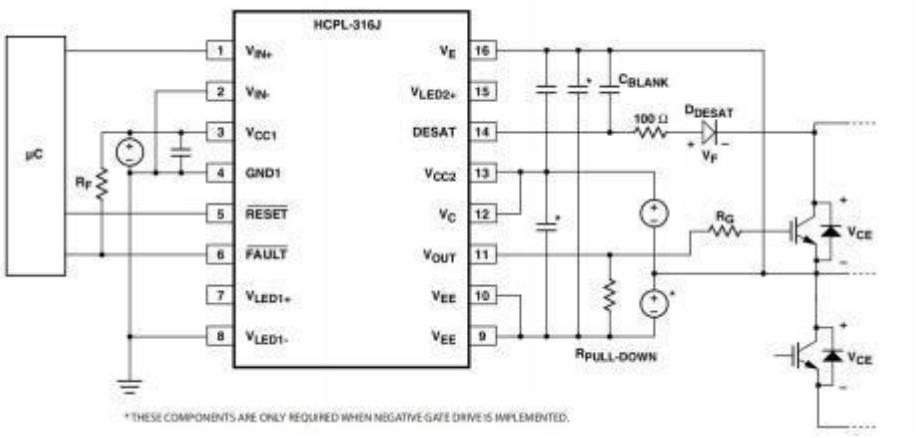


Figure 56. I_{EL} test circuit.



典型故障保护 IGBT 门驱动电路 TypicaI FauIt protected IGBT Gate Drive circuit

AT316J 是一款易于使用的智能栅极驱动器 ，其 IGBT 的 V_{CE} 故障保护结构紧凑 ，经济实惠 ，易于实现。用户可配置输入、集成去饱和 V_{CE} 检测、欠压锁定(UVLO ）、IGBT 软关断和隔离故障反馈等功能 ，以最大限度地提供设计灵活性和电路保护。
The AT316J is an easy-to use, intelligent gate driver which makes IGBT V_{CE} fault protection compact, affordable, and easy-to-implement. Features such as user configurable inputs, integrated V_{CE} detection, under voltage lockout (UVLO), soft IGBT turn-off and isolated fault feedback provide maximum design flexibility and circuit protection.



1.故麻状态下的操作说明DescriptionofoperationduringFaultcondition

. DESAT 终端通过 D_{DESAT} 监控 IGBT V_{CE} 电压
DESAT terminal monitors the IGBTV_{CE} voltage through D_{DESAT}.

. 当 DESAT 端的电压超过 7V 时 ，IGBT 门电压(V_{OUT} ）缓慢降低
when the voltage on the DESAT terminal exceeds 7 volts, the IGBT gate voltage (V_{OUT}) is slowly lowered.

. FAULT 输出低电平时 ，通知微控制器故障状态
$\overline{\text{FAULT}}$ output goes low, notifying the microcontroller of the fault condition.

. 微控制器采取适当的措施
Microcontroller takes appropriate action.

2.输出控制。utputcontrol

AT316J 的输出(V_{OUT} 和 FAULT)由 V_{IN}，UVLO 和检测到的 IGBT Desat 保护控制。如下表所示 ，AT316J 可以分别使用 V_{IN+}或 V_{IN-}输入来设置反相或非反相。当需要设置反相时 ，V_{IN+}必须保持在高电平 ，并切换 V_{IN-}。当需要设置非反相时 ，V_{IN-}必须保持低电平 ，并切换 V_{IN+}。一旦 UVLO 失效(V_{CC2} - V_E > V_{UVLO}) ， V_{OUT} 被允许输出高电平 ，AT316J 的 DESAT 检测功能将成为 IGBT 保护的主要来源。UVLO 需要确保 DESAT 的功能。一旦 V_{UVLO+} > 11.6 V，DESAT 持续工作 ，直到 V_{UVLO-} <12.4 V。因此 ，AT316J 的 DESAT 检测和 UVLO 功能协同工作 ，以确保持续的 IGBT 保护。
The outputs (V_{OUT} and FAULT) of the AT316J are controlled by the combination of V_{IN}, UVLO and a detected IGBT Desat condition. As indicated in the below table, the AT316J can be configured as inverting or non-inverting using the V_{IN+} or V_{IN-} inputs respectively. when an inverting configuration is desired, V_{IN+} must be held high and V_{IN-} toggled. when a non-inverting configuration is desired, V_{IN-} must be held low and V_{IN+} toggled. Once UVLO is not active (V_{CC2} - V_E > V_{UVLO}), V_{OUT} is allowed to go high, and the DESAT detection feature of the AT316J will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once V_{UVLO+} > 11.6V, DESAT will remain functional until V_{UVLO-} <12.4V. Thus, the DESAT detection and UVLO features of the AT316J work in conjunction to ensure constant IGBT protection.

V_{INP}	V_{INN}	UVLO(V_{DD2}-V_E)	DesatconditionDetect	FAULTB	V_{OUT}
X	X	Active	X	X	Low
X	X	X	yes	Low	Low
Low	X	X	X	X	Low
X	High	X	X	X	Low
High	Low	Not Active	No	High	High

典型的应用和操作 TyPicaI APPIication/oPeration

1.故障麻检测与保护技术简介IntroductiontoFaultDetectionandprotection

一个典型的三相逆变器的功率级易发生多种类型的故障 ，其中大多数故障对功率 IGBTs具有潜在的破坏性。这些故障模式可以分为四种基本类型:由于用户连接错误或线路不良导致的相位或轨道电源短路、 由于噪声或计算错误导致的控制信号故障、 由负载引起的过载以及栅极驱动电路中的组件故障。在任何一种故障条件下 ，通过 IGBTs 的电流都会迅速增加 ，导致过度的功耗和发热。当负载电流接近器件的饱和电流时 ，IGBTs 损坏 ，并且集电极到发射极的电压上升到饱和电压水平以上。急剧增加的功耗快速令电源设备过热并受到损坏。为了防止损坏驱动器 ，必须实施故障保护 ，以减少或关闭故障状态下的过流。

The power stage of a typical three phase inverter is susceptible to several types of failures, most of which are potentially destructive to the power IGBTs. These failure modes can be grouped into four basic categories: phase and/or rail supply short circuits due to user misconnect or bad wiring, control signal failures due to noise or computational errors, overload conditions induced by the load, and component failures in the gate drive circuitry. under any of these fault conditions, the current through the IGBTs can increase rapidly, causing excessive power dissipation and heating. The IGBTs become damaged when the current load approaches the saturation current of the device, and the collector to emitter voltage rises above the saturation voltage level. The drastically increased power dissipation very quickly overheats the power device and destroys it. To prevent damage to the drive, fault protection must be implemented to reduce or turn-off the overcurrents during a fault condition.

一种理想的解决方案就是提供快速的本地故障检测和关闭的电路 ，但迄今为止，所需的元件数量 ，电路板空间的消耗 ，成本和复杂性限制了其在高性能驱动器中的使用。该电路必须具有高速、低成本、低分辨率、低功耗和体积小的特点。

A circuit providing fast local fault detection and shutdown is an ideal solution, but the number of required components, board space consumed, cost, and complexity have until now limited its use to high performance drives. The features which this circuit must have are high speed, low cost, low resolution, low power dissipation, and small size.

2.应用程字信息ApplicationsInfomation

AT316J 满足了将高速、大电流输出驱动器、输入和输出之间的高压光隔离、IGBT 饱和检测、关断以及一个光隔离的故障状态信号反债集成到一个 16 引脚封装中的标准。

The AT316J satisfies these criteria by combining a high speed, high output current driver, high voltage optical isolation between the input and output, local IGBT desaturation detection and shutdown, and an optically isolated fault status feedback signal into a single 16-pin surface mount package.

AT316J 中采用的故障检测方法是通过监测 IGBT 的饱和(集电极）电压 ，并在集电极电压超过预定國值时触发局部故障停机而实现的。小栅极放电装置缓慢降低由 IGBT 短路引起的大电流 ，防止产生破坏性尖峰电压。在能耗达到破坏性水平之前 ，将 IGBT 关断。在 IGBT 关断状态期间 ，故障检测电路失效 ，以防止产生虚假的“故障”信号。

The fault detection method, which is adopted in the AT316J, is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off state of the IGBT, the fault detect circuitry is simply disabled to prevent false ,fault,signals.

如果功率器件的短路能力已知 ，有效的替代保护方案是测量 IGBT 电流以防止去饱和 ，但是如果栅极驱动电压降低到仅能将 IGBT 部分接通 ，则该方法将失败。通过直接测量集电极电压 ，AT316J 即使在栅极驱动电压不足的情况下也能限制 IGBT 的功耗。去饱和检测方法的另一个更巧妙的优势是监控 IGBT 的功耗 ，采用电流感测法 ，预设一个电流國值来预测安全工作的范围。因此 ，不需要过于保守的过电流國值来保护 IGBT。

The alternative protection scheme of measuring IGBT current to prevent desaturation is effective if the short circuit capability of the power device is known, but this method will fail if the gate drive voltage decreases enough to only partially turn on the IGBT. By directly measuring the collector voltage, the AT316J limits the power dissipation in the IGBT even with insufficient gate drive voltage. Another more subtle advantage of the desaturation detection method is that power dissipation in the IGBT is monitored, while the current sense method relies on a preset current threshold to predict the safe limit of operation. Therefore, an overly conservative over current threshold is not needed to protect the IGBT.

3.推荐应用电路RecommendedApplicationcircuit

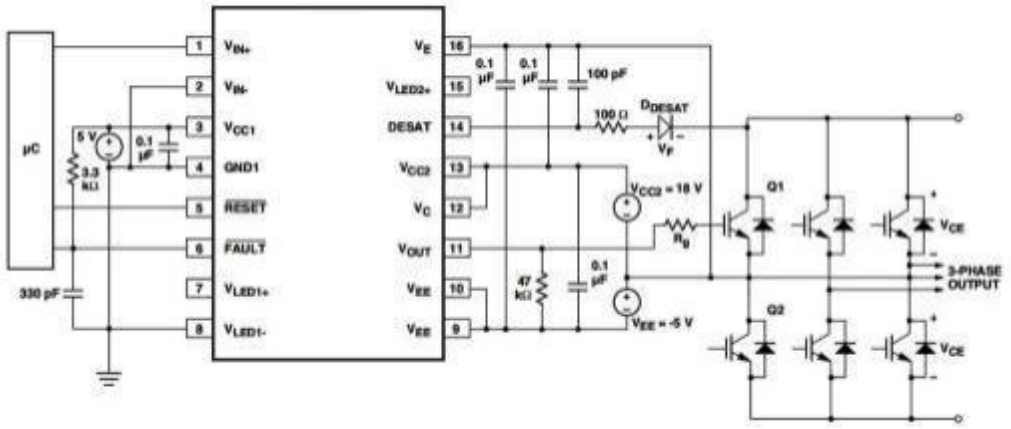
AT316J 具有反相和非反相栅极控制输入 ，一个有源低电平复位输入和一个开路集电极故障输出 ，适用于“或”逻辑电路应用。图 57 中所示的推荐应用电路体现了使用 AT316J 的典型栅极驱动电路。

The AT316J has both inverting and non-inverting gate control inputs, an active low reset input, and an open collector fault output suitable for wired ,OR,applications. The recommended application circuit shown in Figure 57 illustrates a typical gate drive implementation using the AT316J.

四个电源旁路电容器(0.1μF)在开关瞬态提供瞬态大电流。由于充电电流的瞬态性质 ，一个小功率电流(5mA)电源就足够了。DESAT 二极管和 100pF 的电容是故障检测电路中必不可少的外部元件。栅极电阻(10Ω)用于限制栅极充电电流 ，并控制 IGBT 集电极电压的上升和下降时间。开路集电极故障输出有一个无源上拉电阻 3.3kΩ和一个 330pF 的滤波电容。V_{OUT} 的 47kΩ下拉电阻可提供一个可预测的高电平输出电压(V_{OH})。在这类应用中 ，当检测到故障时 ，IGBT 门驱动器将关断 ，直到微控制器施加复位信号后才会恢复开启。

The four supply bypass capacitors (0.1 μF) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (5mA) power supply suffices. The DESAT diode and 100pF capacitor are the necessary external components for the fault detection circuitry. The gate resistor (10Ω) serves to limit gate charge current and indirectly control the IGBT collector voltage rise and fall times. The open collector fault output has a passive 3.3kΩ pull-up resistor and a 330 pF filtering capacitor. A 47kΩ pulldown resistor on V_{OUT} provides a more predictable high level output voltage (V_{OH}). In this application, the IGBT gate driver will shut down when a fault is detected and will not resume switching until the microcontroller applies a reset signal.

Figure 57. Recommended application circuit.



行为电路示意图 BehavioraI Circuit schematic

AT316J 的功能行为由图 60 中的逻辑图表示 ，该逻辑图充分描述了 AT316J 内部和外部信号的相互作用和序列。

The functional behavior of the AT316J is represented by the logic diagram in Figure 60 which fully describes the interaction and sequence of internal and external signals in the AT316J.

1 输 入 CInptc

在正常开关模式下 ，未检测到输出故障 ，故障锁存器的低状态允许输入信号控制 LED 信号。故障输出处于集电极开路状态 ，复位引脚的状态不影响对 IGBT 栅极的控制。当检测到故障时 ，故障输出和信号输入都被锁存。故障输出变为低电平有效状态 ，信号 LED 被强制关端 (输出低电平)。锁存状态将持续存在 ，直至复位引脚被拉低为止

In the normal switching mode , no output fault has been detected , and the low state of the fault latch allows the input signals to control the signal LED. The fault output is in the open-collector state , and the state of the Reset pin does not affect the control of the IGBT gate. when a fault is detected , the FAULT output and signal input are both latched. The fault output changes to an active low state , and the signal LED is forced off (output LOw). The latched condition will persist until the Reset pin is pulled low.

2. 输出coutputc

三个内部信号控制驱动器输出的状态 : LED 信号的状态 ，UVLO 和故障信号。如果 IGBT 集电极未检测到故障 ，且供电电压高于 UVLO 國值 ，则 LED 信号将控制驱动器的输出状态。逻辑驱动器中有一个互锁装置 ，以确保输出级的上拉和下拉装置永远不会同时导通。如果检测到欠压状态 ，无论 LED 状态如何 ，输出将被 50x DMOS 设备主动拉低。如果在 LED 信号亮起时检测到 IGBT 去饱和故障 ，故障信号将被锁存在高电平状态。三重达林顿和 50x DMOS 设备被禁用 ，一个较小的 1x DMOS 下拉设备被激活 ，缓慢地对 IGBT 栅极放电。当输出降至 2V 以下时 ，50x DMOS 设备再次开启 ，将 IGBT 栅极牢牢地钳位在 V_{EE} 上。故障信号仍保持锁存在高电平状态 ，直到 LED 信号关断。

Three internal signals control the state of the driver output: the state of the signal LED , as well as the UVLO and Fault signals. If no fault on the IGBT collector is detected , and the supply voltage is above the UVLO threshold , the LED signal will control the driver output state. The driver stage logic includes an interlock to ensure that the pull-up and pull-down devices in the output stage are never on at the same time. If an undervoltage condition is detected , the output will be actively pulled low by the 50x DMOS device , regardless of the LED state. If an IGBT desaturation fault is detected while the signal LED is on , the Fault signal will latch in the high state. The triple darlington AND the 50x DMOS device are disabled , and a smaller 1x DMOS pull-down device is activated to slowly discharge the IGBT gate. when the output drops below two volts , the 50x DMOS device again turns on , clamping the IGBT gate firmly to V_{EE}. The Fault signal remains latched in the high state until the signal LED turns off.

Figure 58. Behavioral Circuit Schematic

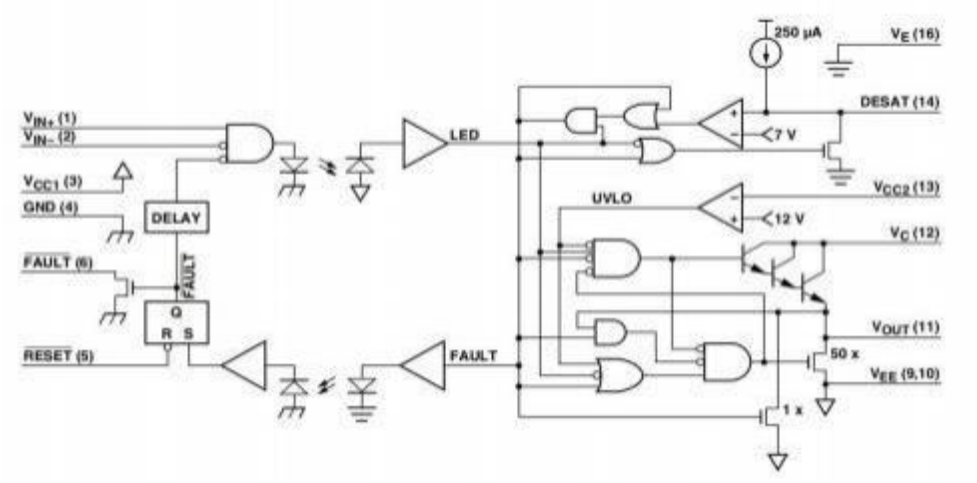


Figure 59. Output pull-down resistor

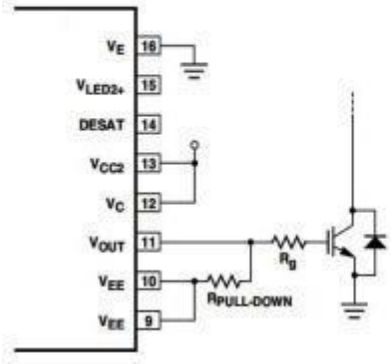


Figure 60. DESAT pin protection

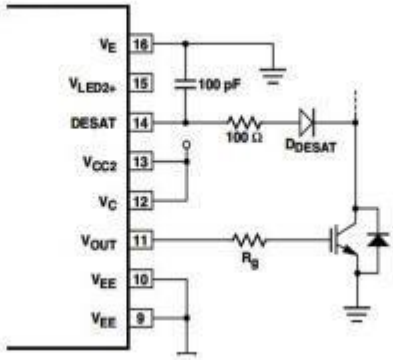
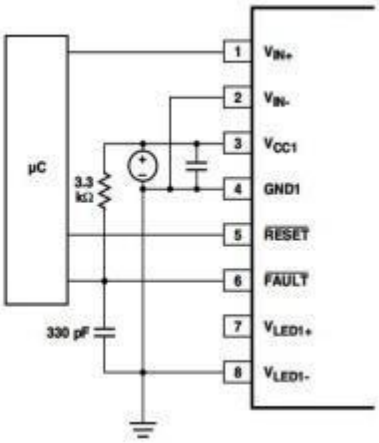


Figure 61. FAULT pin CMR protection



3.其他推存的组件。 therRecommendedcomponemts

图 57 中的应用电路包括一个输出下拉电阻、一个 DESAT 引脚保护电阻、一个 FAULT 引脚电容(330pF)和一个 FAULT 引脚上拉电阻。

The application circuit in Figure 57 includes an output pull-down resistor, a DESAT pin protection resistor, a FAULT pin capacitor (330pF), and a FAULT pin pull-up resistor.

4.输出下拉电器。 utputpull-DownResistor

在输出为高电平的转换期间 ,输出电压迅速上升至 V_{CC2} ,并保持在 3 个二极管压降以内。如果输出电流因容性负载而降至零 ,输出电压将在几微秒内缓慢上升约至 V_{CC2} -3(V_{BE})与 V_{CC2} 之间。为了将输出电压限制在 V_{CC2} -3(V_{BE}) ,建议在输出端与 V_{EE} 之间接一个下拉电阻 $R_{PULL-DOWN}$,以便在输出为高电平时产生几个 650µA 的灌电流。下拉电阻值取决于正向电源的值，可以根据公式 $R_{pull-down}$ =[V_{CC2} -3 *(V_{BE})]/650µA 进行调整。

During the output high transition, the output voltage rapidly rises to within 3 diode drops of V_{CC2}. If the output current then drops to zero due to a capacitive load, the output voltage will slowly rise from roughly V_{CC2} -3(V_{BE}) to V_{CC2} within a period of several microseconds. To limit the output voltage to V_{CC2} -3(V_{BE}), a pull-down resistor, $R_{PULL-DOWN}$ between the output and V_{EE} is recommended to sink a static current of several 650µA while the output is high. Pull-down resistor values are dependent on the amount of positive supply and can be adjusted according to the formula, $R_{pull-down}$ = [V_{CC2} -3 * (V_{BE})] / 650µA.

5.DESAT引脚保护DESATpinprotection

与 IGBTs连接的续流二极管会产生大大超过二极管正向电压理论值的瞬态正向电压。这可能会导致 DESAT 引脚上产生较大的反向尖峰电压 ，如果不采取保护措施的话 ，将从集成电路中转移大量电流。为了将这个电流限制在不会损坏集成电路的水平 ，需要插入一个 100 欧姆的电阻与 DESAT 二极管串联。这个新增的电阻不会改变 DESAT 國值或 DESAT 消隐时间。

The freewheeling of fly back diodes connected across the IGBTs can have large instantaneous forward voltage transients which greatly exceed the nominal forward voltage of the diode. This may result in a large negative voltage spike on the DESAT pin which will draw substantial current out of the IC if protection is not used. To limit this current to levels that will not damage the IC, a 100 ohm resistor should be inserted in series with the DESAT diode. The added resistance will not alter the DESAT threshold or the DESAT blanking time.

6高CMR的FAULT引脚上的电容capacitoronFAULTpinforHighcMR

当故障输出处于高状态时 ，快速共模瞬态会影响故障端电压。故障端和地之间应连接一个 330pF 电容器(图 60) ，当额定 CMR 为 15kV/μs 时 ，可获得足够的 CMOS 噪声容限。当检测到去饱和状态时 ，新增的电容不会增加故障输出延迟。

Rapid common mode transients can affect the fault pin voltage while the fault output is in the high state. A 330pF capacitor (Fig. 60) should be connected between the fault pin and ground to achieve adequate CMOS noise margins at the specified CMR value of 15kV/μs. The added capacitance does not increase the fault output delay when a desaturation condition is detected.

7.FAULT引脚上的上拉电阻器pull-UPResistoronFAULTpin

故障引脚是一个集电器开路输出 ，因此需要一个上拉电阻来提供高电平信号。

The FAULT pin is an open-collector output and therefore requires a pull-up resistor to provide a high-level signal.

8对于高CMR，采用标准的CMOS或TTL动电路DrivingwithstandardcMOS/TLforHighcMR

从隔离式高压电路到输入端涉及到的电路的电容糯合是 CMR 的主要限制。必须考虑到这种糯合 ，以实现较高的 CMR 性能。输入引脚 V_{IN+}和 V_{IN-}必须有自启动信号 ，以防止在极端共模瞬态条件下输出的意外切换。应避免使用上拉或下拉电阻的输入驱动电路 ，如集电极开路结构。建议使用标准的 CMOS 或 TTL 驱动电路

Capacitive coupling from the isolated high voltage circuitry to the input referred circuitry is the primary CMR limitation. This coupling must be accounted for to achieve high CMR performance. The input pins V_{IN+} and V_{IN-} must have active drive signals to prevent unwanted switching of the output under extreme common mode transient conditions. Input drive circuits that use pull-up or pull-down resistors, such as open collector configurations, should be avoided. Standard CMOS or TTL drive circuits are recommended

Figure 62. Typical input configuration, noninverting

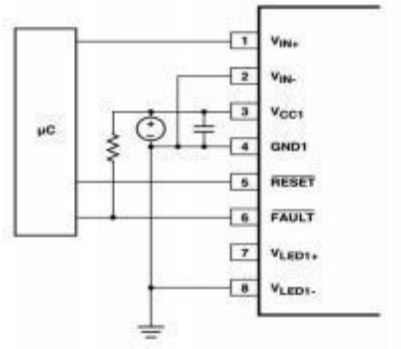


Figure 63. Typical Input configuration, Inverting

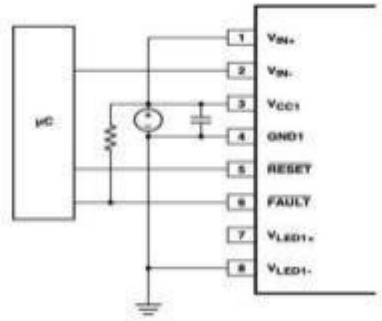
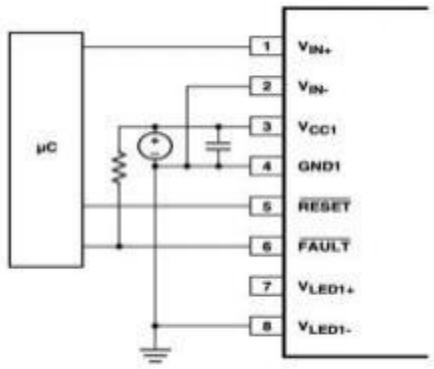


Figure 64. Local shutdown, local reset configuration



9.AT316J输入端的用户配量user-configurationottheAT316JInputside

V_{IN+} ,V_{IN-} ,FAULT 和 RESET 输入引脚令各种栅极控制和故障配置成为可能 ,具体取决于电机驱动要求。AT316J 同时具有反相和非反相栅极控制输入 ,适用于“或”应用的集电极开路故障输出和自动低电平复位输入。

The V_{IN+}, V_{IN-}, FAULT and RESET input pins make a wide variety of gate control and fault configurations possible, depending on the motor drive requirements. The AT316J has both inverting and noninverting gate control inputs, an open collector fault output suitable for wired , OR,applications and an active low reset input.

10.AT316J非反相反相模式动输入DrivingInputpfA316JinNon-inverting/InvertingMode

AT316J 的栅极驱动电压输出可以使用 V_{IN-}和 V_{IN+}输入来设置反相或非反相。如图 62 所示 ,当需要设置非反相时 ,通过将其连接到 GND1 ,将 V_{IN-}保持在低电平 ,并切换 V_{IN+}。如图 63 所示 ,当需要设置反相时 ,V_{IN+}连接到 V_{cc1} ,其保持在高电平 ,并切换 V_{IN-}。

The Gate Drive Voltage Output of the AT316J can be configured as inverting or non-inverting using the V_{IN-} and V_{IN+} inputs. As shown in Figure 62, when a non-inverting configuration is desired, V_{IN-} is held low by connecting it to GND1 and V_{IN+} is toggled. As shown in Figure 63, when an inverting configuration is desired, V_{IN+} is held high by connecting it to V_{cc1} and V_{IN-} is toggled.

11.局部关断，局部复位Localshutdown,LocalReset

如图 64 所示 ,对 AT316J 栅极驱动器的故障输出分别进行轮询 ,并且在故障发生后 ,独立断定复位线为低电平 ,从而复位电机控制器。

As shown in Figure 64, the fault output of each AT316J gate driver is polled separately, and the individual reset lines are asserted low independently to reset the motor controller after a fault condition.

12.全部关断，全部复位Global-shutdown,GlobalReset

如图 65 所示 ，当设置为反相操作时 ，通过将 FAULT 输出绑定到 VIN+ ，可以将 AT316J 设置为在故障情况下自动关断。对于高可靠性的驱动器 ，每个 AT316J 的集电器开路故障输出可以在一个共同的故障总线上连接在一起 ，形成一个单独的故障总线直接与微控制器接口。当 6 个栅极驱动器中的任何一个检测到故障时 ，故障输出信号将同时禁用这 6 个 AT316J 栅极驱动器 ，从而防止产生进一步的灾难性故障。

As shown in Figure 65, when configured for inverting operation, the AT316J can be configured to shutdown automatically in the event of a fault condition by tying the FAULT output to VIN+. For high reliability drives, the open collector $\overline{\text{FAULT}}$ outputs of each AT316J can be wire $\overline{\text{OR}}$,ed together on a common fault bus, forming a single fault bus for interfacing directly to the micro-controller. When any of the six gate drivers detects a fault, the fault output signal will disable all six AT316J gate drivers simultaneously and thereby provide protection against further catastrophic failures.

13.自动复位Auto-Reset

Figure 65. Global-shutdown, global reset configuration

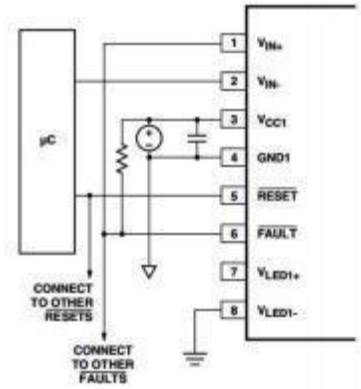


Figure 66. Auto-reset configuration

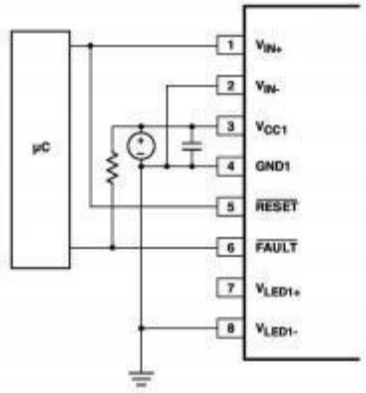


Figure 67a. safe hardware reset for noninverting input configuration (automatically resets for every V_{IN+} input)

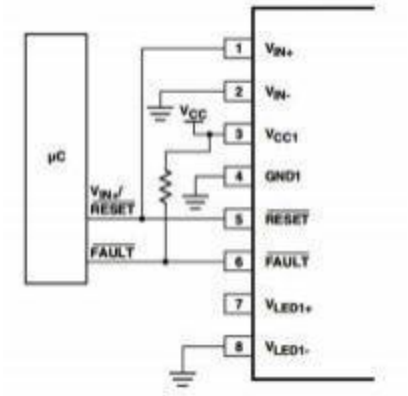
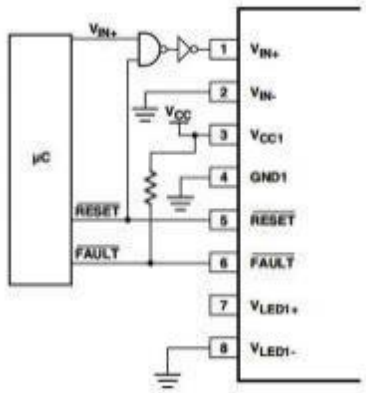


Figure 67b. safe hardware reset for noninverting input configuration



如图 66 所示 ，当反相 V_{IN-}输入连接到地面(设置非反相) 时 ，通过将 REsET 连接 V_{IN+}，可以将 AT316J 设置为自动复位。在这种情况下 ，在这种情况下 ，每个开关周期对非反相输入端和复位输入端施加栅极控制信号来复位故障锁存器。在 IGBT 正常工作时 ，断定复位输入低电平无效。发生故障后 ，门极驱动器保持在锁存故障状态 ，直到栅极控制信号变为写门低写状态并重置故障锁存。如果门极控制信号为连续的 PWM 信号 ，则故障锁存器在下一次输入信号变高时将一直复位。这种配置在逐周期的基础上保护 IGBT ，并在下一个写开启写周期之前自动复位。故障输出可以通过连接写 OR 写来提醒微控制器 ，但在这种(自动复位)配置下 ，该信号不能用于控制目的。此配置会逐个循环地保护 IGBT ，并在下一个 “开启” 循环之前

自动重置。故障输出可以连接起来或一起提醒微控制器 ，但这个信号不会用于此(自动重置) 配置中的控制目的。当 AT316J 设置为自动复位时 ，保证的最小故障信号脉冲宽度为 3μs。

As shown in Figure 66, when the inverting V_{IN-} input is connected to ground (non-inverting configuration), the AT316J can be configured to reset automatically by connecting RESET to V_{IN+}. In this case, the gate control signal is applied to the non-inverting input as well as the reset input to reset the fault latch every switching cycle. During normal operation of the IGBT, asserting the reset input low has no effect. Following a fault condition, the gate driver remains in the latched fault state until the gate control signal changes to the ,gate low,state and resets the fault latch. If the gate control signal is a continuous PWM signal, the fault latch will always be reset by the next time the input signal goes high. This configuration protects the IGBT on a cycle-by-cycle basis and automatically resets before the next ,on,cycle. The fault outputs can be wire ,OR,ed together to alert the micro- controller, but this signal would not be used for control purposes in this (Auto-Reset) configuration. When the AT316J is configured for Auto-Reset, the guaranteed minimum FAULT signal pulse width is 3 μs.

14. 遵循故障条件进行重置 ResettingFollowingaFaultcondition

为了在故障状态(FAULT 输出低电平) 后恢复正常的开关操作 ，RESET 引脚必须输出为低电平 ，以释放内部故障锁存器并重置 FAULT 输出(高电平) 。在确定 RESET 管脚为低电平之前 ，输入(VIN) 开关信号必须设置为输出(VOL) 低电平状态。这可以通过微控制器直接处理 ，也可以通过硬连线将 RESET 信号与合适的输入信号进行同步。这可以通过微控制器直接处理 ，也可以通过硬连线将 RESET 信号与合适的输入信号进行同步。图 67a 所示为在同相输入配置下 ，如何将 RESET 连接到 VIN+信号进行安全自动复位。图 67b 显示了如何配置 VIN+/ RESET 信号 ，使来自微控制器的 RESET 信号输入处于写输出-关断写状态。同样 ，图 67c和图 67d 显示了自动复位和微控制器复位安全配置的反相输入设置。

To resume normal switching operation following a fault condition (FAULT output low), the RESET pin must first be asserted low in order to release the internal fault latch and reset the FAULT output (high). Prior to asserting the RESET pin low, the input (VIN) switching signals must be configured for an output (VOL) low state. This can be handled directly by the microcontroller or by hardwiring to synchronize the RESET signal with the appropriate input signal. Figure 67a shows how to connect the RESET to the VIN+ signal for safe automatic reset in the noninverting input configuration. Figure 67b shows how to configure the VIN+/RESET signals so that a RESET signal from the microcontroller causes the input to be in the "output-off" ,state. Similarly, Figures 67c and 67d show automatic RESET and microcontroller RESET safe configurations for the inverting input configuration.

15. 用户配量AT316J输出侧RG和可选电器user-configurationoftheAT316JoutputsideRGandoptionalResistorR

栅极电阻 R_G (以及 V_{cc2} 和 V_{EE}) 的大小决定了栅极充/放电电流($I_{ON,\ PEAK}$ 和 $I_{OFF,\ PEAK}$) 的最大值 ，因此应谨慎选择以匹配被驱动 IGBT 的尺寸。通常希望栅极充电电流峰值略小于放电电流峰值($I_{ON,\ PEAK} < I_{OFF,\ PEAK}$) 。对于这种情况 ，可以使用一个可选的电阻(R_c) 和 R_G 来独立测定 $I_{ON,\ PEAK}$ 和 $I_{OFF,\ PEAK}$ ，而不需要使用转向二极管。作为示例 ，参考图 68。假设 R_G 已经确定 ，并且设计 $I_{OH,\ PEAK}$ = 0.5 A ，R_c 的值可以用下面的方法估计 ：

The value of the gate resistor R_G (along with V_{cc2} and V_{EE}) determines the maximum amount of gate-charging/dis-charging current ($I_{ON,PEAK}$ and $I_{OFF,PEAK}$) and thus should be carefully chosen to match the size of the IGBT being driven. Often it is desirable to have the peak gate charge current be somewhat less than the peak discharge current ($I_{ON,\ PEAK} < I_{OFF,PEAK}$). For this condition, an optional resistor (R_c) can be used along with R_G to independently determine $I_{ON,\ PEAK}$ and $I_{OFF,PEAK}$ without using a steering diode. As an example, refer to Figure 68. Assuming that R_G is already determined and that the design $I_{OH,\ PEAK}$ = 0.5A, the value of R_c can be estimated in the following way:

$$R_c + R_G = \frac{[V_{cc2} - V_{OH} - (V_{EE})]}{I_{OH,\ PEAK}}$$

$$= \frac{[4V - (-5V)]}{0.5A}$$

$$= 18\Omega$$

$$R_c = 8\Omega$$

16.采用外部电流缓冲超高输出电流HigheroutputcurrentusinganExtemalcurrentBuffer

为了提高 IGBT 栅极驱动电流 ，可以使用非反相电流缓冲器(如图 69 所示的 npn/pnp 缓冲器)。反相型与去饱和故障保护电路不兼容 ，应避免使用。为了在故障条件下保持 IGBT 的慢关断特性 ，需要在输入到 VEE 的缓冲器中连接一个 10nF 的电容 ，并在输出和公共 npn/ pnp 基极之间插入一个 10Ω的电阻。MJD44H11/MJD45H11 适用于最大 8A 的电流。D44VH10/ D45VH10 适用于最大 15A 的电流。

To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/pnp buffer shown in Figure 69) may be used. Inverting types are not compatible with the desaturation fault protection circuitry and should be avoided. To preserve the slow IGBT turn-off feature during a fault condition, a 10nF capacitor should be connected from the buffer input to VEE and a 10 Ω resistor inserted between the output and the common npn/ pnp base. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8A maximum. The D44VH10/ D45VH10 pair is appropriate for currents up to 15A maximum.

Figure 67c. safe hardware reset for inverting input configuration

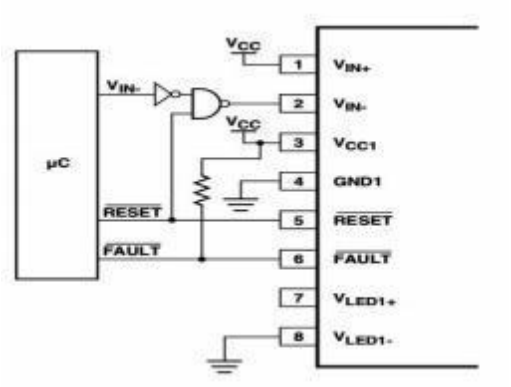


Figure 67d. safe hardware reset for inverting input configuration (automatically resets for every VIN- input)

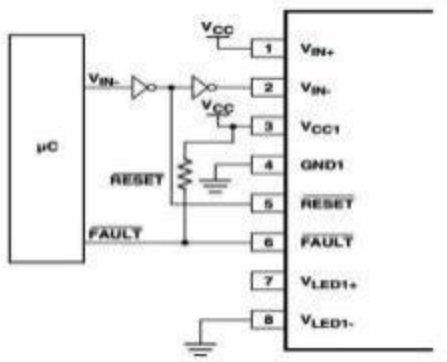


Figure 68. use of Rc to further limit ION, PEAK

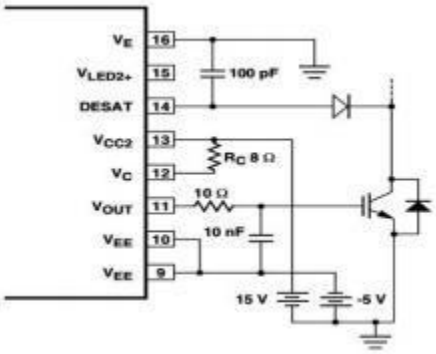
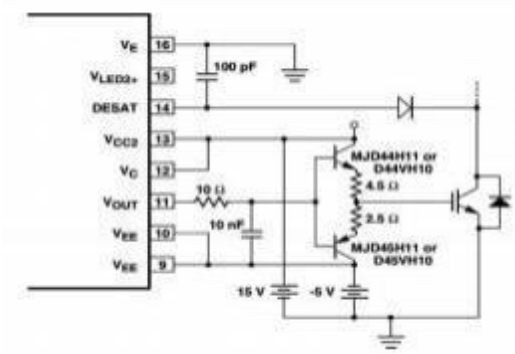


Figure 69. current buffer for increased drive current



17.DESAT二极管和DESAT阈值DESATDiodeandDESATThreshold

DESAT 二极管的作用是导通正向电流 ，可以感知 IGBT 的饱和集电极-发射极电压、V_{CESAT} (当 IGBT 处于导通状态时) 并阻断高压(当 IGBT写关断写时)。在 IGBT 关断的短时间内 ，IGBT 集电极到发射极之间通常存在非常高的 d V_{CE} / dt 电压上升率。这就产生了 I_{CHARGE} (= C_{D-DSAT} 根 dV_{CE} / dt)充电电流 ，该充电电流将对电容器 C_{BLANK}进行充电。为了尽量减少这种充电电流 ，避免误触发 DESAT ，最好使用快速响应二极管。在图 57 所示的推荐应用电路中 ，引脚 14 上的电压(DESAT) 为 V_{DESAT} = V_F + V_{CE} ，(其中 V_F 为 D_{DESAT} 的正向开启电压，V_{CE}为 IGBT 的集电极-发射极电压)。触发 DESAT 发出信号 FAULT 条件的 V_{CE}值名义上为 7V - V_F。如果需要 ，可以通过使用多个 DESAT 二极管串联来降低该 DESAT 國值电压。若 n 为 DESAT 二极管个数 ，则标称國值变为 $V_{CE,\ FAULT(TH)}$ = 7V-n x V_F。在使用两个二极管代替一个二极管的情况下 ，可以选择总所需最大反向耐压额定值的一半的二极管。

The DESAT diode , s function is to conduct forward current , allowing sensing of the IGBT , s saturated collector-to-emitter voltage , V_{CESAT} , (when the IGBT is " on") and to block high voltages (when the IGBT is " off"). During the short period of time when the IGBT is switching , there is commonly a very high dV_{CE}/dt voltage ramp rate across the IGBT , s collector-to-emitter. This results in I_{CHARGE} (= $C_{D-DESAT}$ x dV_{CE}/dt) charging current which will charge the blanking capacitor , C_{BLANK}. In order to minimize this charging current and avoid false DESAT triggering , it is best to use fast response diodes. In the recommended application circuit shown in Figure 57 , the voltage on pin 14 (DESAT) is V_{DESAT} = V_F + V_{CE} , (where VF is the forward ON voltage of D_{DESAT} and VCE is the IGBT collector-to-emitter voltage). The value of V_{CE} which triggers DESAT to signal a FAULT condition , is nominally 7V − V_F. If desired , this DESAT threshold voltage can be decreased by using multiple DESAT diodes in series. If n is the number of DESAT diodes then the nominal threshold value becomes $V_{CE,\ FAULT(TH)}$ = 7V — n x V_F. In the case of using two diodes instead of one , diodes with half of the total required maximum reverse-voltage rating may be chosen.

电源/布局注意事项 power/Layout considerations

1.在最大允许额定功率(RG的调整值)范围内运行。peratingwithintheMaximumAllowablepowerRatings(Adjusting valueofRG

在选择 R_G值时 ，必须确认 AT316J 的功耗在最大允许功耗范围内。

when choosing the value of R_G , it is important to confirm that the power dissipation of the AT316J is within the maximum allowable power rating.

执行此操作的步骤是 ：

The steps for doing this are:

(1) 计算最小期望 R_G ；
Calculate the minimum desired R_G ;

(2) 参考图 73 计算该部分的总功耗。(每个周期提供给 AT316J 的平均开关能量 vs R_G)
Calculate total power dissipation in the part referring to Figure 73. (Average switching energy supplied to AT316J per cycle vs. R_G plot)

(3) 将在步骤#2 中计算的输入、输出功耗与 AT316J 的最大推荐功耗进行比较。 (如果超过最大推荐水平 ，可能需要提高 RG 值以降低开关功率 ，并重复步骤 2。)
Compare the input and output power dissipation calculated in step #2 to the maximum recommended dissipation for the AT316J. (If the maximum recommended level has been exceeded , it may be necessary to raise the value of RG to lower the switching power and repeat step #2.)

例如 ，在满足一下条件的情况下 ，可以计算总输入输出功率损耗 ：

As an example , the total input and output power dissipation can be calculated given the following conditions:

- $I_{ON,\ MAX}$ ~ 2.0A
- V_{CC2} = 18V
- V_{EE} = -5V
- $f_{CARRIER}$ = 15 kHz

步骤 1:根据 I_{OL} 峰值计算 R_G 最小值：

Step 1: calculate R_G minimum from I_{OL} peak specification

为了找到充电峰值 I_{OL} ,假设栅极初始充电为 V_{EE} 的稳态值。因此 ,应用以下关系。

To find the peak charging I_{OL} assume that the gate is initially charged the steady-state value of V_{EE}. Therefore apply the following relationship.

$$RG = \frac{[V_{OH}@650\mu A-(V_{OL}+V_{EE})]}{I_{OL,PEAK}}$$

$$= \frac{[V_{cc2}-1-(V_{OL}+V_{EE})]}{I_{OL,PEAK}}$$

$$= \frac{18V-1V-(1.5V+(-5V))}{2.0A}$$

$$= 10.25\Omega$$

$$= 10.5\Omega \text{ (for a 1\% resistor)}$$

（从图 70 中可以注意，I_{OL} 的实际值可能与从所示的简单模型计算出的值有所不同。Note from Figure 70 that the real value of I_{OL} may vary from the value calculated from the simple model shown.）

步骤 2:计算 AT316J 中的总功耗：

Step2: calculate total power dissipation in the AT316J

AT316J 总功耗(P_T) 等于输入端功率(P_I) 和输出端功率(P_O) 之和：

The AT316J total power dissipation (P_T) is equal to the sum of the input-side power (P_I) and output-side power (P_O):

$P_T = P_I + P_O$;　　$P_I = I_{cc1} * V_{cc1}$

$P_O = P_{O(BIAS)} + P_{O,SWITCH}$

$= I_{cc2} * (V_{cc2}-V_{EE}) + E_{SWITCH} * f_{SWITCH}$

$P_{O（BIAS）}$ = AT316J 中由于器件偏置导致的稳态功耗

$P_{O(BIAS)}$ = steady-state power dissipation in the AT316J due to biasing the device.

$P_{O（SWITCH）}$ = AT316J 中由于功率器件栅极充放电而产生的瞬态功率耗散

$P_{O(SWITCH)}$ = transient power dissipation in the AT316J due to charging and discharging power device gate.

E_{SWITCH} =在一个开关周期内，由于功率器件的开关而耗散在 AT316J 中的平均能量(μJ/ cycle)。

E_{SWITCH} = Average Energy dissipated in AT316J due to switching of the power device over one switching cycle (μJ/cycle).

高频开关=平均载波信号频率

f_{SWITCH} = average carrier signal frequency

对于 R_G = 10.5 ,从图 71 中读取的值是 E_{SWITCH} =6.05μJ。假设最坏情况下平均 I_{cc1} = 16.5 mA （由 I_{cc1H}和 I_{cc1L} 的平均值给出）。类似于平均 I_{cc2} = 5.5 mA

For R_G = 10.5, the value read from Figure 71 is E_{SWITCH} = 6.05 μJ. Assume a worst-case average I_{cc1} = 16.5 mA (which is given by the average of I_{cc1H} and I_{cc1L}). Simiarly the average I_{cc2} = 5.5 mA

P_I = 16.5 mA * 5.5V = 90.8 mW

$P_O = P_{O(BIAS)} + P_{O,SWITCH}$

= 5.5 mA * (18V - (-5V)) + 6.051 μJ * 15 kHz

= 126.5 mW + 90.8 mW

= 217.3 mW

步骤 3:将计算出的功耗与 AT316J 的绝对最大值进行比较

step 3: Compare the calculated power dissipation with the absolute maximum values for the AT316J:

For the example

p_i = 90.8 mw < 150 mw (abs. max.) Ok

p_O = 217.3 mw < 600 mw (abs. max.) Ok

因此 ，本例没有超过功耗绝对最大额定值。

Therefore, the power dissipation absolute maximum rating has not been exceeded for the example.

Figure 70. Typical peak ION and IOFF currents vs. Rg (for AT316J output driving an IGBT rated at 600 V/100 A)

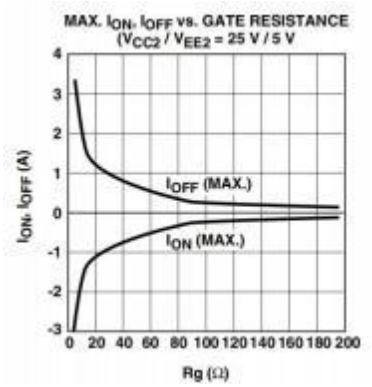
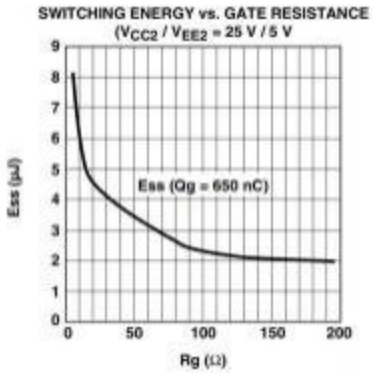


Figure 71. switching energy plot for calculating average pswitch (for AT316J output driving an IGBT rated at 600 V/100 A)



热模型 ThermaI ModeI

AT316J 设计通过输入 IC 的引脚 4 和输出 IC 的引脚 9 和 10 来散热。 (为此 ，输出侧有两个 V_{EE} 引脚 ，即引脚 9 和 10) 通过其他引脚或通过封装直接进入环境的热流被认为可以忽略不计 ，此处不予建模。

The AT316J is designed to dissipate the majority of the heat through pins 4 for the input IC and pins 09 and 10 for the output IC. (There are two VEE pins on the output side, pins 9 and 10, for this purpose.) Heat flow through other pins or through the package directly into ambient are considered negligible and not modeled here.

为了实现绝对最大规格中规定的功耗 ，引脚 4、9 和 10 必须连接地层。只要不超过最大功率规格 ，125气的绝对最大结温规格是对功耗的唯一其他限制。结温可通过以下公式计算 ：

In order to achieve the power dissipation specified in the absolute maximum specification, it is imperative that pins 4, 9, and 10 have ground planes connected to them. As long as the maximum power specification is not exceeded, the only other limitation to the amount of power one can dissipate is the absolute maximumjunction temperature specification of 125。C. Thejunction temperatures can be calculated with the following equations:

T_{ji} = pi (qi4 + q4A) + T_A

T_{jo} = po (qo9,10 + q9,10A) + T_A

其中 pi =输入 IC 的功率 ，po =输出 IC 的功率。 由于 q4A 和 q9,10A 取决于 pCB 布局和气流 ，因此可能无法得到它们的准确数值。因此 ，可用一下公式更精确地计算结温 ：

where pi = power into input IC and po = power into output IC. since q4A and q9,10A are dependent on pCB layout and airflow, their exact number may not be available. Therefore, a more accurate method of calculating the junction temperature is with the following equations:

T_{ji} = p_{qi4} + T_{p4}

T_{jo} = $p_{bqo9,10}$ + $T_{p9,10}$

然而 ，这些方程要求用 AT316J 封装边缘引脚上的热电偶测量引脚 4 和引脚 9，10 的温度

These equations，however，require that the pin 4 and pins 9，10 temperatures be measured with a thermal couple on the pin at the AT316J package edge.

从前期的功耗计算实例可知 :Pi = 90.8 mw，Po = 314 mw，T_A = 100气，，假设如下图 73 所示的热模型

From the earlier power dissipation calculation example: Pi = 90.8 mw，Po = 314 mw，T_A = 100。C，and assuming the thermal model shown in Figure 73 below.

Tji = (90.8 mw)(60。C/w + 50。C/w) + 100。C

= 110。C

Tjo = (240 mw)(30。C/w + 50。C/w) + 100。C

= 119。C

两者都在 125。C 的绝对最大规格范围内。然而 ，如果我们假设最坏的 PCB 布局和没有气流的情况下 ，其中估计的 q4A 和 q9，10A 为 100。C/w。则结温变为:

Both of which are within the absolute maximum specification of 125。C. If we，however，assume a worst case PCB layout and no air flow where the estimated q4A and q9，10A are 100。C/w. Then thejunction temperatures become:

Tji = (90.8 mw)(60。C/w + 100。C/w) + 100。C

= 115。C

Tji = (240 mw)(30。C/w + 100。C/w) + 100。C

= 131。C

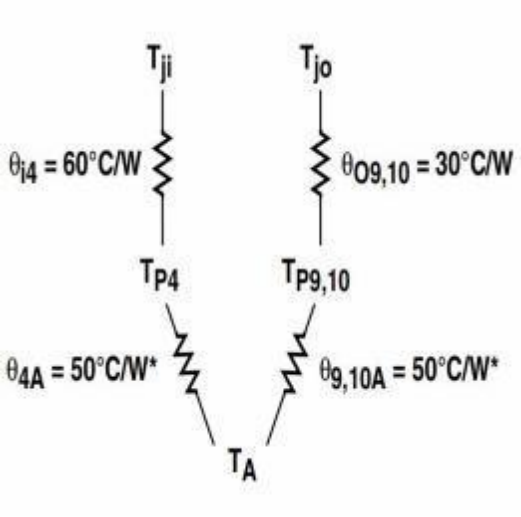
输出 IC 结温度超过最大规格 125气. 在这种情况下 ，需要对 PCB 的布局和气流进行设计 ，使输出 IC 的结温度不超过 125气.

The output ICjunction temperature exceeds the absolute maximum specification of 125。C. In this case，PCB layout and airflow will need to be designed so that thejunction temperature of the output IC does not exceed 125。C.

如果图 72 中热模型的计算结温高于 125。C ，为了更准确地估计结温 ，需要在最恶劣的工作环境下测量 9 引脚和 10 引脚的温度 (在包装边缘处)

If the calculatedjunction temperatures for the thermal model in Figure 72 is higher than 125。C，the pin temperature for pins 9 and 10 should be measured (at the package edge) under worst case operating environment for a more accurate estimate of thejunction temperatures.

Figure 72. AT316Jthermal model



T_{ji} =输入端 IC 结温

T_{ji} =junction temperature of input side IC

T_{jo} =输出端 IC 结温

T_{jo} =junction temperature of output side IC

T_{P4} =封装边缘的引脚 4 温度

T_{P4} = pin 4 temperature at package edge

$T_{P9,10}$ =封装边缘引脚引脚 9 和 10 的温度

$T_{P9,10}$ = pin 9 and 10 temperature at package edge

θ_{I4} =输入端 IC 到引脚 4 的热阻

θ_{I4} = input side IC to pin 4 thermal resistance

$\theta_{I9,10}$ =输出端 IC 到引脚 9 和 10 的热阻

$\theta_{I9,10}$ = output side IC to pin 9 and 10 thermal resistance

θ_{4A} = 引脚 4 环境热阻

θ_{4A} = pin 4 to ambient thermal resistance

$\theta_{9,10A}$ =引脚 9 和 10 环境热阻

$\theta_{9,10A}$ = pin 9 and 10 to ambient thermal resistance

*此处显示的θ_{5A}和$\theta_{9,12A}$值是针对图 74 气流合理的 PCB 布局。根据 PCB 布局/气流情况 ,该值可能增加或减少 2 倍

*The θ_{4A} and $\theta_{9,10A}$ Values shown here are for PCB layouts shown in Figure 74 with reasonable air flow. This Value may increase or decrease by a factor of 2 depending on PCB layout and air flow.

印刷电路板布局的注意事项 printed circuit Board Layout considerations

高压隔离电路与任何输入参考电路之间应始终保持足够的间距。必须注意在印刷电路板的两个相邻的高边隔离区之间提供相同的最小间距。间距不足会降低有效隔离度 ，增加寄生耦合 ，降低 CMR 性能。

Adequate spacing should always be maintained between the high voltage isolated circuitry and any input referenced circuitry. Care must be taken to provide the same minimum spacing between two adjacent high-side isolated regions of the printed circuit board. Insufficient spacing will reduce the effective isolation and increase parasitic coupling that will degrade CMR performance.

电源旁路电容的布线需要特别注意。在开关瞬态过程中 ，大部分的栅极电荷由旁路电容提供。保持较短的旁路电容跟踪长度将保证较低的电源纹波和干净的开关波形。

The placement and routing of supply bypass capacitors requires special attention. During switching transients , the majority of the gate charge is supplied by the bypass capacitors. Maintaining short bypass capacitor trace lengths will ensure low supply ripple and clean switching waveforms.

接地平面连接对于引脚 4 (GND1)和引脚 9 和 10 (VEE)是必要的 ，以实现最大的功耗 ，因为 AT316J 的设计是为了消耗通过这些引脚产生的大部分热量。实际功耗将取决于应用环境(PCB 布局、气流、部件放置等) ，有关如何估计结温的详细信息 ，请参阅热模型部分。

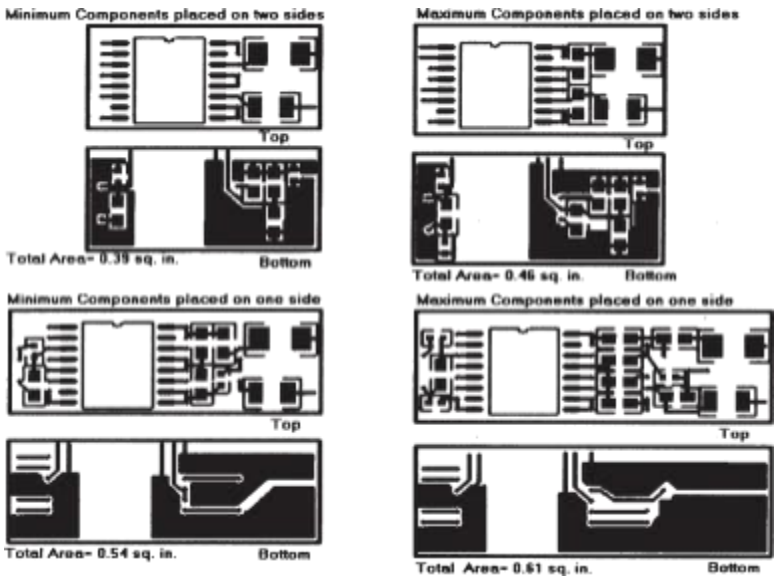
引脚 4 (GND1)和引脚 9 和 10 (V_{EE})需要接地 ，以实现最大功耗 ，因为 AT316J 设计用于耗散通过这些引脚产生的大部分热量。实际功耗将取决于应用环境(PCB 布局、气流、部件放置等。)关于如何估计结温的详细信息 ，请参阅热模型部分。

Ground Plane connections are necessary for pin 4 (GND1) and pins 9 and 10 (V_{EE}) in order to achieve maximum power dissipation as the AT316J is designed to dissipate the majority of heat generated through these pins. Actual power dissipation will depend on the application environment (PCB layout , air flow , part placement , etc.) see the Thermal Model section for details on how to estimatejunction temperature.。

下面的布局实例具有良好的电源旁路和热特性 ，PCB 占地面积小 ，信号和供电线路容易连接。这四个例子涵盖了单面和双面元件布局 ，以及最小和改进的性能电路。

The layout examples below have good supply bypassing and thermal properties , exhibit small PCB footprints , and have easily connected signal and supply lines. The four examples cover single sided and double sided component placement , as well as minimal and improved performance circuits.

Figure 73. Recommended layout(s).



系统注意事项 system considerations

传播延迟差 Propagation Delay Difference (PDD)

AT316J 包括一个传播延迟差异(PDD)规范 ，旨在帮助设计人员在功率逆变器设计中尽量减少写死区时间写。死区时间是高、低侧功率晶体管(图 57 中的 Q1 和 Q2)均关断的时间段。Q1 和 Q2 导通的任何重叠都将导致大电流流过高低压电机导轨之间的功率器件 ，这是一个必须防止的潜在灾难性条件。

The AT316J includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 57) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails, a potentially catastrophic condition that must be prevented.

在给定的设计中 ，为了最小化死区时间 ，AT316J 驱动 Q2 的导通应该延迟(相对于 AT316J 驱动 Q1 的关断) ，这样在最坏的情况下 ，当晶体管 Q2 导通时 ，晶体管 Q1 刚好关断 ，如图 74 所示。在-40。c 到 110。c 的工作温度范围内 ，实现该条件所需的延迟量等于传播延迟差 PDDMAX 的最大值 ，即指定为 400ns。

To minimize dead time in a given design, the turn-on of the AT316J driving Q2 should be delayed (relative to the turn-off of the AT316J driving Q1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 74. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDDMAX, which is specified to be 400 ns over the operating temperature range of -40。c to 110。c.

通过最大传播时延差对 AT316J 开通信号进行延迟保证了最小死区时间为零 ，但并没有告诉设计者最大死区时间是多少。最大死区时间相当于最大和最小传播时延差规范的差值 ，如图 75 所示。在-40。c 到 110。c 的工作温度范围内 ，AT316J 的最大死时间为 800 ns ((= 400ns - (- 400ns)))。

Delaying the AT316J turn-on signals by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 75. The maximum dead time for the AT316J is 800 ns (= 400ns - (-400ns)) over an operating temperature range of -40。c to 110。c.

值得注意的是 ，用于计算 PDD 和死区时间的传播延迟是在相同的温度和测试条件下计算的 ，因为所考虑的光耦通常安装在彼此接近的位置 ，并且是开关相同的 IGBT。

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

Figure 74. Minimum LED Skew for zero Dead Time

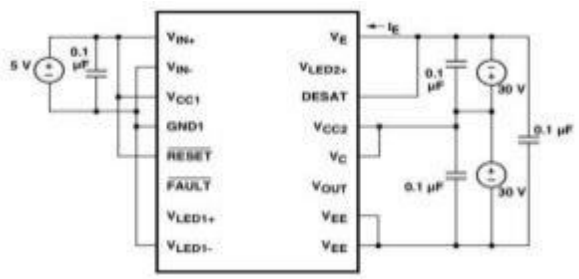
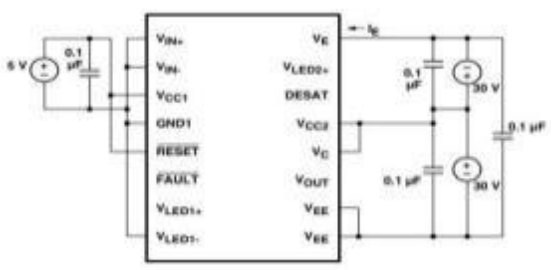
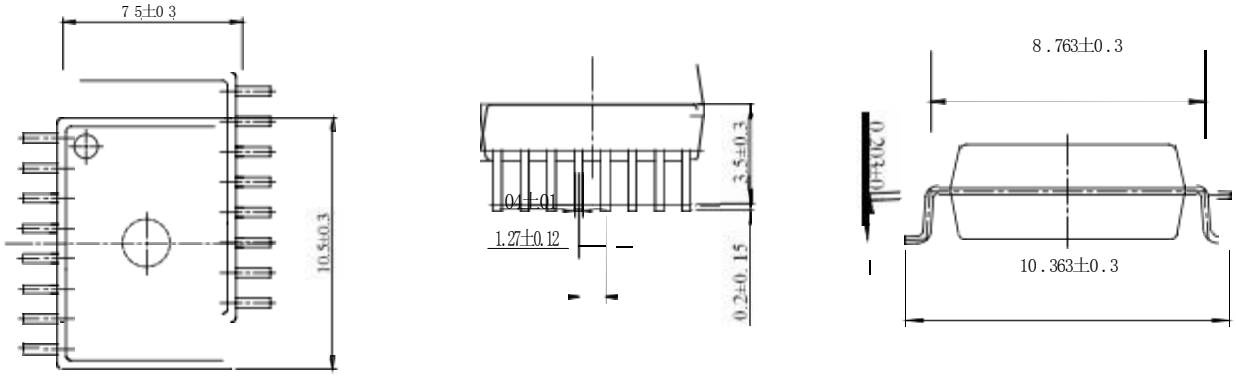


Figure 75. waveforms for Dead Time calculation



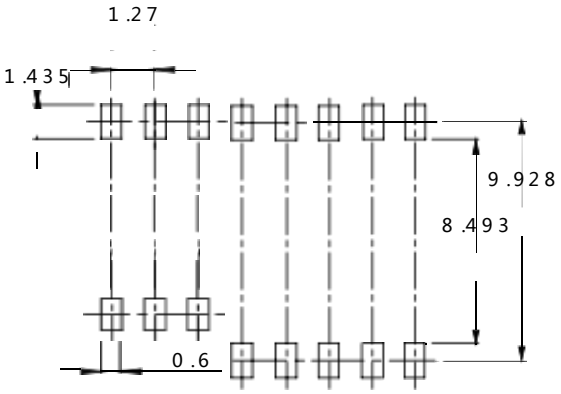
外形尺寸 OutIine Dimensions

SOP16



单位 unit: mm

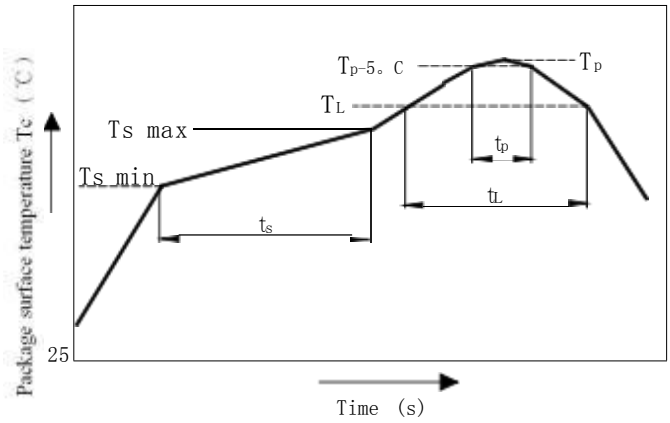
建议焊盘布局 Recommended Pad Layout



单位 unit: mm

注 :上图为产品正视图。
Note:The picture above is the front view of the product.

回流焊温度曲线图 SoIder RefIow profiIe

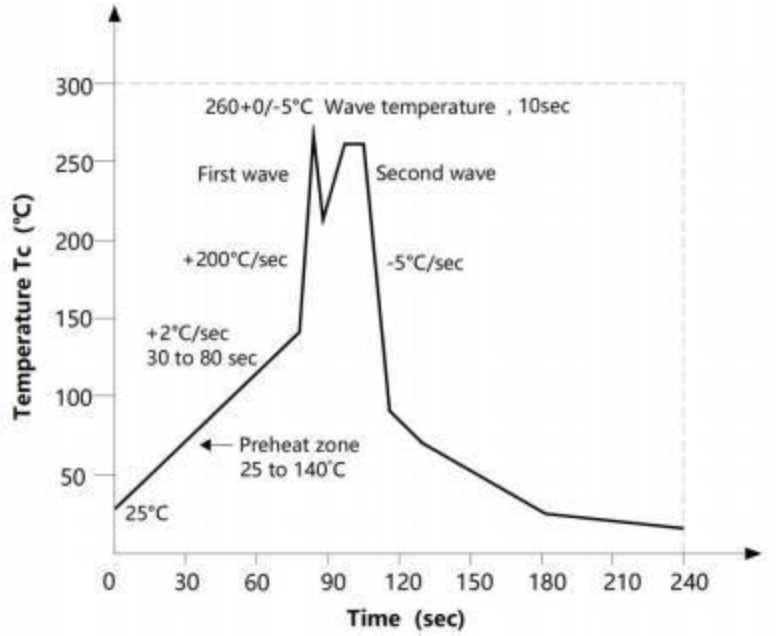


项目 Item	符号 Symbol	最小值 Min.	最大值 Max.	单位 Unit
预热温度 preheat Temperature	T_s	150	200	气
预热时间 preheat Time	t_s	60	120	s
升温速率 Ramp-Up Rate (T_L to T_p)	-		3	气/s
液相线温度 Liquidus Temperature	T_L	217		气
时间高于 T_L Time Above T_L	t_L	60	150	s
峰值温度 peak Temperature	T_p		260	气
T_c在(T_p-5)和 T_p 之间的时间 Time During which T_c Is Between (T_p-5) and T_p	t_p		30	s
降温速率 Ramp-down Rate(T_p to T_L)	-		6	气/s

注 :建议在所示的温度和时间条件下进行回流焊 ，最多不能超过三次。

Note:Reflow soldering is recommended at the temperatures and times shown, no more than three times.

波峰焊温度曲线图 wave SOIdering prOfiIe



手工烙铁焊接 SOIdering with hand SOIdering irOn

A. 手工烙铁焊仅用于产品返修或样品测试；
Hand soldering iron is only used for product rework or sample testing;

B. 手工烙铁焊要求 :温度 360气 士 5气，时间<3s。
Manual soldering method Temperature: 360气 士 5气, within 3s.

包装 packing

.汇总表summarytable

封装试	包装形式	每卷数量	每盒数量	每箱数量	防静电包规格	注意
SOP16	Reel(φ330mm蓝盘)	850 个/卷	2 条/箱	10 盒/箱	450*390*0.1mm	防护带最小 200mm
packageType	ackingFom	Quanttyper Reel	QuantityperBOX	Quanttyper arton	ntistaticBagspecifcation	Note
SOP16	Reel(φ330mm Blue)	850pcs/reel	2reels/box	10boxes/ctn	450*390*0.1mm	Guard band 200mm min.

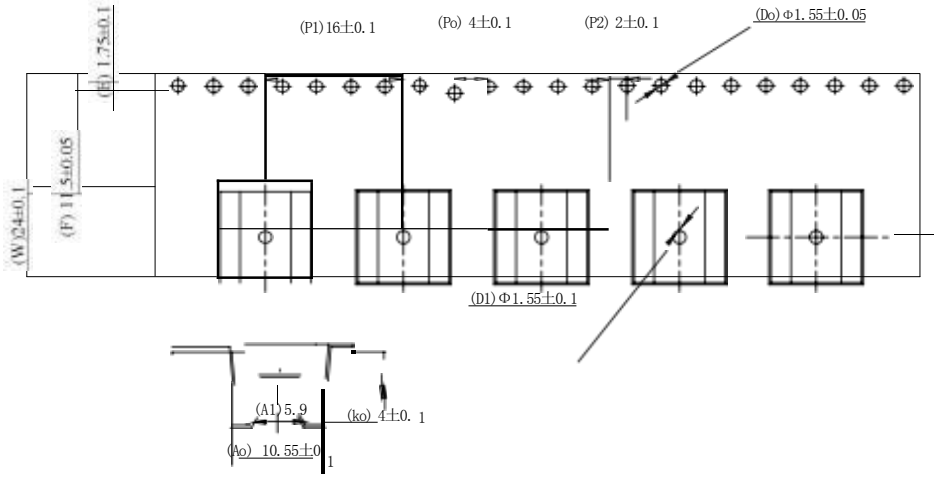
.编带包装Tape&Reel

1) 每卷数量: 850 只。
Qty/reel : 850pcs.

2) 每箱数量:17000 只。
Qty/ct n:17000pcs.

3) 内包装 :每盒 2 盘。
Inner packing:2 reels/box.

4) 示意图 Schematic :



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