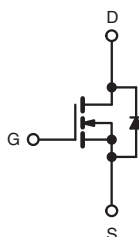
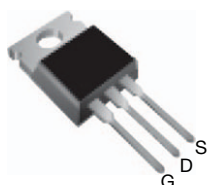


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.450
Q_g (Max.) (nC)	81	
Q_{gs} (nC)	20	
Q_{gd} (nC)	36	
Configuration	Single	

TO-220AB



N-Channel MOSFET

FEATURES

- Lower Gate Charge Q_g Results in Simpler Drive Requirements
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage
- Compliant to RoHS Directive 2002/95/EC



RoHS*
Available

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supplies
- High Speed Power Switching

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRFB13N50APbF SiHFB13N50A-E3
SnPb	IRFB13N50A SiHFB13N50A

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	500	V
Gate-Source Voltage			V _{GS}	± 30	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	14	A
		T _C = 100 °C		9.1	
Pulsed Drain Current ^a			I _{DM}	56	
Linear Derating Factor				2.0	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	560	mJ
Avalanche Current ^a			I _{AR}	14	A
Repetitive Avalanche Energy ^a			E _{AR}	25	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	250	W
Peak Diode Recovery dV/dt ^c			dV/dt	9.2	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	
Mounting Torque	6-32 or M3 screw			10	
				1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 5.7\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 14\text{ A}$, $dV/dt = 7.6\text{ V/ns}$ (see fig. 12a).
- $I_{SD} \leq 14\text{ A}$, $dI/dt \leq 250\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greasd Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.50	

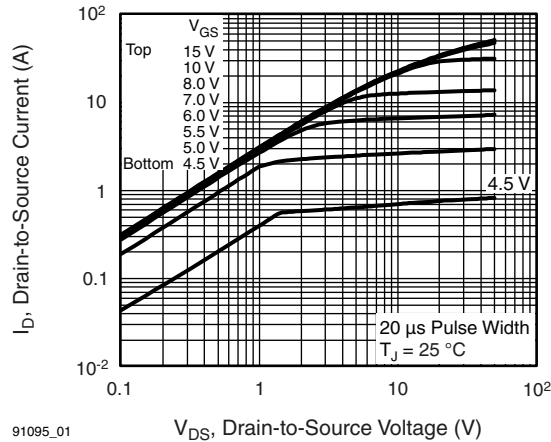
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.55	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 8.4 A ^b	-	-	0.450	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 8.4 A		8.1	-	-	S
Dynamic							
Input Capacitance	C _{ISS}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1910	-	pF
Output Capacitance	C _{OSS}			-	290	-	
Reverse Transfer Capacitance	C _{RSS}			-	11	-	
Output Capacitance	C _{OSS}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	2730	-	
			V _{DS} = 400 V, f = 1.0 MHz	-	82	-	
Effective Output Capacitance	C _{OSS} eff.	V _{DS} = 0 V to 400 V ^c		-	160	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 14 A, V _{DS} = 400 V, see fig. 6 and 13 ^b	-	-	81	nC
Gate-Source Charge	Q _{gs}			-	-	20	
Gate-Drain Charge	Q _{gd}			-	-	36	
Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V	V _{DD} = 250 V, I _D = 14 A, R _g = 7.5 Ω, see fig. 10 ^b	-	15	-	ns
Rise Time	t _r			-	39	-	
Turn-Off Delay Time	t _{d(off)}			-	39	-	
Fall Time	t _f			-	31	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	14	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	56	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 14 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 14 A, T _J = 125 °C, di/dt = 100 A/μs ^b		-	370	550	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	4.4	6.5	μC
Body Diode Reverse Recovery Current	I _{RRM}			-	21	31	A
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

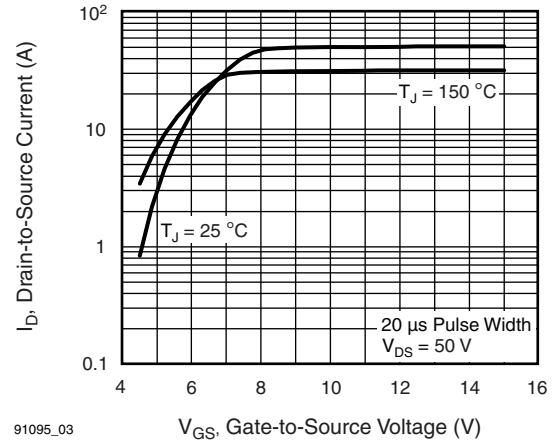
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



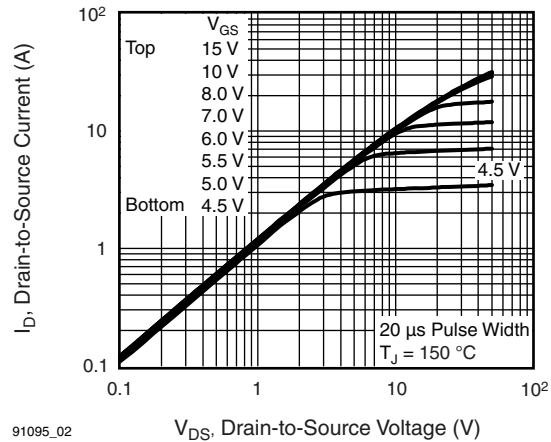
91095_01

Fig. 1 - Typical Output Characteristics



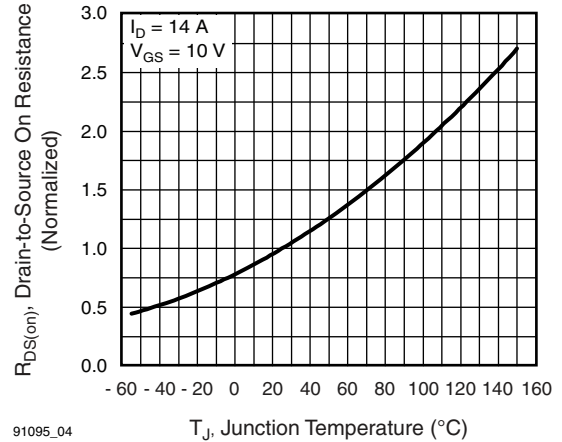
91095_03

Fig. 3 - Typical Transfer Characteristics



91095_02

Fig. 2 - Typical Output Characteristics



91095_04

Fig. 4 - Normalized On-Resistance vs. Temperature

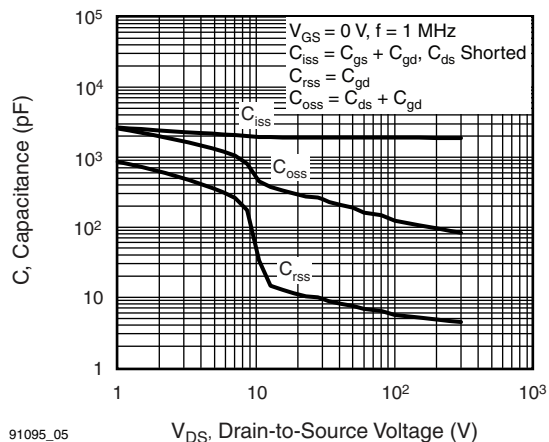


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

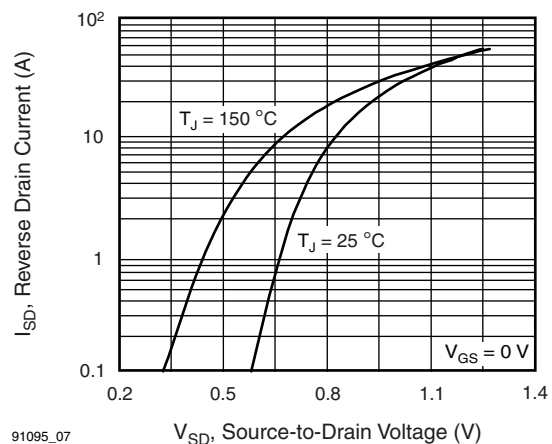


Fig. 7 - Typical Source-Drain Diode Forward Voltage

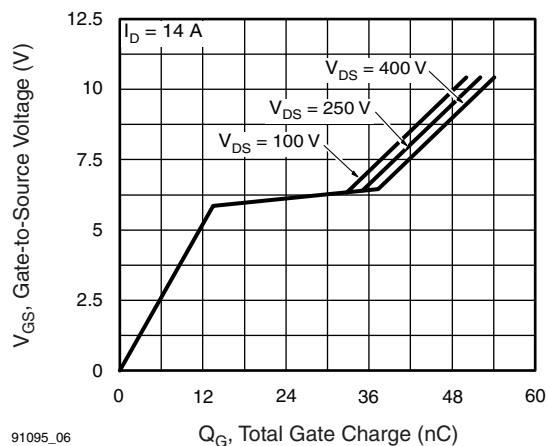


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

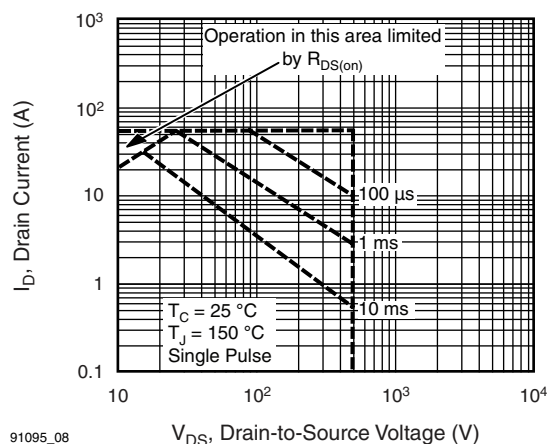


Fig. 8 - Maximum Safe Operating Area

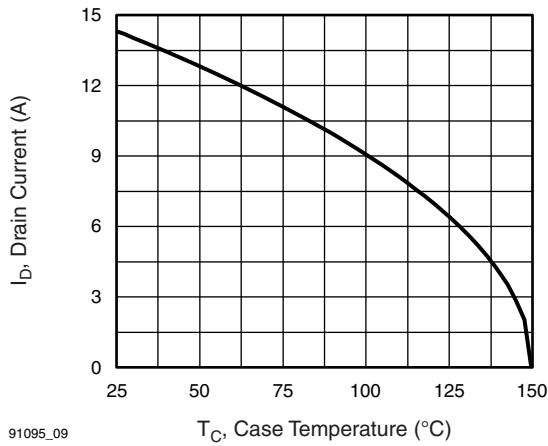


Fig. 9 - Maximum Drain Current vs. Case Temperature

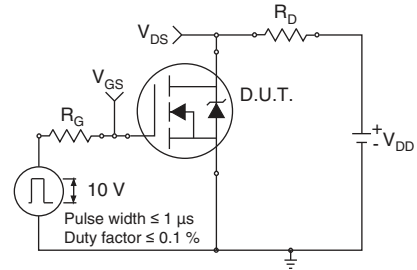


Fig. 10a - Switching Time Test Circuit

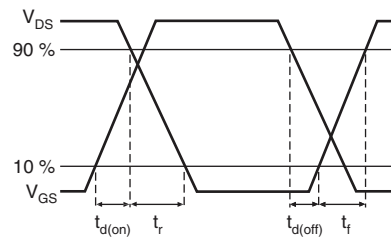


Fig. 10b - Switching Time Waveforms

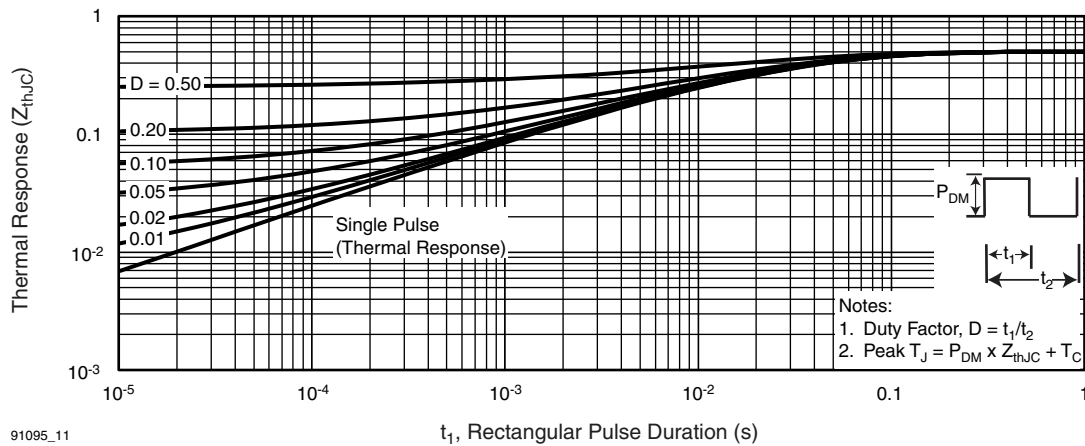


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

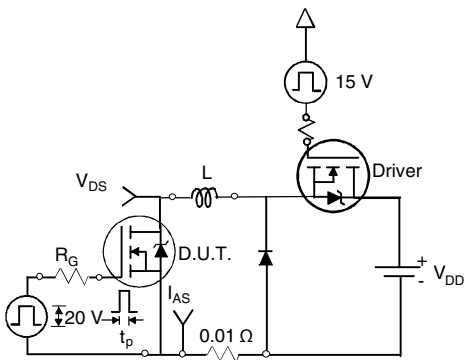


Fig. 12a - Unclamped Inductive Test Circuit

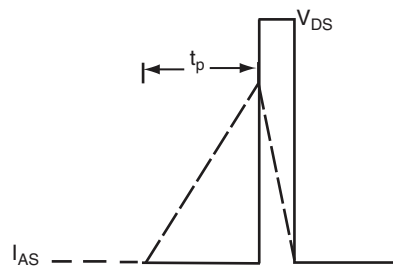


Fig. 12b - Unclamped Inductive Waveforms

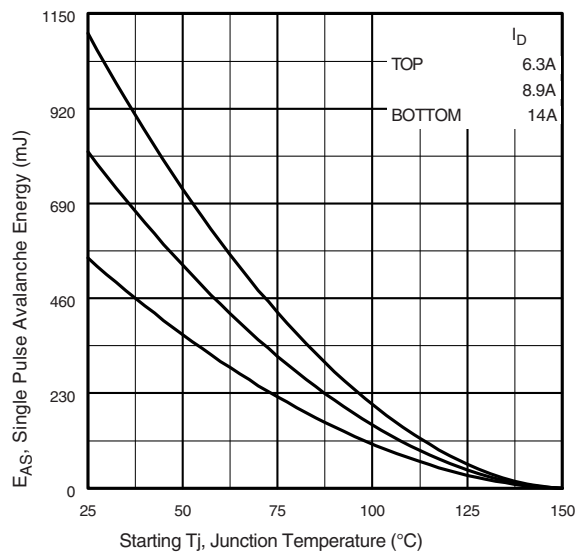


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

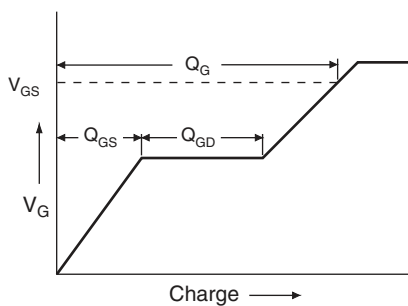


Fig. 13a - Basic Gate Charge Waveform

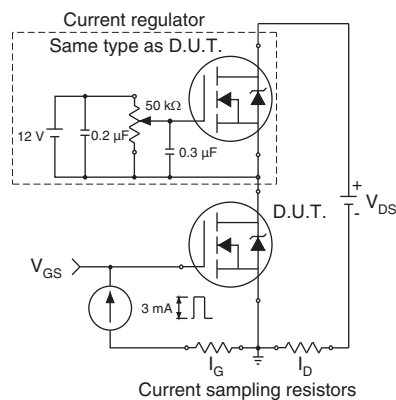


Fig. 13b - Gate Charge Test Circuit

Circuit layout considerations

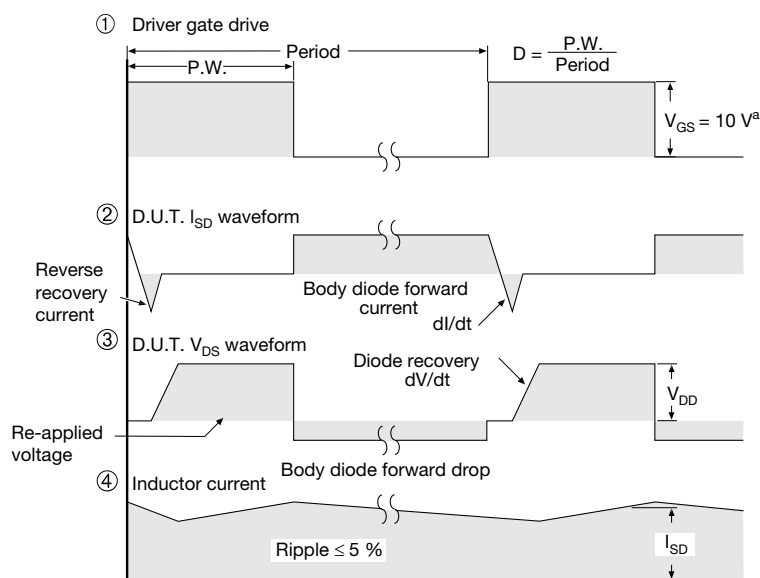
- Low stray inductance
- Ground plane
- Low leakage inductance current transformer

Annotations:

- ①: Pulse generator
- ②: Driver MOSFET
- ③: D.U.T. (Device Under Test)
- ④: Load resistor

Labels:

- D.U.T. (Device Under Test)
- R_g (Gate resistor)
- V_{DD} (DC supply voltage)



a. $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 14 - For N-Channel

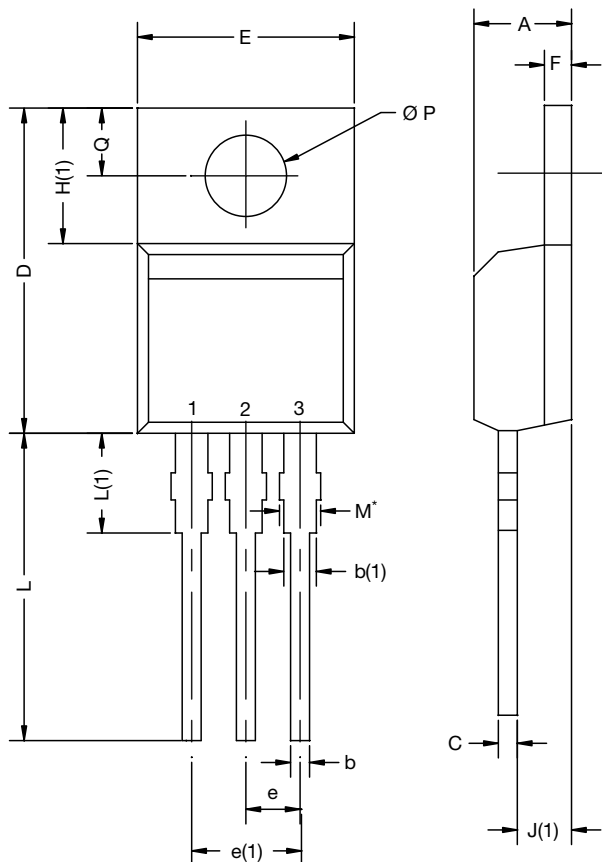
IRFB13N50A, SiHFB13N50A

Vishay Siliconix



reliability data, see www.vishay.com/ppg?91095.

TO-220-1



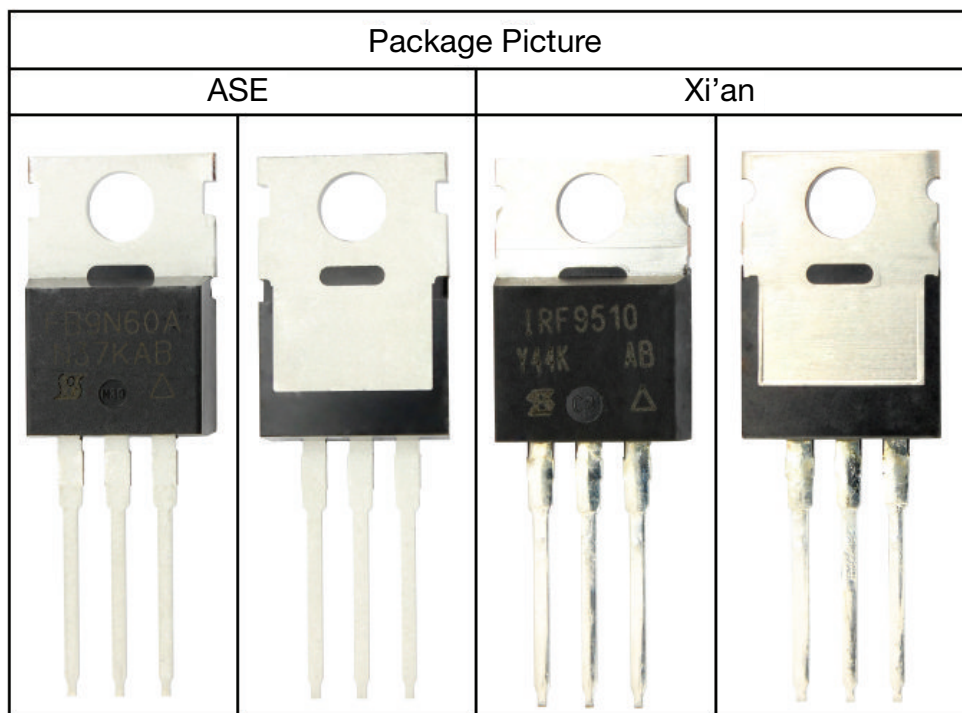
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0364-Rev. C, 14-Dec-15
DWG: 6031

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture





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