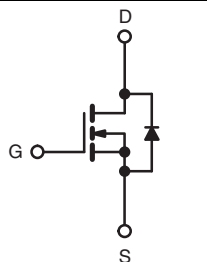
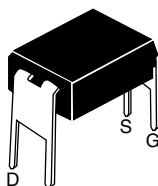


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	50	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.10
Q_g (Max.) (nC)	24	
Q_{gs} (nC)	7.1	
Q_{gd} (nC)	7.1	
Configuration	Single	

HVMDIP


N-Channel MOSFET

FEATURES

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Ease of Paralleling
- Excellent Temperature Stability
- Compliant to RoHS Directive 2002/95/EC


RoHS*
COMPLIANT

DESCRIPTION

The HVMDIP technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HVMDIP design achieves very low on-state resistance combined with high transconductance and extreme device ruggedness. HVMDIPs feature all of the established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

The HVMDIP 4 pin, dual-in-line package brings the advantages of HVMDIPs to high volume applications where automatic PC board insertion is desirable, such as circuit boards for computers, printers, telecommunications equipment, and consumer products. Their compatibility with automatic insertion equipment, low-profile and end stackable features represent the state-of-the-art in power device packaging.

ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRFD020PbF SiHFD020-E3
SnPb	IRFD020 SiHFD020

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage ^a	V_{DS}	50	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current ^b	I_{DM}	19	W/ $^\circ\text{C}$
Linear Derating Factor		0.0080	
Inductive Current, Clamped	I_{LM}	19	A
Unclamped Inductive Current (Avalanche Current) ^c	I_L	2.2	
Maximum Power Dissipation	P_D	1.0	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

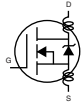
- $T_J = 25^\circ\text{C}$ to 150°C
- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 25\text{ V}$, starting $T_J = 25^\circ\text{C}$, $L = 100\text{ }\mu\text{H}$, $R_g = 25\text{ }\Omega$
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

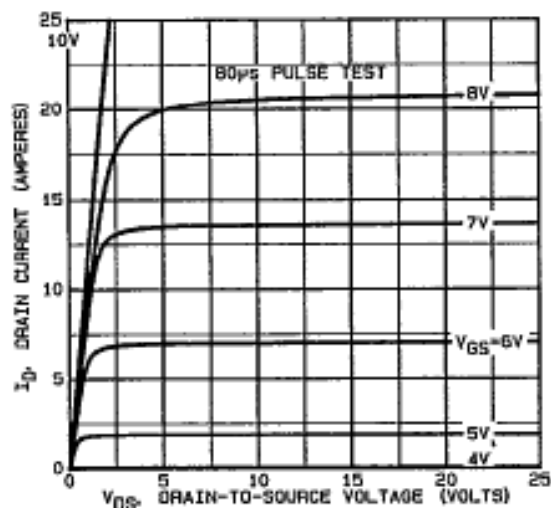
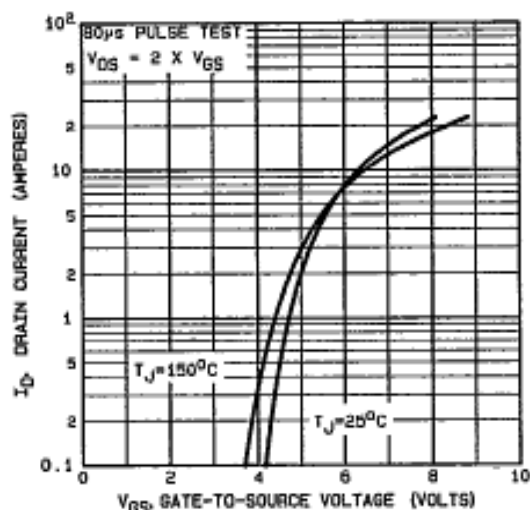
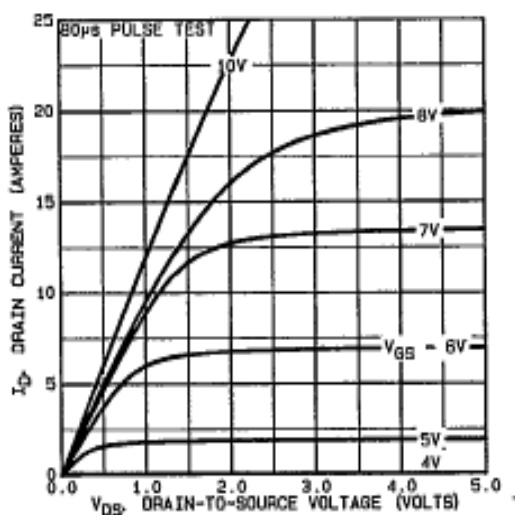
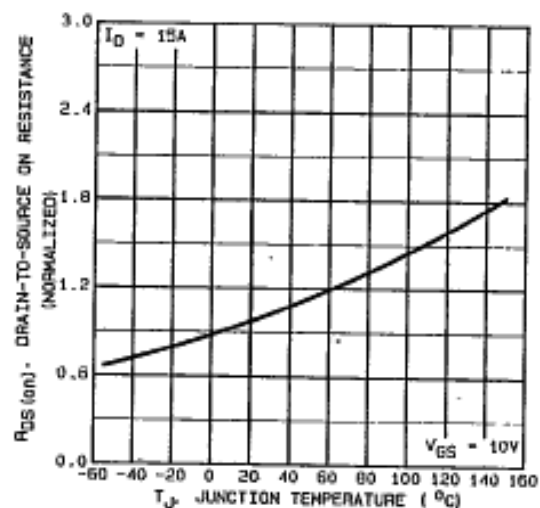
SPECIFICATIONS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		50	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 500	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = max. rating, V _{GS} = 0 V		-	-	250	μA
		V _{DS} = max. rating x 0.8, V _{GS} = 0 V, T _C = 125		-	-	1000	
On-State Drain Current ^b	I _{D(on)}	V _{GS} = 10 V	V _{DS} > I _{D(on)} x R _{DS(on)} max.	2.4	-	-	A
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.4 A	-	0.080	0.10	Ω
Forward Transconductance ^b	g _{fs}	V _{DS} = 20 V, I _D = 7.5 A		4.9	7.3	-	S
Dynamic							
Input Capacitance	C _{ISS}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz		-	400	-	pF
Output Capacitance	C _{OSS}			-	260	-	
Reverse Transfer Capacitance	C _{RSS}			-	44	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 15 A, V _{DS} = max. rating x 0.8	-	16	24	nC
Gate-Source Charge	Q _{gs}			-	4.7	7.1	
Gate-Drain Charge	Q _{gd}			-	4.7	7.1	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 25 V, I _D = 15 A, R _g = 18 Ω, R _D = 1.7 Ω		-	8.7	13	ns
Rise Time	t _r			-	55	83	
Turn-Off Delay Time	t _{d(off)}			-	16	24	
Fall Time	t _f			-	26	39	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L _S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	2.4	A
Pulsed Diode Forward Current ^c	I _{SM}			-	-	19	
Body Diode Voltage ^a	V _{SD}	T _C = 25 °C, I _S = 2.4 A, V _{GS} = 0 V		-	-	1.4	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 15 A, dI/dt = 100 A/μs		57	130	310	ns
Body Diode Reverse Recovery Charge	Q _{rr}			0.17	0.34	0.85	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.c. $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 100\text{ }\mu\text{H}$, $R_g = 25\text{ }\Omega$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

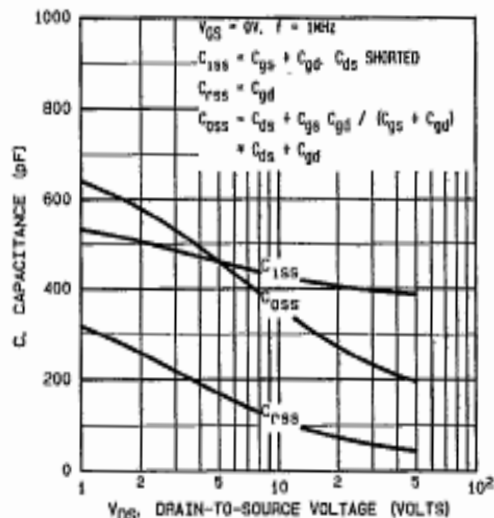


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

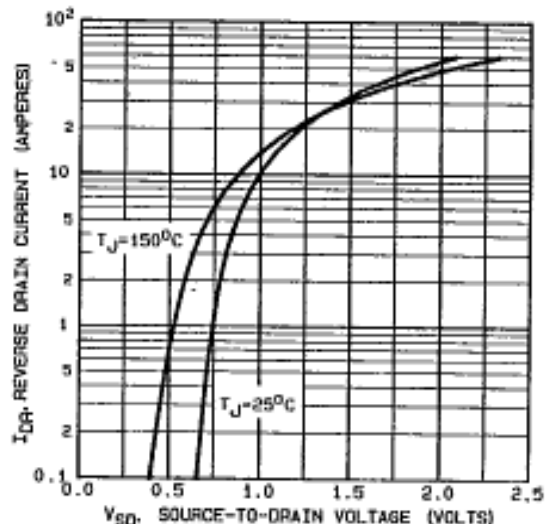


Fig. 7 - Typical Source-Drain Diode Forward Voltage

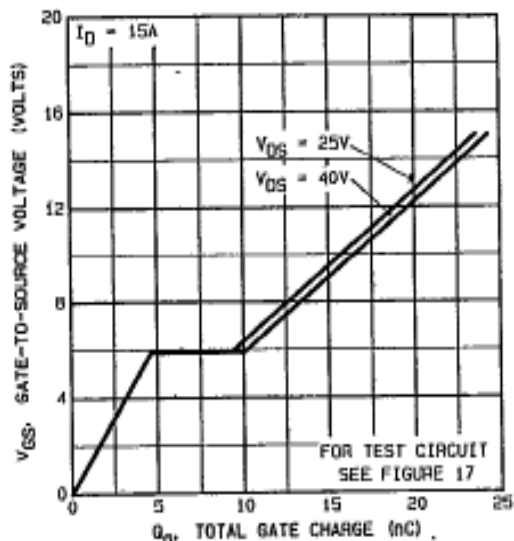


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

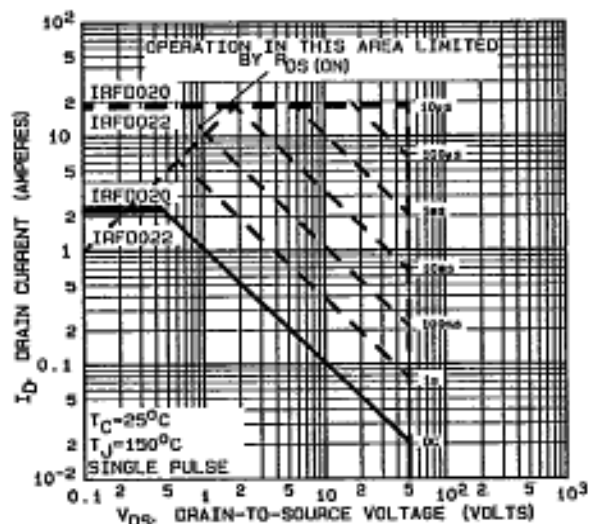


Fig. 8 - Maximum Safe Operating Area

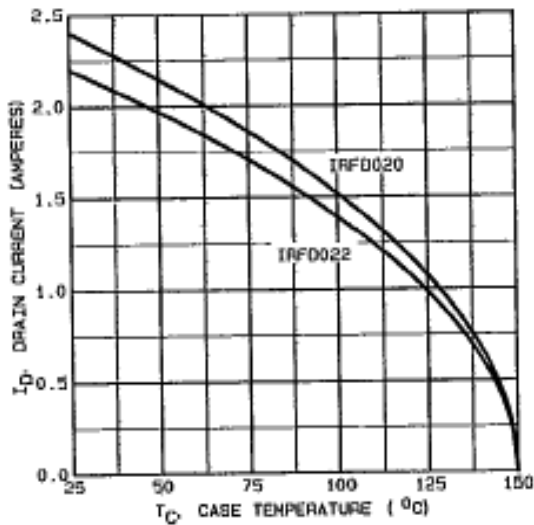


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

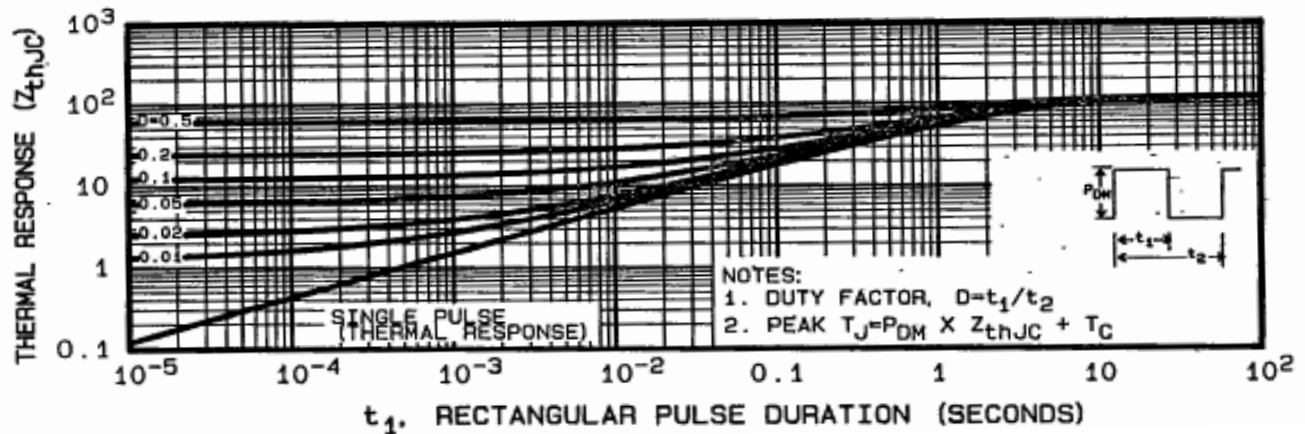


Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

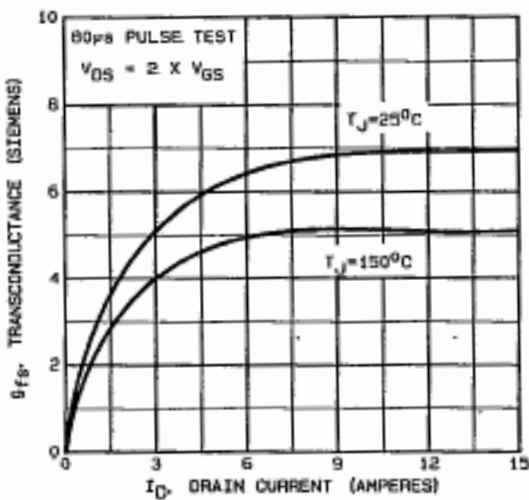


Fig. 11 - Typical Transconductance vs. Drain Current

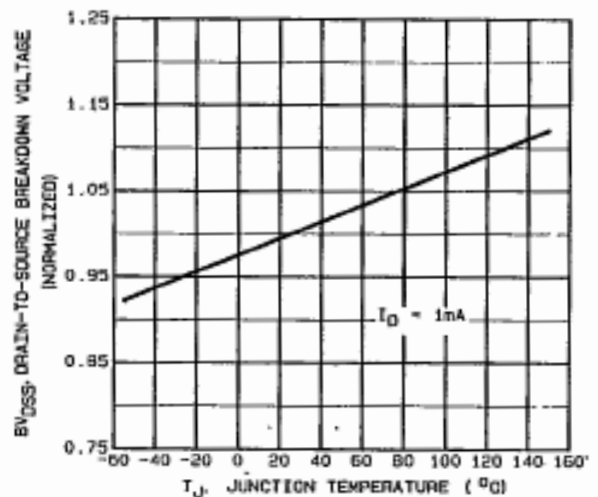


Fig. 12 - Breakdown Voltage vs. Temperature

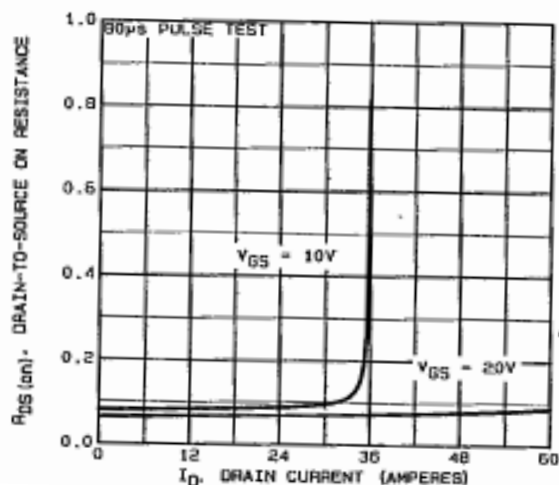


Fig. 13 - Typical on-Resistance vs. Drain Current

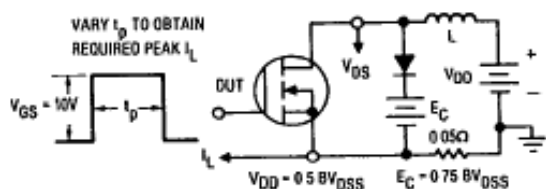


Fig. 14a - Clamped Inductive Test Circuit

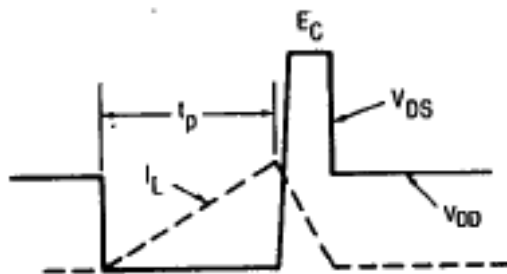


Fig. 14b - Clamped Inductive Waveforms

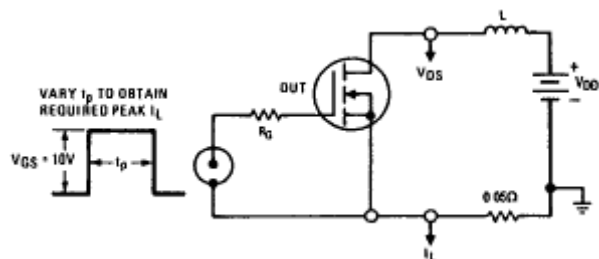


Fig. 15a - Unclamped Inductive Test Circuit

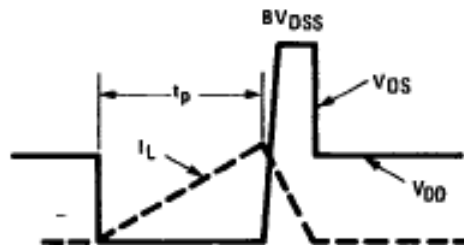


Fig. 15a - Unclamped Inductive Load Test Waveforms

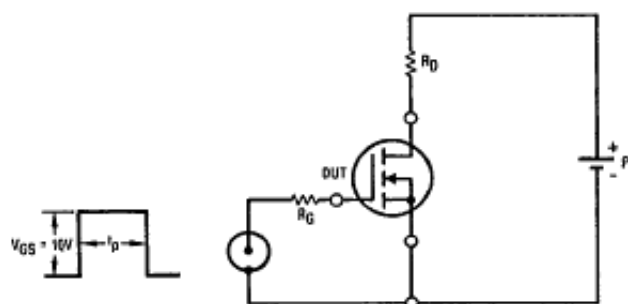


Fig. 16 - Switching Time Test Circuit

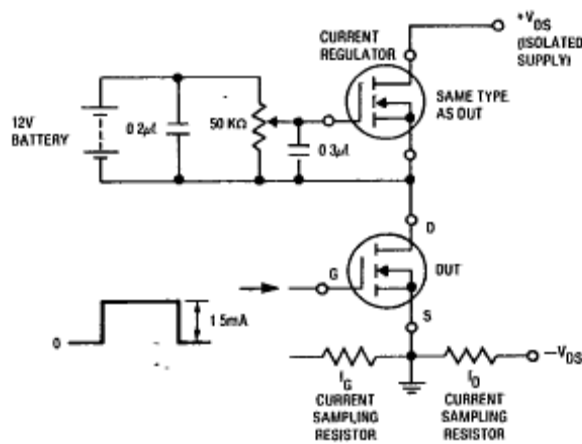


Fig. 17 - Gate Charge Test Circuit

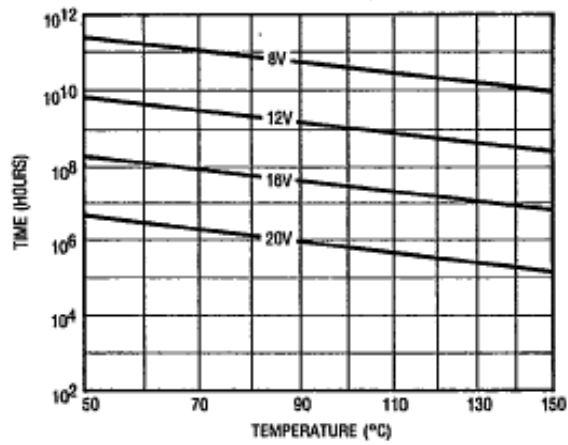


Fig. 18 - Typical Time to Accumulated 1 % Gate Failure

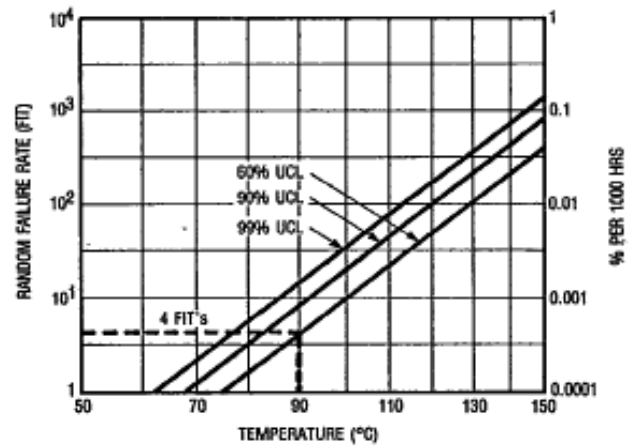
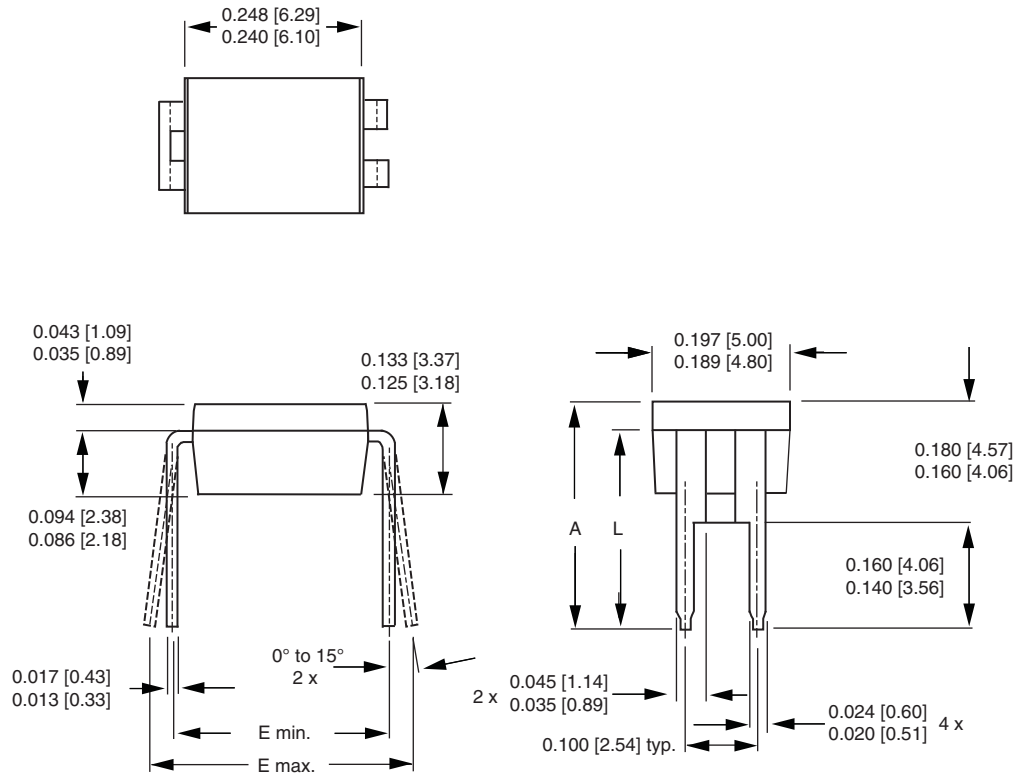


Fig. 19 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91465.

HVM DIP (High voltage)



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10
DWG: 5974

Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.



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