

MOSFET – Single, N-Channel, Logic Level, POWER trench®

30 V, 6.3 A, 25 mΩ

FDC655BN

General Description

This N-Channel Logic Level MOSFET is produced using onsemi's advanced POWER trench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- Max $R_{DS(ON)}$ = 25 mΩ @ V_{GS} = 10 V, I_D = 6.3 A
- Max $R_{DS(ON)}$ = 33 mΩ @ V_{GS} = 4.5 V, I_D = 5.5 A
- Fast Switching
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- This Device is Pb-Free, Halide Free and is RoHS Compliant

MOSFET MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

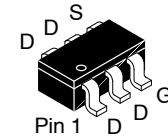
Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	–Continuous T_A = 25°C (Note 1a)	6.3	A
	–Pulsed	20	
P_D	Power Dissipation (Note 1a)	1.6	W
	(Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

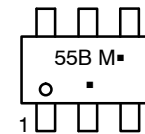
Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	°C/W

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
30 V	25 mΩ @ 10 V	6.3 A
	33 mΩ @ 4.5 V	



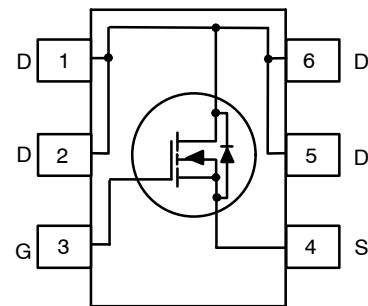
TSOT23 6-Lead
(SUPERSOT™ –6)
CASE 419BL

MARKING DIAGRAM



55B = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
FDC655BN	TSOT23–6 (Pb–Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FDC655BN

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V,	30	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	25	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	–	–	1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1	1.9	3	V
ΔV _{GS(th)} / ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	–5	–	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 6.3 A	–	21	25	mΩ
		V _{GS} = 4.5 V, I _D = 5.5 A	–	26	33	
		V _{GS} = 10 V, I _D = 6.3 A, T _J = 125°C	–	30	36	
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 6.3 A	–	35	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	–	470	620	pF
C _{oss}	Output Capacitance		–	100	130	pF
C _{rss}	Reverse Transfer Capacitance		–	60	90	pF
R _g	Gate Resistance		–	3.0	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	6	11	ns
t _r	Rise Time		–	2	10	ns
t _{d(off)}	Turn-Off Delay Time		–	15	26	ns
t _f	Fall Time		–	2	10	ns
Q _{g(Tot)}	Total Gate Charge	V _{GS} = 0 V to 10 V, V _{DD} = 15 V, I _D = 6.3 A	–	9	13	nC
Q _{g(Tot)}	Total Gate Charge	V _{GS} = 0 V to 5 V, V _{DD} = 15 V, I _D = 6.3 A	–	5	7	nC
Q _{gs}	Gate to Source Charge	V _{DD} = 15 V, I _D = 6.3 A	–	1.4	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	1.6	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain-Source Diode Forward Current		–	–	1.3	A
V _{SD}	Source-Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.3 A (Note 2)	–	0.8	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 6.3 A, di/dt = 100 A/μs	–	15	26	ns
Q _{rr}	Reverse Recovery Charge		–	4	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.
 - 78°C/W when mounted on a 1 in² pad of 2 oz copper on FR-4 board.
 - 156°C/W when mounted on a minimum pad.
- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

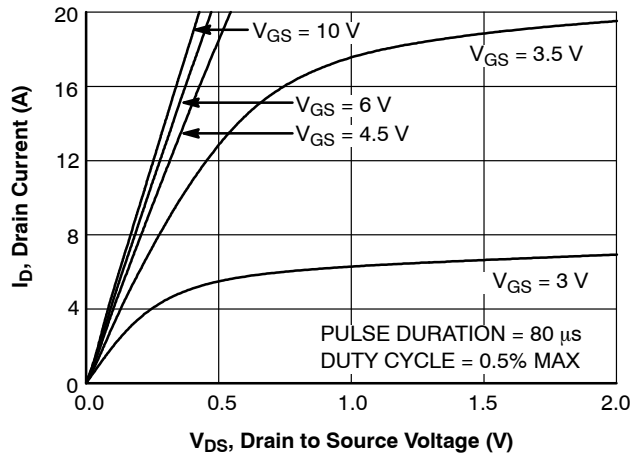


Figure 1. On Region Characteristics

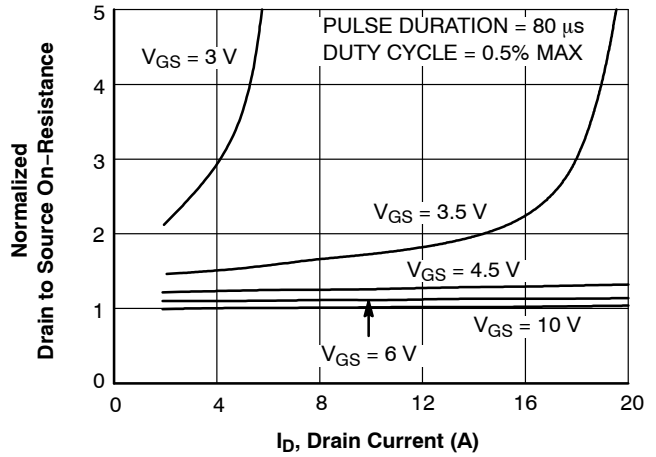


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

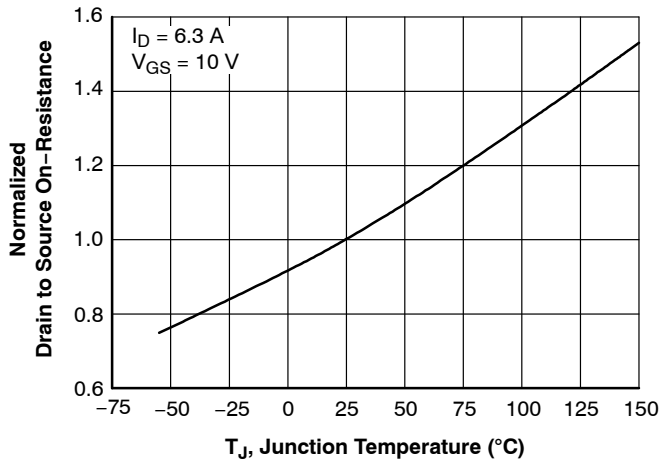


Figure 3. Normalized On Resistance vs. Junction Temperature

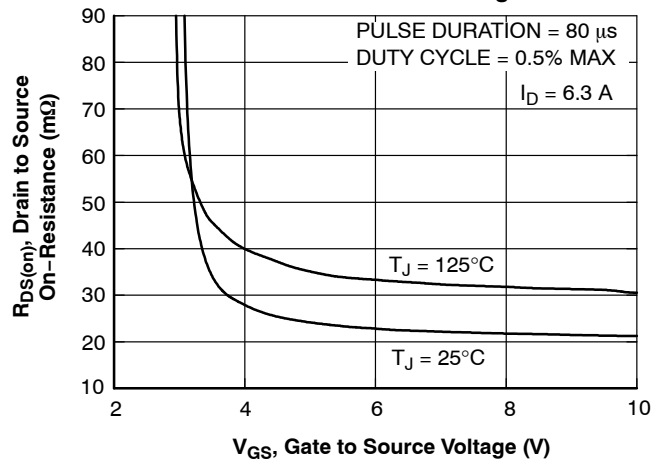


Figure 4. On-Resistance vs. Gate to Source Voltage

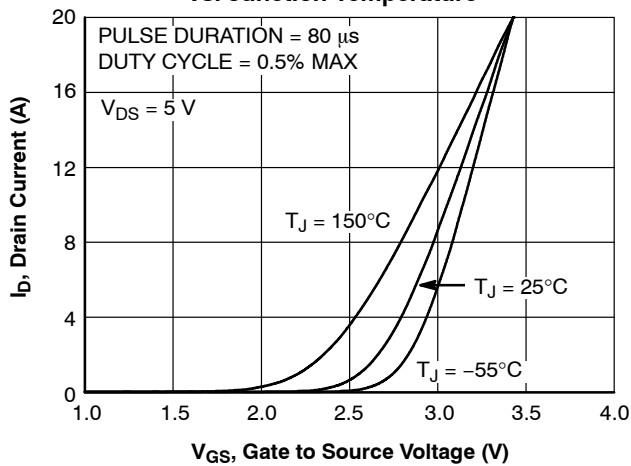


Figure 5. Transfer Characteristics

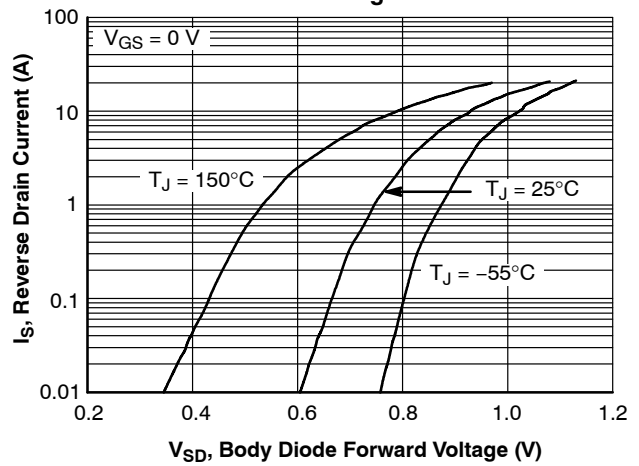


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

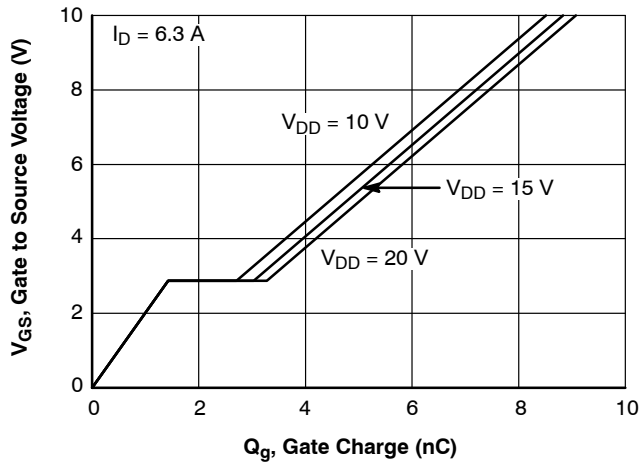


Figure 7. Gate Charge Characteristics

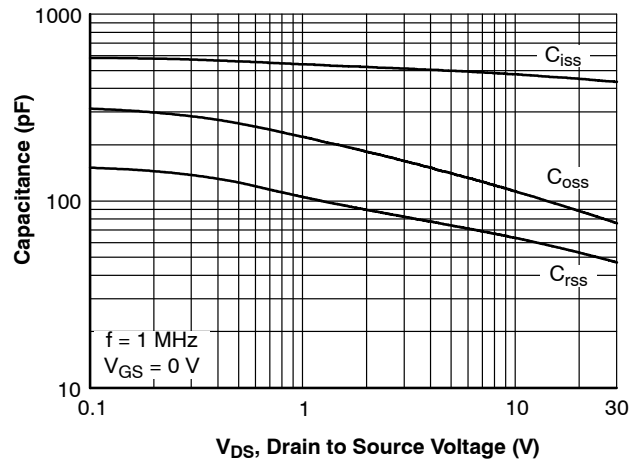


Figure 8. Capacitance vs. Drain to Source Voltage

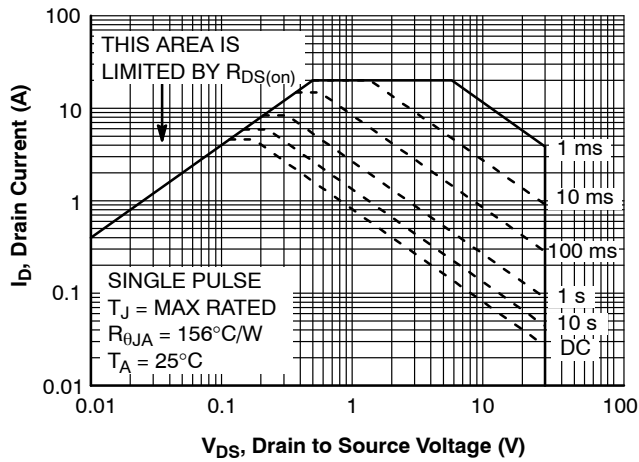


Figure 9. Forward Bias Safe Operating Area

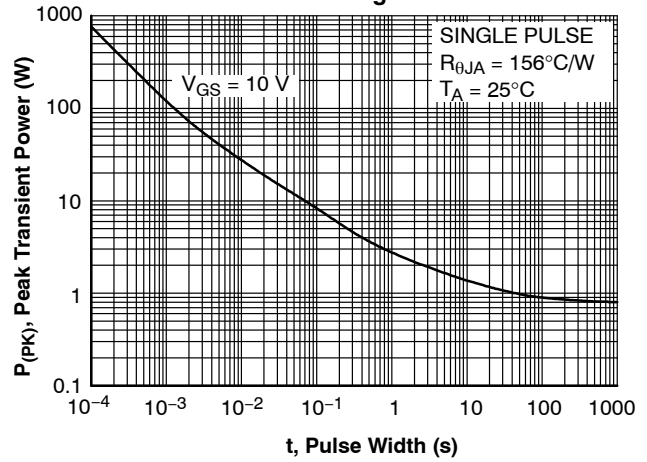


Figure 10. Single Pulse Maximum Power Dissipation

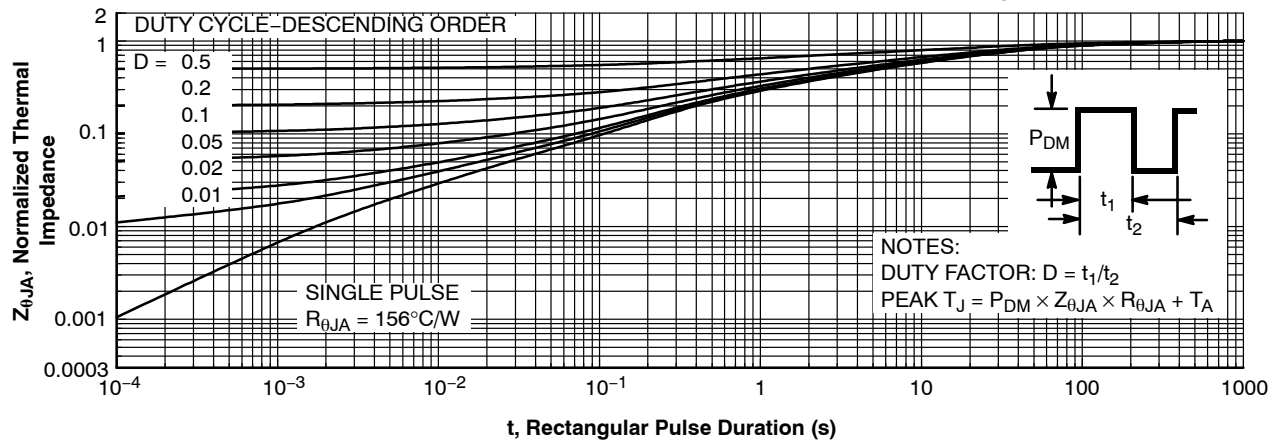


Figure 11. Junction-to-Ambient Transient Thermal Response Curve

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

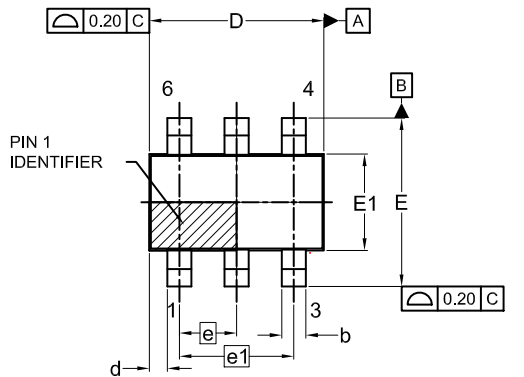
ON Semiconductor®



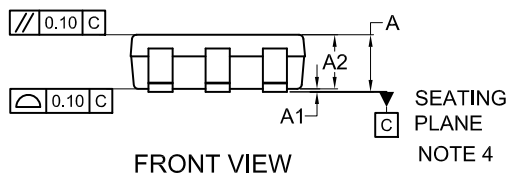
SCALE 2:1

TSOT23 6-Lead CASE 419BL ISSUE A

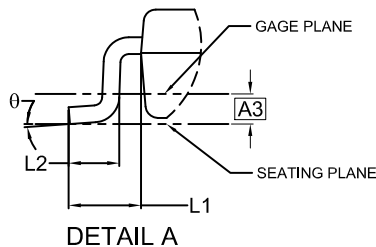
DATE 31 AUG 2020



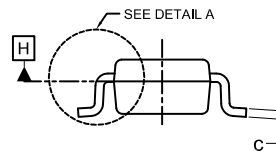
TOP VIEW



FRONT VIEW

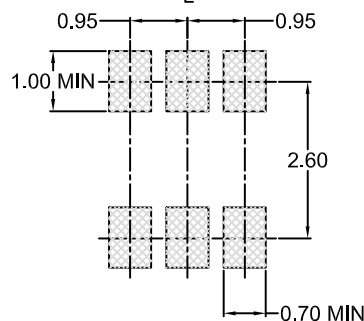


DETAIL A



SIDE VIEW

SYMM



LAND PATTERN
RECOMMENDATION

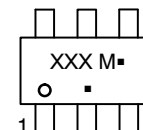
*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
Θ	0°	—	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSOT23 6-Lead	PAGE 1 OF 1

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