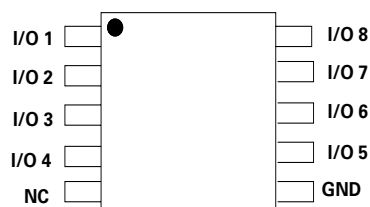


HF RoHS GREEN



The schematic shows a 4x4 grid of diodes. The columns are labeled I/O 1, I/O 2, I/O 3, and I/O 4 from left to right. The rows are labeled I/O 5, I/O 6, I/O 7, and I/O 8 from bottom to top. Each diode is oriented with its cathode towards the top and its anode towards the bottom. A central ground symbol is connected to the bottom row (I/O 5) and the second column (I/O 2).

Datasheet



Resources



Samples

The SP4060 integrates low capacitance diodes with an additional zener diode to protect each I/O pin against ESD and high surge events. This robust device can safely absorb up to 20A per IEC 61000-4-5 ($t_p=8/20\mu s$) without performance degradation and a minimum $\pm 30kV$ ESD per IEC 61000-4-2 International Standard. Their low loading capacitance also makes them ideal for protecting high speed signal pins.

- ESD, IEC 61000-4-2, $\pm 30\text{kV}$ contact, $\pm 30\text{kV}$ air
- EFT, IEC 61000-4-4, 40A (5/50ns)
- Lightning, IEC 61000-4-5, 20A (8/20us)
- Low capacitance of 4.4pF (TYP) per I/O
- Low leakage current of $1\mu\text{A}$ (MAX) at 2.5V
- Moisture Sensitivity Level (MSL-1)

- LCD/PD TVs
- Desktops
- Game Consoles
- Set Top Boxes
- Notebooks

The diagram illustrates the LVDS interface connection. On the left, the **LVDS Interface** block has pins labeled CLK+, CLK-, A0+, A0-, A1+, A1-, A2+, and A2-. On the right, the **LVDS Controller** block is shown. The **SP4060-08ATG** chip is positioned between them. The connections are as follows:

- CLK+ is connected to the top-left pin of the SP4060-08ATG.
- CLK- is connected to the second pin from the top-left of the SP4060-08ATG.
- A0+ is connected to the third pin from the top-left of the SP4060-08ATG.
- A0- is connected to the fourth pin from the top-left of the SP4060-08ATG.
- A1+ is connected to the fifth pin from the top-left of the SP4060-08ATG.
- A1- is connected to the sixth pin from the top-left of the SP4060-08ATG.
- A2+ is connected to the seventh pin from the top-left of the SP4060-08ATG.
- A2- is connected to the eighth pin from the top-left of the SP4060-08ATG.
- The bottom-left pin of the SP4060-08ATG is connected to **Shield GND**.
- The bottom-right pin of the SP4060-08ATG is connected to **Shield GND**.
- The signal lines from the SP4060-08ATG are connected to the LVDS Controller. A specific signal line is labeled **Signal**.

The area to the left of the LVDS Interface is labeled *Outside World*.

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{PP}	Peak Current ($t_p=8/20\mu s$)	20.0	A
P_{PK}	Peak Pulse Power ($t_p=8/20\mu s$)	300	W
T_{OP}	Operating Temperature	-40 to 125	°C
T_{STOR}	Storage Temperature	-55 to 150	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

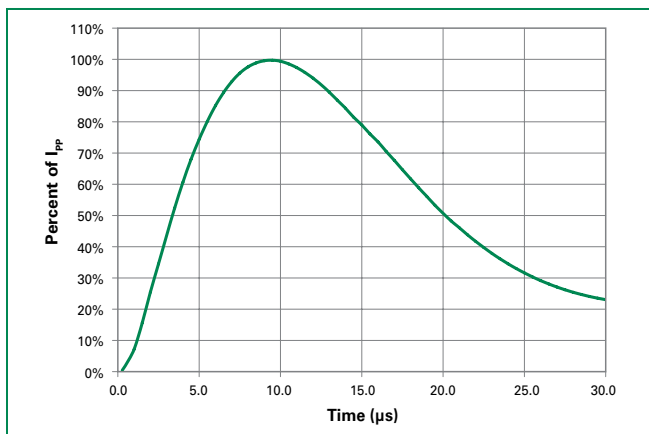
Parameter	Rating	Units
Storage Temperature Range	-55 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s)	260	°C

Electrical Characteristics ($T_{OP}=25^{\circ}C$)

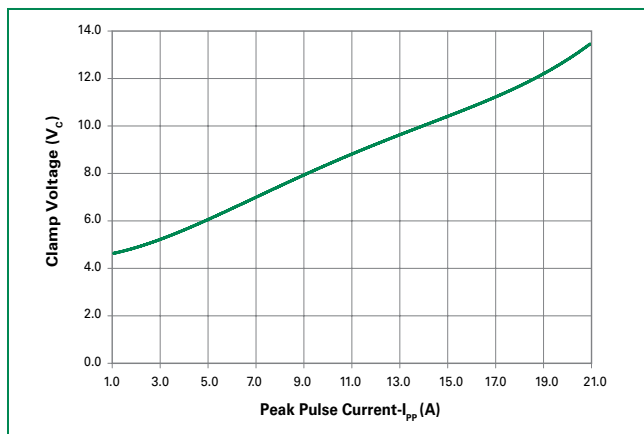
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Standoff Voltage	V_{RWM}				2.5	V
Snap Back Voltage	V_{SB}	$I_{SB}=50mA$	2.0			V
Reverse Leakage Current	I_{LEAK}	$V_R=2.5V$, I/O to GND		0.5	1.0	μA
Clamp Voltage ¹	V_C	$I_{PP}=1A$, $t_p=8/20\mu s$, Fwd		4.5	5.5	V
		$I_{PP}=5A$, $t_p=8/20\mu s$, Fwd		6.0	7.2	V
		$I_{PP}=10A$, $t_p=8/20\mu s$, Fwd		8.0	9.6	V
		$I_{PP}=20A$, $t_p=8/20\mu s$, Fwd		12.5	15.0	V
ESD Withstand Voltage ¹	V_{ESD}	IEC61000-4-2 (Contact)	± 30			kV
		IEC61000-4-2 (Air)	± 30			kV
Diode Capacitance ¹	$C_{I/O-GND}$	Reverse Bias=0V		4.4	5.0	pF
Diode Capacitance ¹	$C_{I/O-I/O}$	Reverse Bias=0V		2.2		pF

Note: ¹ Parameter is guaranteed by design and/or device characterization.

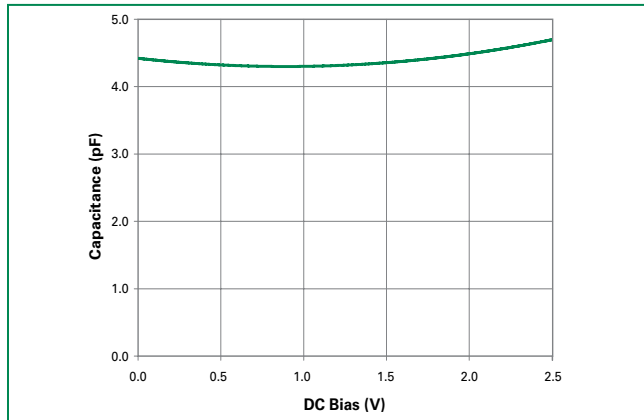
8/20 μs Pulse Waveform



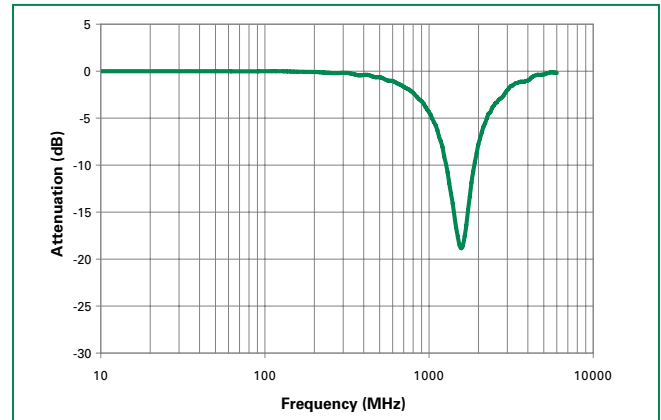
Clamping Voltage vs. I_{PP}



Capacitance vs. Bias

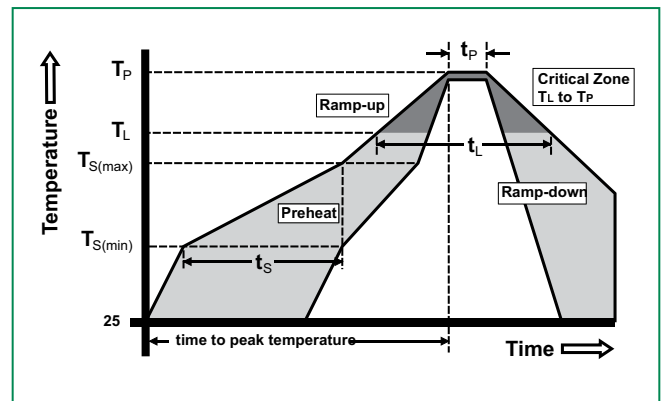


Insertion Loss (S21) I/O to GND

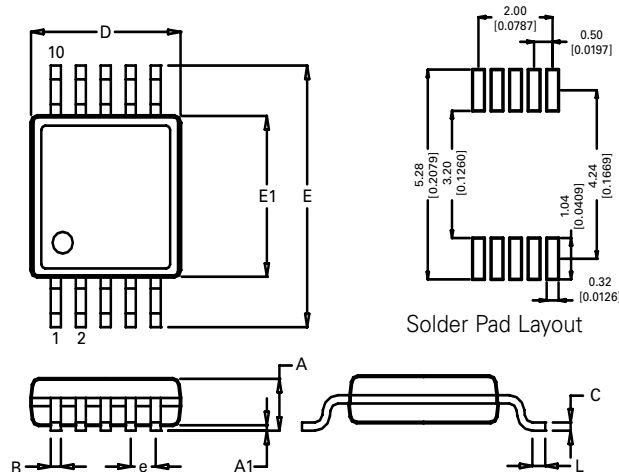


Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	- Temperature Min ($T_{s(min)}$)	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{s(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	- Temperature (T_L) (Liquidus)	217°C
	- Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_p)		260 $^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_p)		8 minutes Max.
Do not exceed		260°C

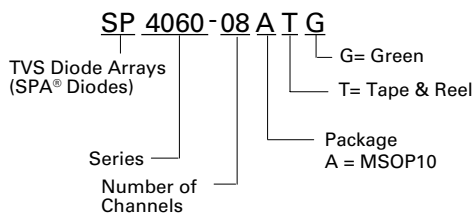


Package Dimensions — MSOP10

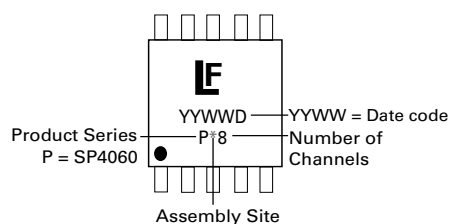


Package	MSOP			
Pins	10			
JEDEC	MO-187			
	Millimeters		Inches	
DIM	Min	Max	Min	Max
A	-	1.10	-	0.043
A1	0.00	0.15	0.000	0.006
B	0.17	0.27	0.007	0.011
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
E	4.67	5.10	0.184	0.200
E1	2.90	3.10	0.114	0.122
e	0.50 BSC		0.020 BSC	
L	0.40	0.80	0.016	0.032

Part Numbering System



Part Marking System



Product Characteristics

Lead Plating	Pre-Plated Frame
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Substitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL 94 V-0

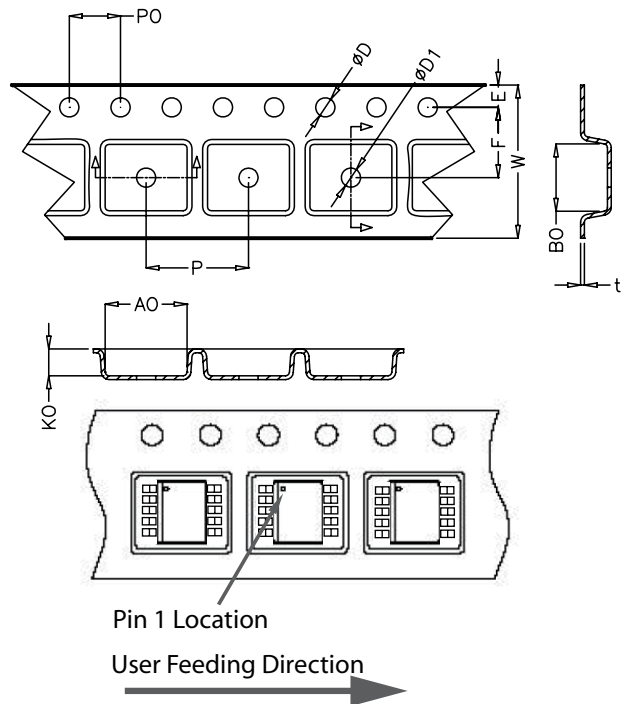
Notes :

1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP4060-08ATG	MSOP10	P*8	4000

Embossed Carrier Tape & Reel Specification — MSOP-10



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.40	5.60	0.213	0.220
D	1.50	1.60	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.90	4.10	0.154	0.161
10P0	40.0 ± 0.20		1.574 ± 0.008	
W	11.90	12.10	0.469	0.476
P	7.90	8.10	0.311	0.319
A0	5.20	5.40	0.205	0.213
B0	3.20	3.40	0.126	0.134
K0	1.20	1.40	0.047	0.055
t	0.30 ± 0.05		0.012 ± 0.002	

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