

## **500V N-Channel Enhancement Mode MOSFET**

#### Description

The SX5N50D-L is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

#### **General Features**

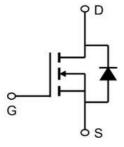
V<sub>DS</sub> = 500V I<sub>D</sub> =5.0A

 $R_{DS(ON)} < 1.85\Omega @ V_{GS}=10V$ 

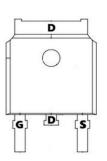
#### **Application**

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)







#### Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage (VGS = 0V)	500	V
<b>l</b> o@Tc=25℃	Continuous Drain Current, V <sub>GS</sub> @ 10V¹	5	Α
lo@Tc=75°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	3	Α
IDM	Pulsed Drain Current (note1)	20	Α
VGS	Gate-Source Voltage	±30	V
EAS	Single Pulse Avalanche Energy (note2)	137	mJ
P <b>o@T</b> c= <b>25</b> ℃	Total Power Dissipation <sup>4</sup>	83	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	°C
RthJC	Thermal Resistance, Junction-to-Case	1.5	°C/W
RthJA	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

1



# **500V N-Channel Enhancement Mode MOSFET**

## Electrical Characteristics (TJ=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	lb = 250mA, Vgs = 0V	500	-	-	V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500V, V <sub>GS</sub> = 0V	-	-	1.0	mA
IGSS	Gate-Body Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±30V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250mA	2.0	3.0	4.0	V
RDS(ON)	Static Drain-Source ON-Resistance <sup>(4)</sup>	V <sub>G</sub> S = 10V, I <sub>D</sub> = 2.5A	-	1.55	1.85	mΩ
Ciss	Input Capacitance		-	615	-	pF
Coss	Output Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1MHz	-	67	-	pF
Crss	Reverse Transfer Capacitance	1111112	-	10	-	pF
Qg	Total Gate Charge	V <sub>GS</sub> = 0 to 10V V <sub>DS</sub> = 250V,	-	14	-	nC
Qgs	Gate Source Charge		_	3.3	-	nC
Qgd	Gate Drain("Miller") Charge	1 ID - 2A	_	4	-	nC
td(on)	Turn-On DelayTime	V <sub>G</sub> S = 10V, V <sub>DD</sub> = 240V	-	12	-	ns
tr	Turn-On Rise Time		-	17	-	ns
td(off)	Turn-Off DelayTime	lo= 2A, Rgen = 24W	-	45	-	ns
tf	Turn-Off Fall Time		-	25	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	5	Α
ISM	Maximum Pulsed Drain to Source Diode Forward Current		_	-	20	Α
VSD	Drain to Source Diode Forward Voltage	V <sub>G</sub> s = 0V, I <sub>S</sub> = 5A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time		-	340	-	ns
Qrr	Body Diode Reverse Recovery Charge	l⊧ = 5A, di/dt = 100A/us	-	2.9	-	μC

#### Note:

- 1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
- 2. The EAS data shows Max. rating . IAS = 2.4A, VDD = 50V, RG = 25  $\Omega$ , Starting TJ = 25  $^{\circ}$ C
- 3、The test condition is Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 1%
- 4. The power dissipation is limited by 150  $\!^{\circ}\!\!$  Cjunction temperature
- 5、The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

2

www.sxsemi.com



## **Typical Characteristics**

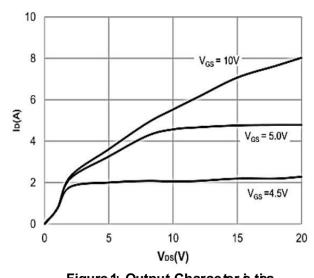


Figure 1: Output Character is tics

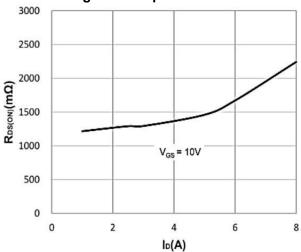


Figure 3:On-resistance vs. Drain Current

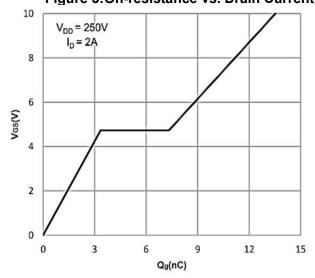
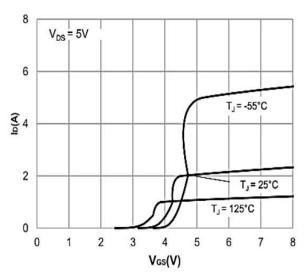


Figure 5: Gate Charge Characteristics



**Figure 2: Typical Transfer Characteristics** 

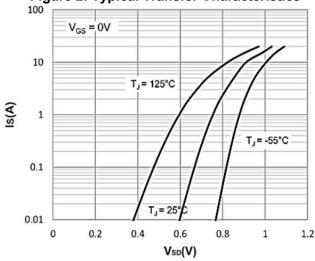
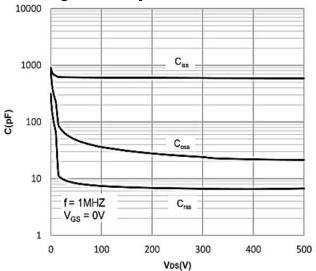


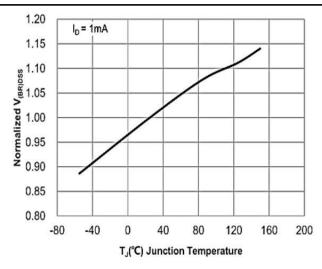
Figure 4: Body Diode Characteristics



**Figure 6: Capacitance Characteristics** 



### **Typical Characteristics**



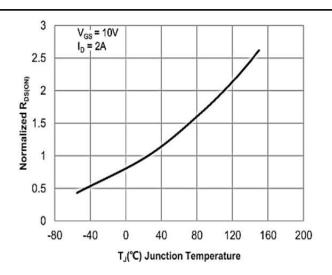


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

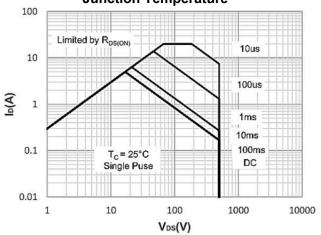


Figure 8: Normalized on Resistance vs Junction Temperature

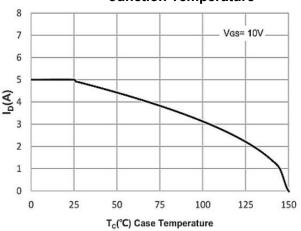


Figure 9: Maximum Safe Operating Are

Figure 10: Maximum Continuous Drain Current vs. Case Temperature

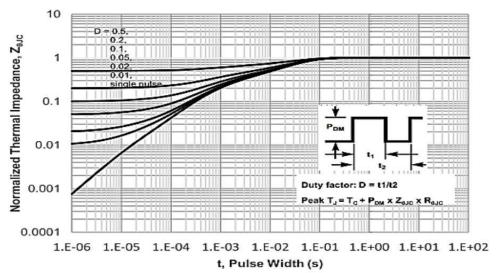
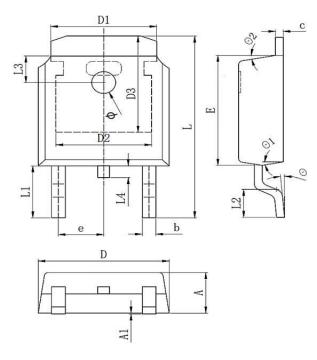


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ca

4



# Package Mechanical Data-TO-252-3L



Completel	Dim in mm			
Symbol	Min	Тур	Max	
A	2.1	2.3	2.5	
A1	0	0.064	0.128	
b	0.64	0.75	0.86	
С	0.45	0.52	0.6	
D	6.4	6.6	6.8	
D1	5.33REF			
D2	4.83REF			
D3	5.25REF			
Е	5.9	6.1	6.3	
е	2.286TYP			
L	9.8	10.1 10.4		
L1	2.888REF			
L2	1.4	1.5 1.7		
L3	1.65REF			
L4	0.6	0.8	1	
ф	1.1	1.2	1.3	
θ	0°		10°	
θ1	5°		10°	
θ2	5°		10°	

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	TO-252-3L		2500

5