

NTMFS4825NFE

Power MOSFET

30 V, 171 A, Single N-Channel, SO-8 FL

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Includes Schottky Diode
- Optimized Gate Charge to Minimize Switching Losses
- Dual Sided Cooling Capability
- These are Pb-Free Device

Applications

- CPU Power Delivery
- DC-DC Converters
- Low Side Switching

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	30	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	29	A
		$T_A = 85^{\circ}\text{C}$		21	
$T_A = 25^{\circ}\text{C}$		P_D	2.74	W	
$T_A = 25^{\circ}\text{C}$		I_D	47	A	
			34		
$T_A = 25^{\circ}\text{C}$		P_D	7.3	W	
$T_A = 25^{\circ}\text{C}$		I_D	17	A	
			12		
$T_A = 25^{\circ}\text{C}$		P_D	0.95	W	
$T_C = 25^{\circ}\text{C}$		I_D	171	A	
			123		
$T_C = 25^{\circ}\text{C}$		P_D	96.2	W	
Pulsed Drain Current	$t_p=10\mu\text{s}$	$T_A = 25^{\circ}\text{C}$	I_{DM}	288	A
Current limited by package		$T_A = 25^{\circ}\text{C}$	$I_{Dmaxpkg}$	100	A
Operating Junction and Storage Temperature		T_J, T_{STG}	-40 to +150	$^{\circ}\text{C}$	
Source Current (Body Diode)		I_S	120	A	
Drain to Source dV/dt		dV/dt	6	V/ns	
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 50\text{ V}, V_{GS} = 10\text{ V}, I_L = 50\text{ A}_{pk}, L = 0.3\text{ mH}, R_G = 25\text{ }\Omega$)		EAS	375	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^{\circ}\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

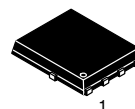
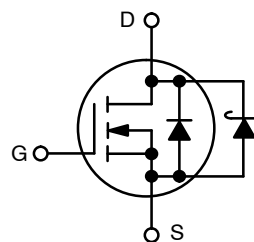


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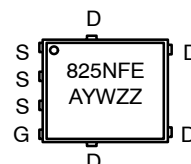
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	2.0 m Ω @ 10 V	171 A
	3.0 m Ω @ 4.5 V	140 A

N-CHANNEL MOSFET



SO-8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4825NFET1G	SO-8FL (Pb-Free)	1500 / Tape & Reel
NTMFS4825NFET3G	SO-8FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.3	°C/W
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	45.7	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	132.1	
Junction-to-Ambient – $t \leq 10$ sec	$R_{\theta JA}$	17.2	
Junction-to-Top	$R_{\theta JT}$	7.0	

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1.0\text{ mA}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			28.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$		60	500	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 1.0\text{ mA}$	1.5	2.0	2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 22\text{ A}$	1.3	2.0	mΩ
			$I_D = 20\text{ A}$	1.3		
		$V_{GS} = 4.5\text{ V}$	$I_D = 20\text{ A}$	2.0	3.0	
			$I_D = 18\text{ A}$	2.0		
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		90		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		5660		pF
Output Capacitance	C_{OSS}			1150		
Reverse Transfer Capacitance	C_{RSS}			495		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 23\text{ A}$		40.2		nC
Threshold Gate Charge	$Q_{G(TH)}$			6.4		
Gate-to-Source Charge	Q_{GS}			15.3		
Gate-to-Drain Charge	Q_{GD}			13.4		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 23\text{ A}$		83.6		nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\text{ }\Omega$		26		ns
Rise Time	t_r			24		
Turn-Off Delay Time	$t_{d(OFF)}$			36		
Fall Time	t_f			13		

3. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
4. Switching characteristics are independent of operating junction temperatures.

NTMFS4825NFE

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		15.7		ns
Rise Time	t_r			21.2		
Turn-Off Delay Time	$t_{d(OFF)}$			44.6		
Fall Time	t_f			14.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 2.0\text{ A}$	$T_J = 25^\circ\text{C}$		0.35	0.70	V
			$T_J = 125^\circ\text{C}$		0.26		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 23\text{ A}$			39.1		ns
Charge Time	t_a				20.1		
Discharge Time	t_b				19		
Reverse Recovery Charge	Q_{RR}				34		nC

PACKAGE PARASITIC VALUES

Source Inductance	L_S	$T_A = 25^\circ\text{C}$		0.66		nH
Drain Inductance	L_D			0.20		
Gate Inductance	L_G			1.5		
Gate Resistance	R_G			0.7	2.0	Ω

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

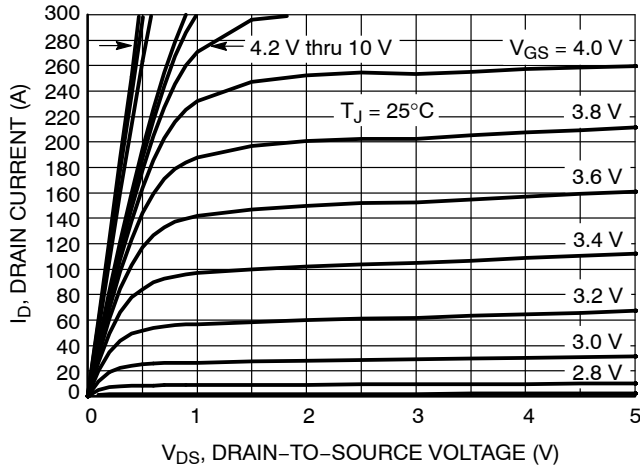


Figure 1. On-Region Characteristics

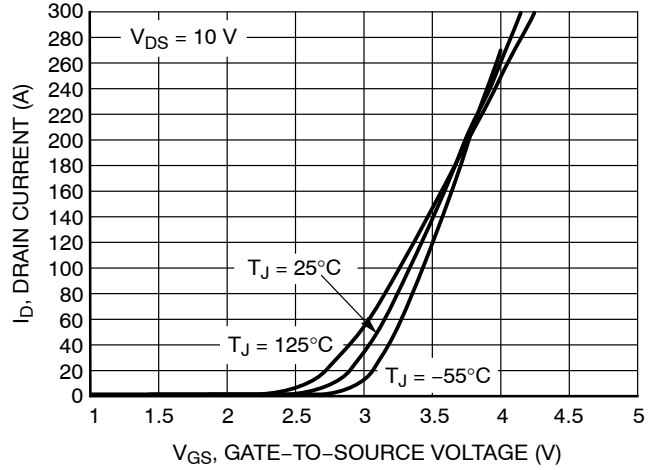


Figure 2. Transfer Characteristics

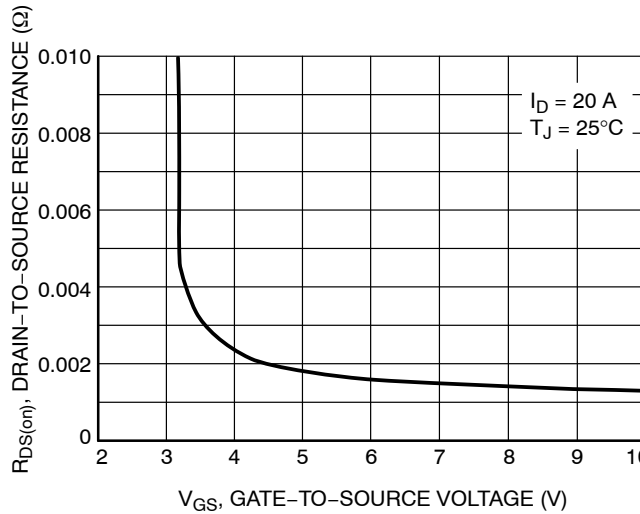


Figure 3. On-Resistance vs. Gate-to-Source Voltage

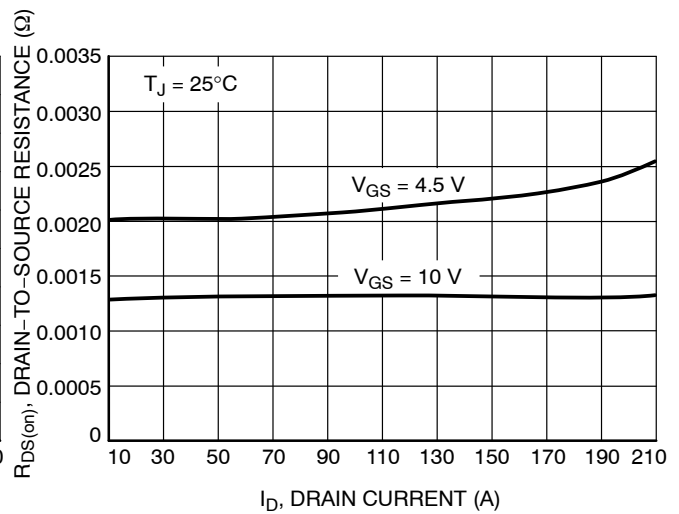


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

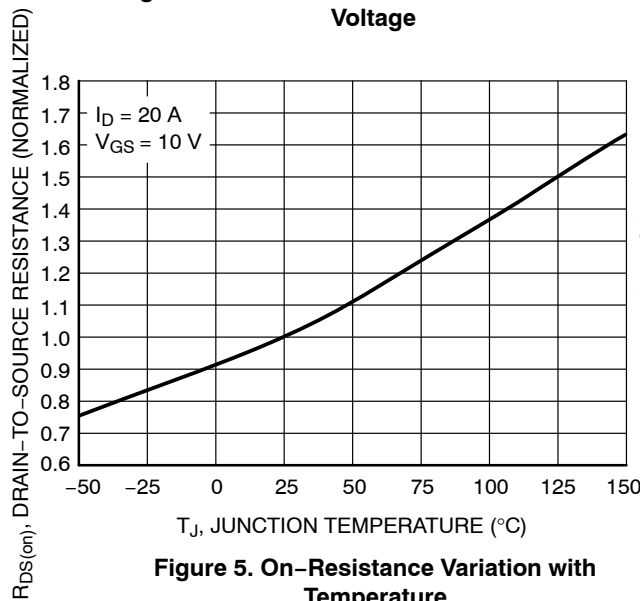


Figure 5. On-Resistance Variation with Temperature

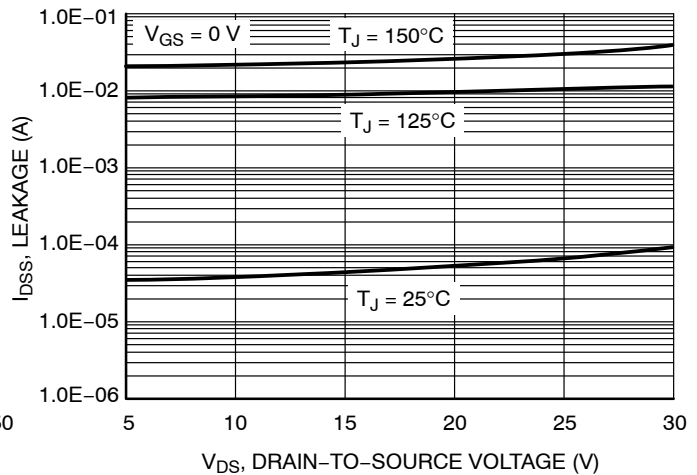


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

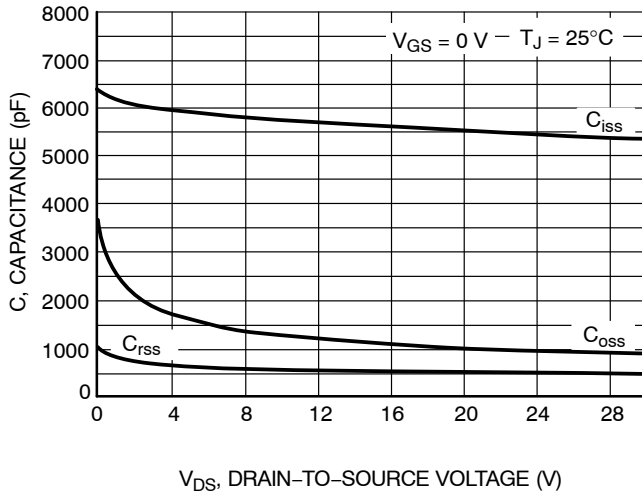


Figure 7. Capacitance Variation

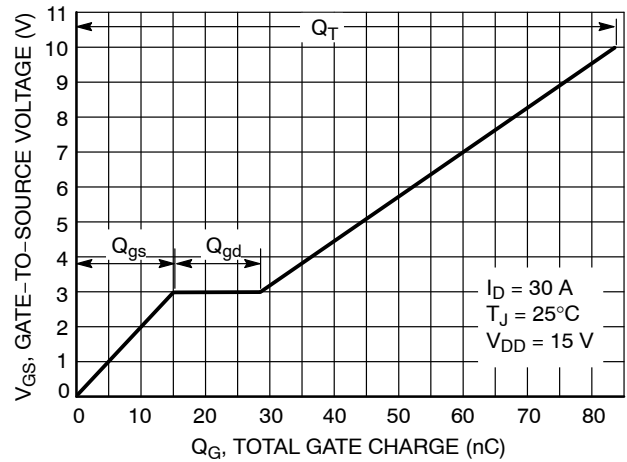


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

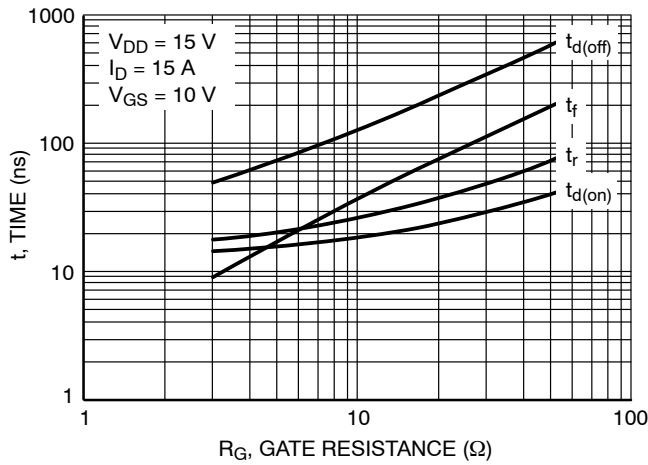


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

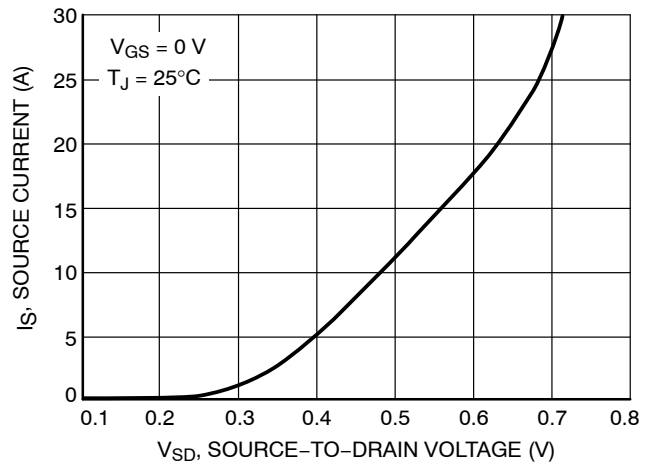


Figure 10. Diode Forward Voltage vs. Current

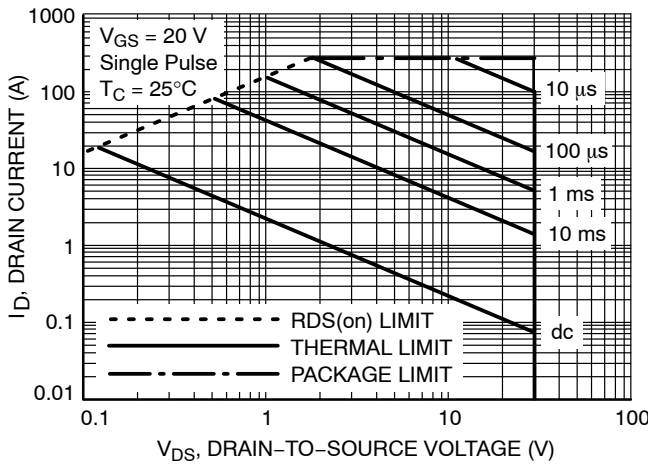


Figure 11. Maximum Rated Forward Biased Safe Operating Area

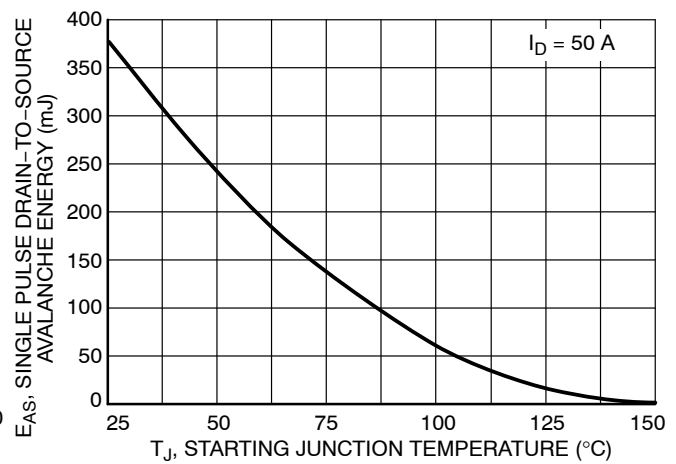


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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