

## P-channel Enhancement Mode Power MOSFET

### Features

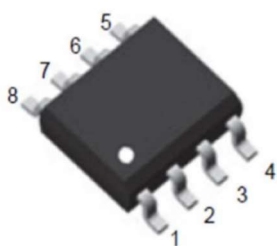
- $V_{DS} = -20V$ ,  $I_D = -13A$   
 $R_{DS(ON)} < 17\text{ m}\Omega$  @  $V_{GS} = -4.5V$   
 $R_{DS(ON)} < 20\text{ m}\Omega$  @  $V_{GS} = -2.5V$

### General Features

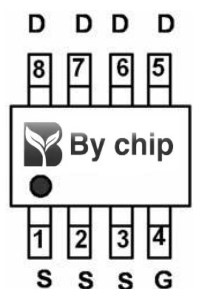
- Advanced Trench Technology
- Provide Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free and Green Available

100% UIS TESTED!

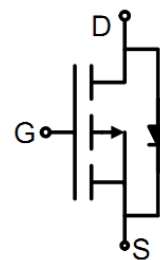
100%  $\Delta V_{ds}$  TESTED!



SOP-8



pin assignment



Schematic diagram

### ■ Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Parameter                                                          |                                         | Symbol          | Maximum    | Unit                      |
|--------------------------------------------------------------------|-----------------------------------------|-----------------|------------|---------------------------|
| Drain-source Voltage                                               |                                         | $V_{DS}$        | -20        | V                         |
| Gate-source Voltage                                                |                                         | $V_{GS}$        | $\pm 10$   | V                         |
| Drain Current                                                      | $T_A = 25^\circ\text{C}$ @ Steady State | $I_D$           | -13        | A                         |
|                                                                    | $T_A = 70^\circ\text{C}$ @ Steady State |                 | -10.4      |                           |
| Pulsed Drain Current <sup>A</sup>                                  |                                         | $I_{DM}$        | -55        | A                         |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$                 |                                         | $P_D$           | 3.0        | W                         |
| Thermal Resistance Junction-to-Ambient @ Steady State <sup>B</sup> |                                         | $R_{\theta JA}$ | 42         | $^\circ\text{C}/\text{W}$ |
| Junction and Storage Temperature Range                             |                                         | $T_J, T_{STG}$  | -55 ~ +150 | $^\circ\text{C}$          |

# ■ Electrical Characteristics (T<sub>J</sub>=25℃ unless otherwise noted)

| Parameter                             | Symbol              | Conditions                                                                                  | Min  | Typ  | Max  | Units |
|---------------------------------------|---------------------|---------------------------------------------------------------------------------------------|------|------|------|-------|
| Static Parameter                      |                     |                                                                                             |      |      |      |       |
| Drain-Source Breakdown Voltage        | BV <sub>DSS</sub>   | V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA                                                | -20  |      |      | V     |
| Zero Gate Voltage Drain Current       | I <sub>DSS</sub>    | V <sub>DS</sub> =-20V,V <sub>GS</sub> =0V,T <sub>C</sub> =25℃                               |      |      | -1   | μA    |
| Gate-Body Leakage Current             | I <sub>GSS</sub>    | V <sub>GS</sub> = ±10V, V <sub>DS</sub> =0V                                                 |      |      | ±100 | nA    |
| Gate Threshold Voltage                | V <sub>GS(th)</sub> | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA                                  | -0.4 |      | -2.0 | V     |
| Static Drain-Source On-Resistance     | R <sub>DS(ON)</sub> | V <sub>GS</sub> = -4.5V, I <sub>D</sub> =-10A                                               |      |      | 17   | mΩ    |
|                                       |                     | V <sub>GS</sub> = -2.5V, I <sub>D</sub> =-6.5A                                              |      |      | 20   |       |
|                                       |                     | V <sub>GS</sub> = -1.8V, I <sub>D</sub> =-4.0A                                              |      |      | 26   |       |
| Diode Forward Voltage                 | V <sub>SD</sub>     | I <sub>S</sub> =-13A,V <sub>GS</sub> =0V                                                    |      |      | -1.2 | V     |
| Maximum Body-Diode Continuous Current | I <sub>S</sub>      |                                                                                             |      |      | -13  | A     |
| Dynamic Parameters                    |                     |                                                                                             |      |      |      |       |
| Input Capacitance                     | C <sub>iss</sub>    | V <sub>DS</sub> =-10V,V <sub>GS</sub> =0V,f=1MHZ                                            |      | 2992 |      | pF    |
| Output Capacitance                    | C <sub>oss</sub>    |                                                                                             |      | 330  |      |       |
| Reverse Transfer Capacitance          | C <sub>rss</sub>    |                                                                                             |      | 272  |      |       |
| Switching Parameters                  |                     |                                                                                             |      |      |      |       |
| Total Gate Charge                     | Q <sub>g</sub>      | V <sub>GS</sub> =-10V,V <sub>DS</sub> =-15V,I <sub>D</sub> =-9.1A                           |      | 72.8 |      | nC    |
| Gate Source Charge                    | Q <sub>gs</sub>     |                                                                                             |      | 6.6  |      |       |
| Gate Drain Charge                     | Q <sub>gd</sub>     |                                                                                             |      | 10.1 |      |       |
| Reverse Recovery Charge               | Q <sub>rr</sub>     | I <sub>F</sub> =-6A, di/dt=100A/us                                                          |      | 34   |      |       |
| Reverse Recovery Time                 | t <sub>rr</sub>     |                                                                                             |      | 67   |      |       |
| Turn-on Delay Time                    | t <sub>D(on)</sub>  | V <sub>GS</sub> =-10V,V <sub>DS</sub> =-15V, I <sub>D</sub> =-6A,<br>R <sub>GEN</sub> =2.5Ω |      | 7    |      | ns    |
| Turn-on Rise Time                     | t <sub>r</sub>      |                                                                                             |      | 33   |      |       |
| Turn-off Delay Time                   | t <sub>D(off)</sub> |                                                                                             |      | 130  |      |       |
| Turn-off Fall Time                    | t <sub>f</sub>      |                                                                                             |      | 132  |      |       |

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. R<sub>θJA</sub> is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJL</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

## ■ Typical Performance Characteristics

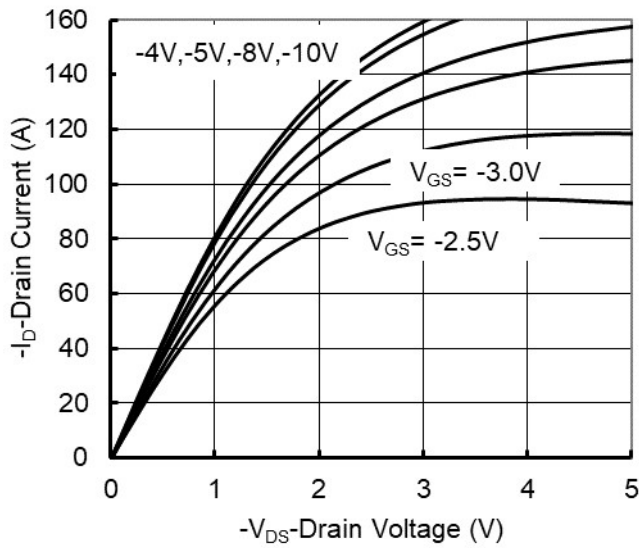


Figure 1. Output Characteristics

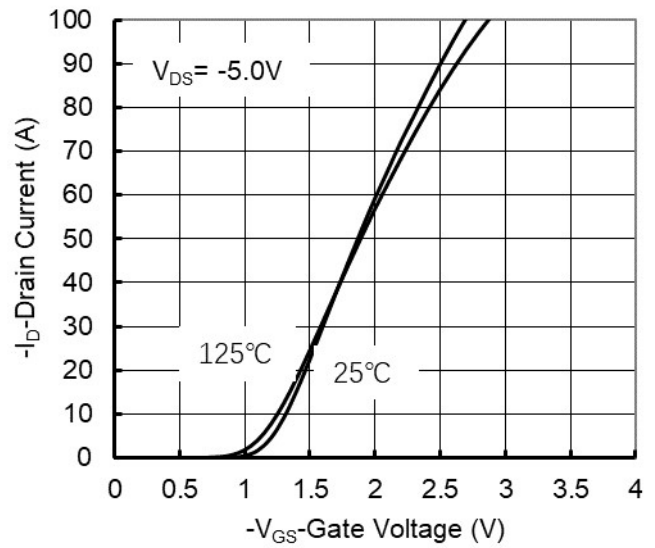


Figure 2. Transfer Characteristics

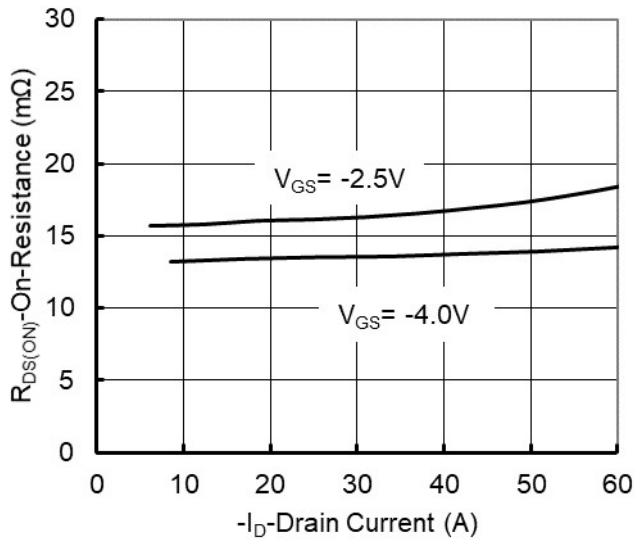


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

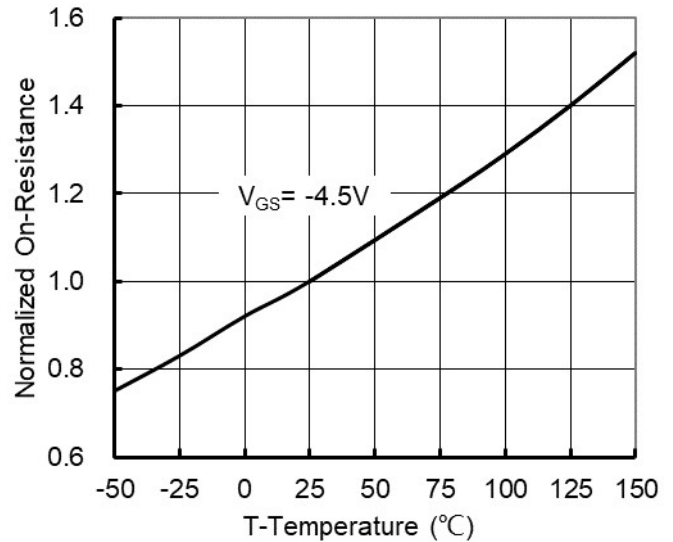


Figure 4. On-Resistance vs. Junction Temperature

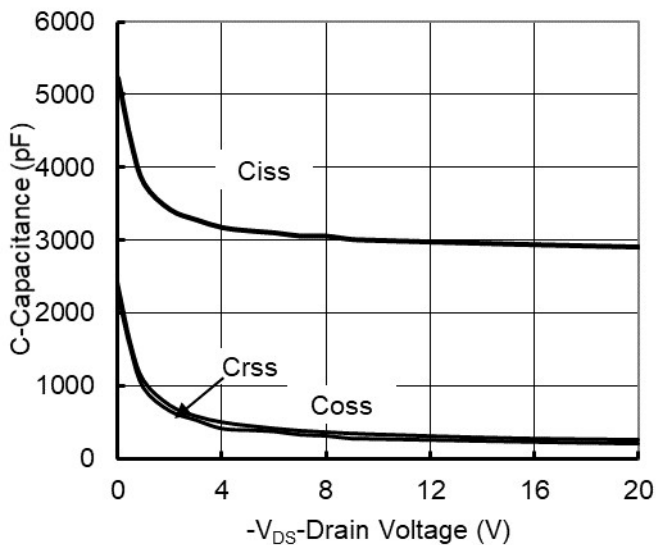


Figure 5. Capacitance Characteristics

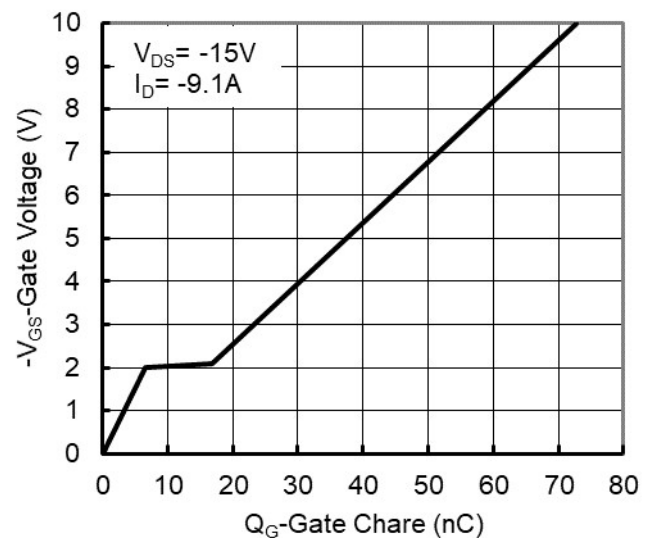


Figure 6. Gate Charge

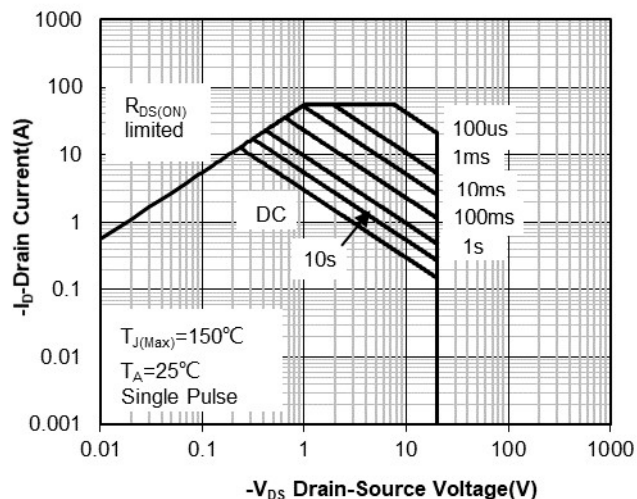


Figure 7. Safe Operation Area

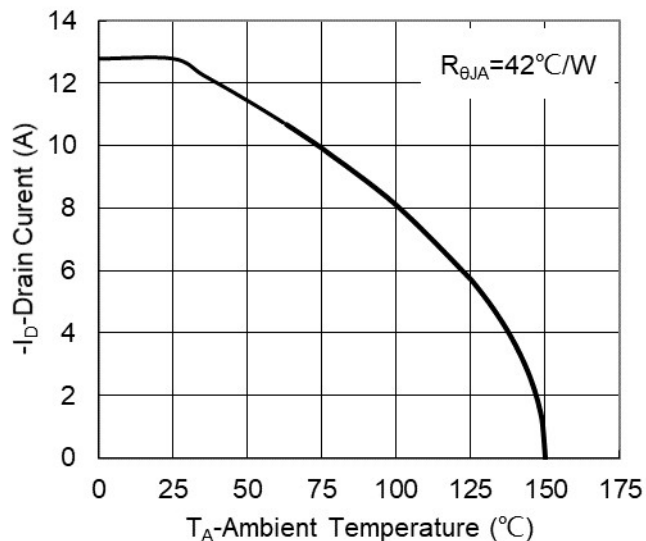


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

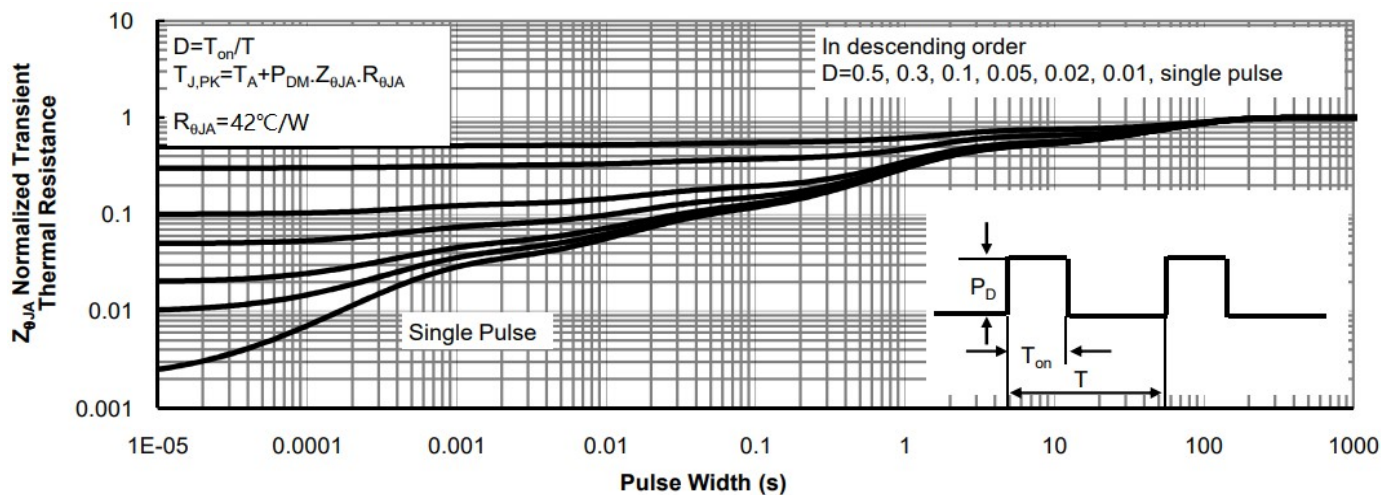
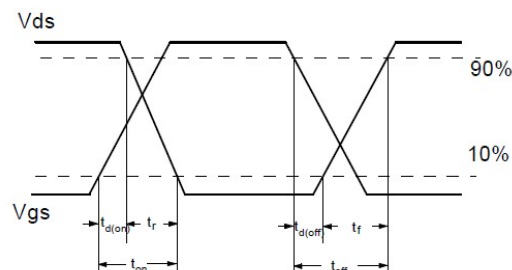
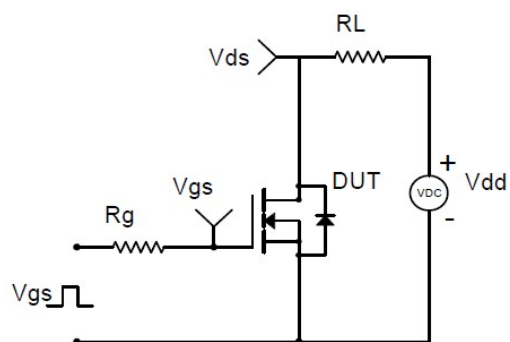
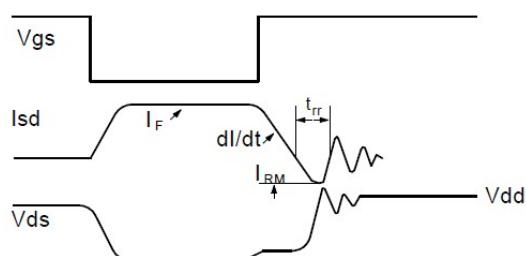
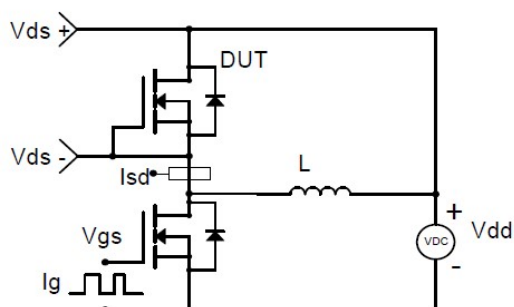


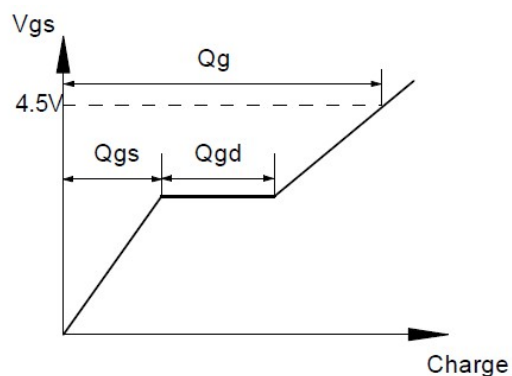
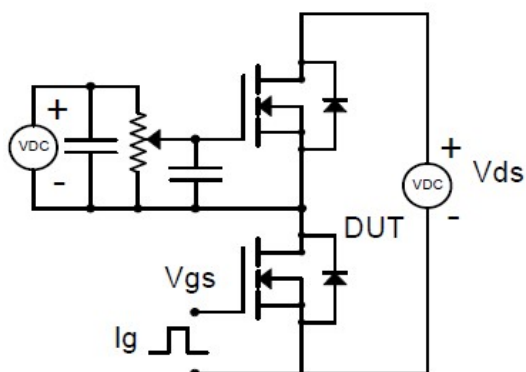
Figure 9. Normalized Maximum Transient Thermal Impedance



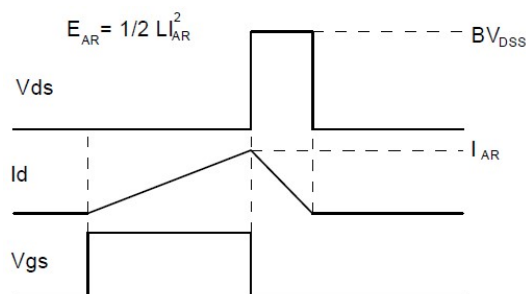
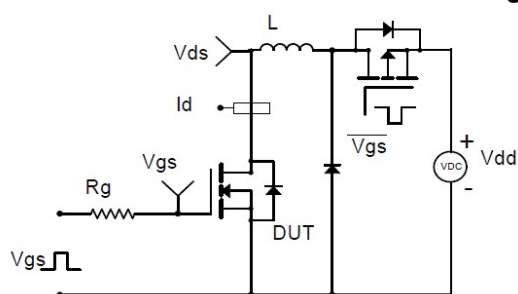
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**