

N-Channel and P-Channel Enhancement Mode Power MOSFET

Features

- N-Channel: 30V, 10A

$$R_{DS(ON)} < 15 \text{ m}\Omega @ V_{GS} = 10\text{V}$$

$$R_{DS(ON)} < 23 \text{ m}\Omega @ V_{GS} = 4.5\text{V}$$

- P-Channel: -30V, -12A

$$R_{DS(ON)} < 34 \text{ m}\Omega @ V_{GS} = -10\text{V}$$

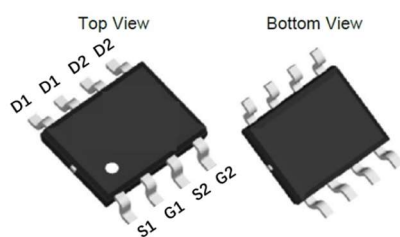
$$R_{DS(ON)} < 49 \text{ m}\Omega @ V_{GS} = -4.5\text{V}$$

General Features

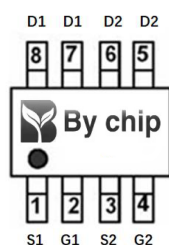
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

100% UIS TESTED!

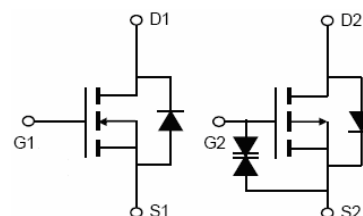
100% ΔV_{ds} TESTED!



SOP-8 Dual



Pin Assignment



Schematic diagram

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	NMOS	PMOS	Unit
Drain-source Voltage		V_{DS}	30	-30	V
Gate-source Voltage		V_{GS}	± 20	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	7	-5	A
	$T_A=100^\circ\text{C}$		4.4	-3	
Pulsed Drain Current ^A		I_{DM}	60	-40	A
Total Power Dissipation ^B	$T_A=25^\circ\text{C}$	P_D	2	2	W
	$T_A=100^\circ\text{C}$		0.8	0.8	
Junction and Storage Temperature Range		T_J, T_{STG}	$-55 \sim +150$	$-55 \sim +150$	$^\circ\text{C}$

■ Thermal resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient ^C	Steady-State	$R_{\theta JA}$	50	60	50	60	$^\circ\text{C/W}$

■ NMOS Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
		V _{DS} =30V, V _{GS} =0V, T _J =150℃	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0		2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =7A	-		15	mΩ
		V _{GS} =4.5V, I _D =5A	-		23	
Diode Forward Voltage	V _{SD}	I _S =7A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	2	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	7	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHz	-	380	-	pF
Output Capacitance	C _{oss}		-	75	-	
Reverse Transfer Capacitance	C _{rss}		-	60	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =7A	-	12.5	-	nC
Gate-Source Charge	Q _{gs}		-	2.5	-	
Gate-Drain Charge	Q _{gd}		-	2.5	-	
Reverse Recovery Charge	Q _{rr}	I _F =7A, di/dt=100A/us	-	1.5	-	nC
Reverse Recovery Time	t _{rr}		-	16	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =15V, I _D =7A R _{GEN} =3Ω	-	5	-	ns
Turn-on Rise Time	t _r		-	30	-	
Turn-off Delay Time	t _{D(off)}		-	15	-	
Turn-off fall Time	t _f		-	20	-	

■ PMOS Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V	-	-	-1	μA
		V _{DS} =-30V, V _{GS} =0V, T _j =150℃	-	-	-100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-1.0		-2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-5A	-		34	mΩ
		V _{GS} =-4.5V, I _D =-3.5A	-		49	
Diode Forward Voltage	V _{SD}	I _S =-5A, V _{GS} =0V	-	-	-1.2	V
Gate resistance	R _G	f=1MHz	-	15	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	-5	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V, f=1MHz	-	490	-	pF
Output Capacitance	C _{oss}		-	75	-	
Reverse Transfer Capacitance	C _{rss}		-	60	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-15V, I _D =-5A	-	9	-	nC
Gate-Source Charge	Q _{gs}		-	1.5	-	
Gate-Drain Charge	Q _{gd}		-	2.3	-	
Reverse Recovery Charge	Q _{rr}	I _F =-5A, di/dt=100A/us	-	12	-	nC
Reverse Recovery Time	t _{rr}		-	32	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-15V, I _D =-5A R _{GEN} =2.5Ω	-	9	-	ns
Turn-on Rise Time	t _r		-	3	-	
Turn-off Delay Time	t _{D(off)}		-	29	-	
Turn-off fall Time	t _f		-	15	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. P_d is based on max. junction temperature, using junction-case thermal resistance.

C. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with T_A=25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

■ NMOS Typical Electrical and Thermal Characteristics Diagrams

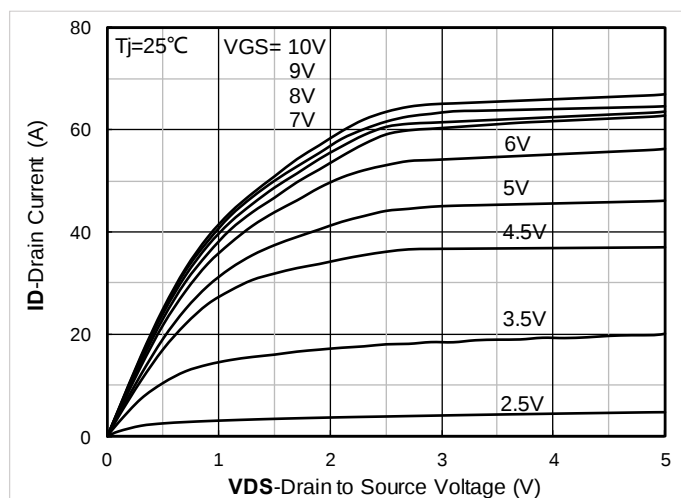


Figure 1. Output Characteristics

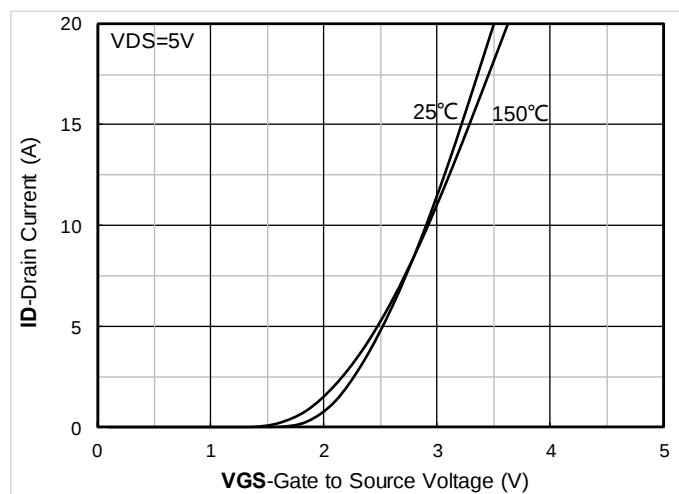


Figure 2. Transfer Characteristics

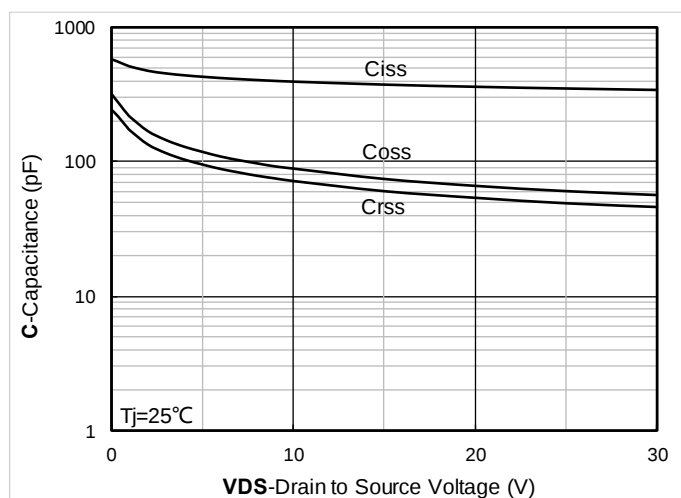


Figure 3. Capacitance Characteristics

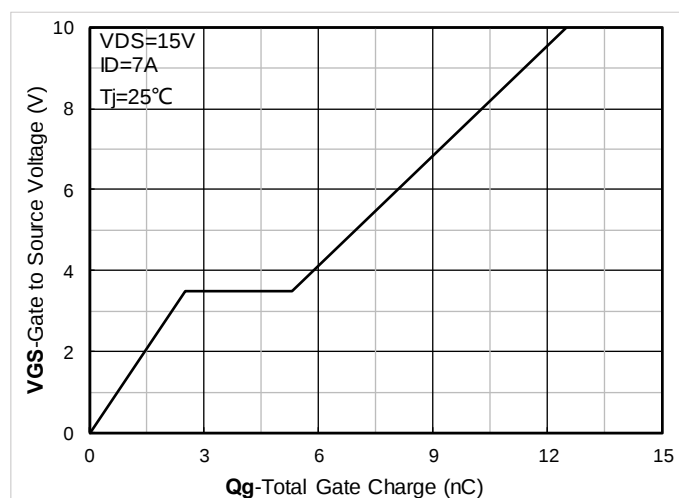


Figure 4. Gate Charge

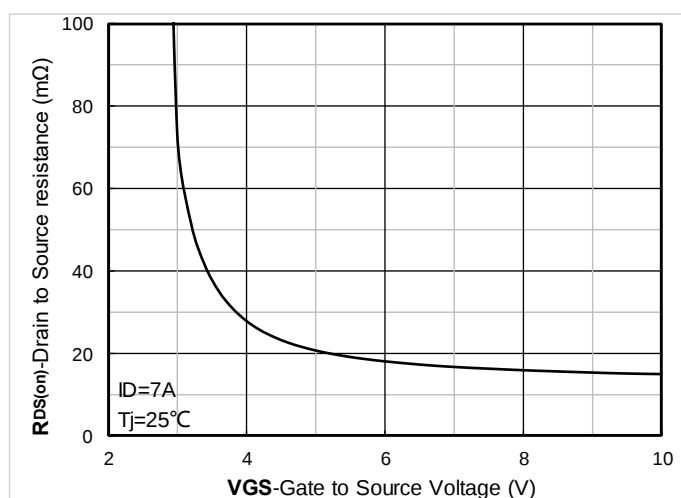


Figure 5. On-Resistance vs Gate to Source Voltage

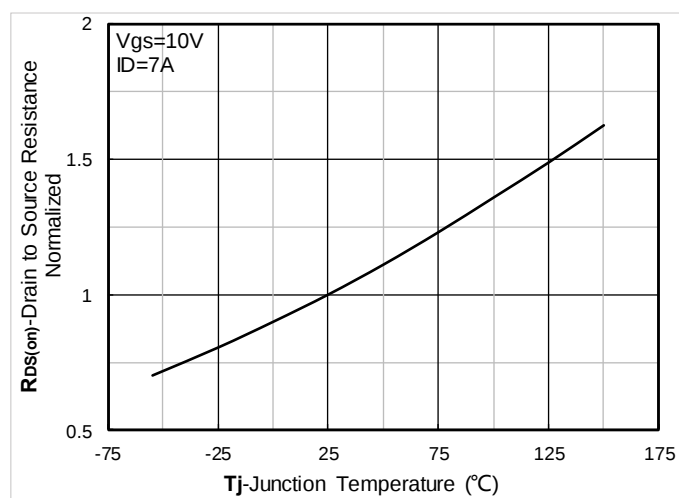


Figure 6. Normalized On- Resistance

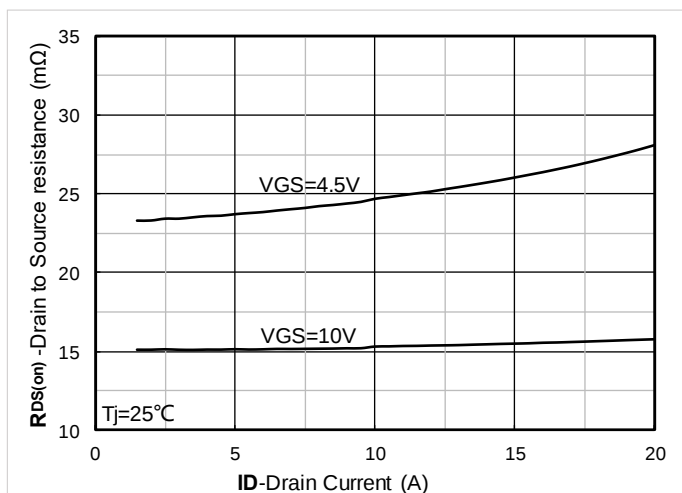


Figure 7. $R_{DS(on)}$ VS Drain Current

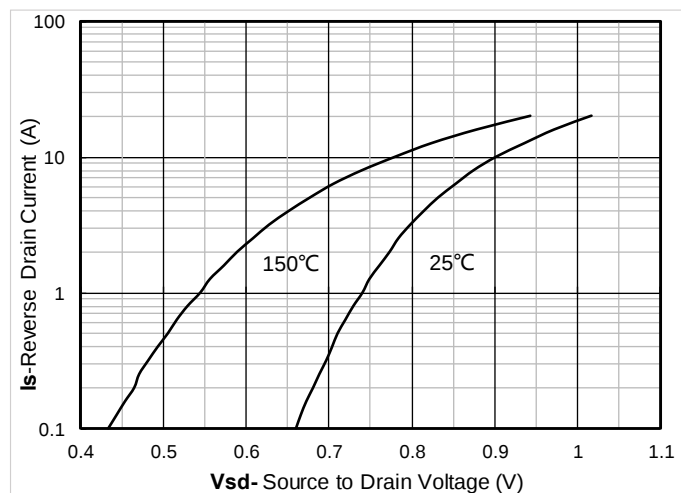


Figure 8. Forward characteristics of reverse diode

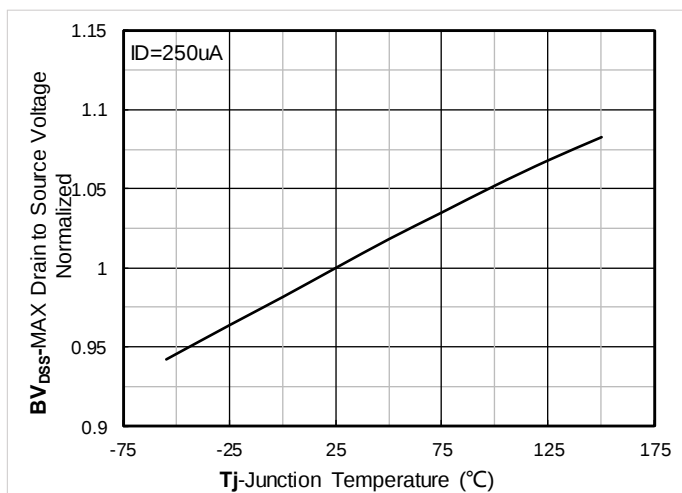


Figure 9. Normalized breakdown voltage

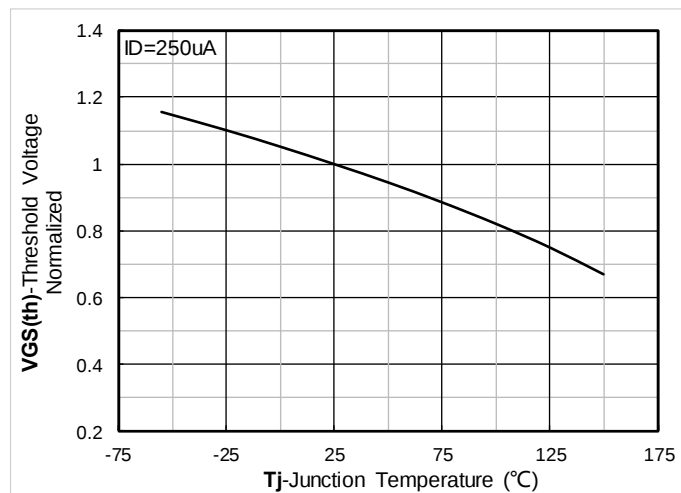


Figure 10. Normalized Threshold voltage

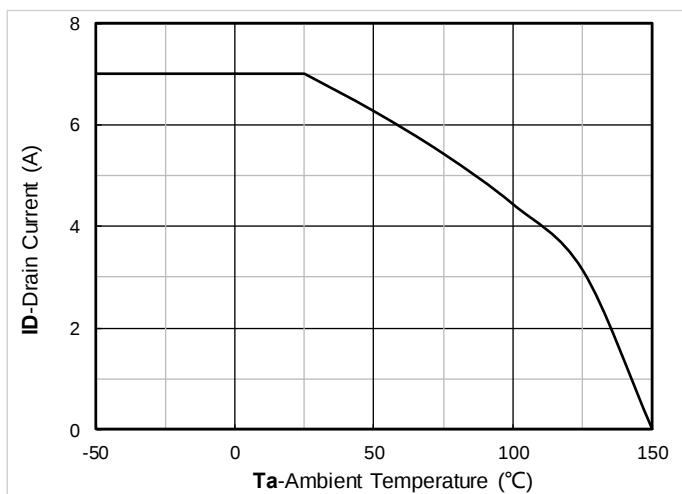


Figure 11. Current dissipation

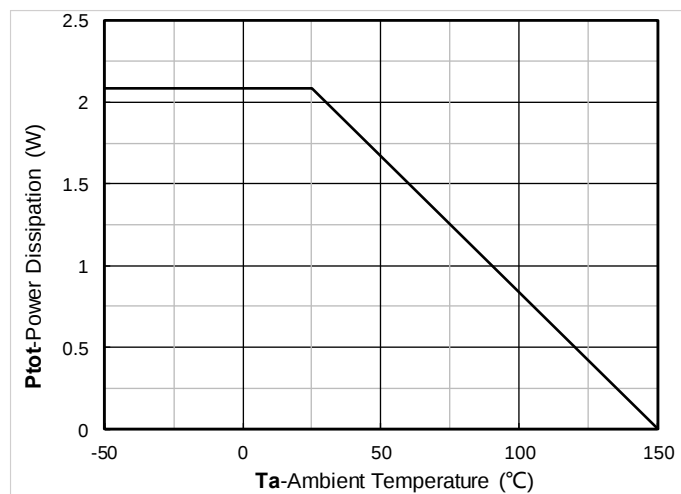


Figure 12. Power dissipation

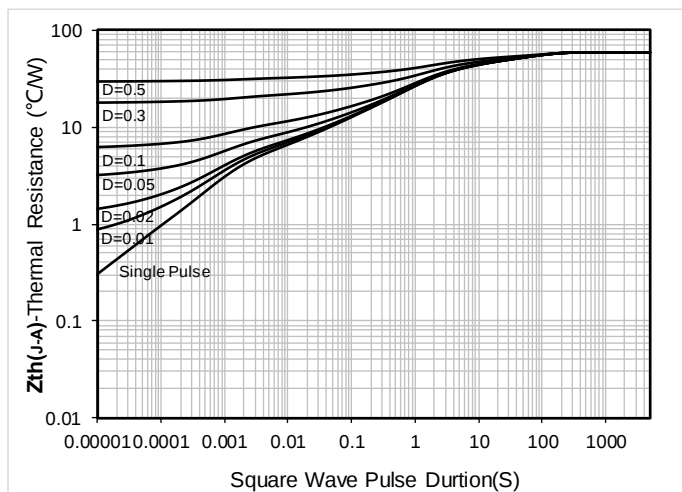


Figure 13. Maximum Transient Thermal Impedance

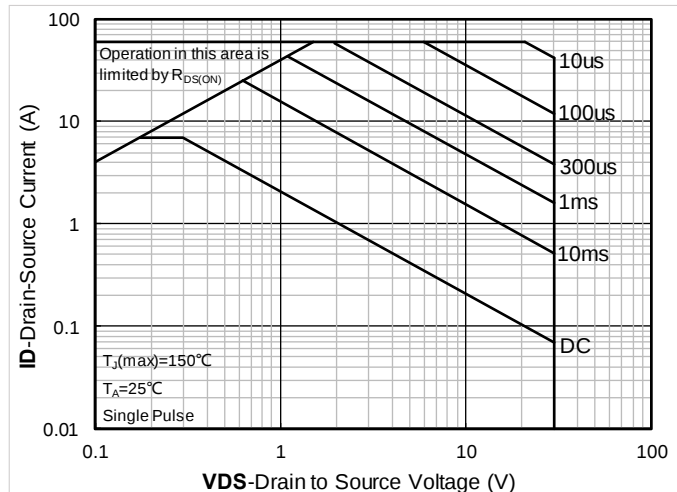


Figure 14. Safe Operation Area

PMOS Typical Electrical and Thermal Characteristics Diagrams

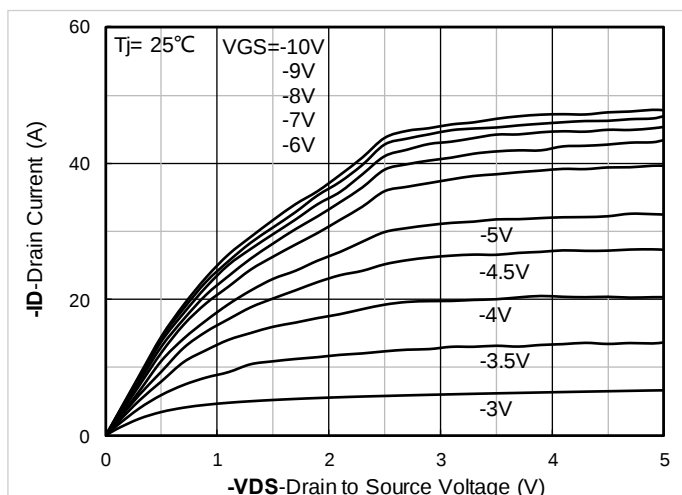


Figure 1. Output Characteristics

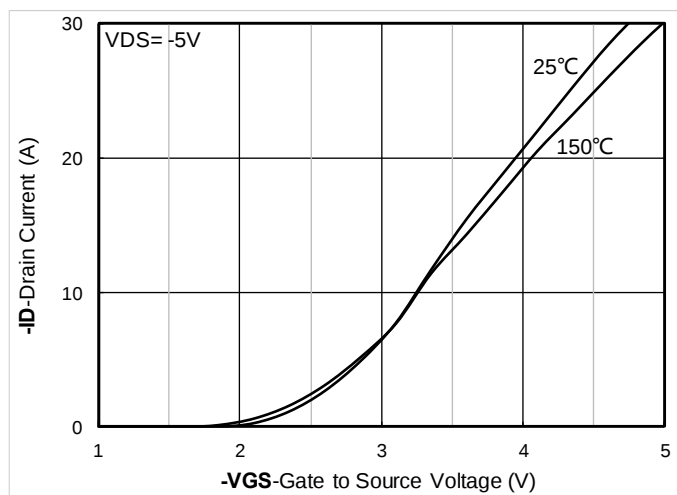


Figure 2. Transfer Characteristics

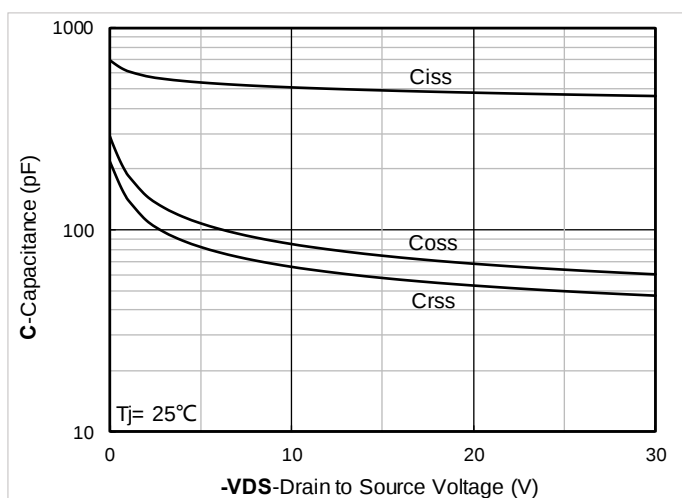


Figure 3. Capacitance Characteristics

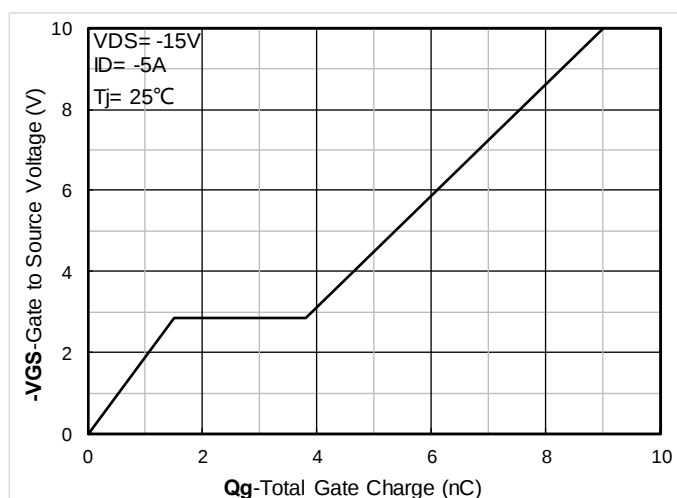


Figure 4. Gate Charge

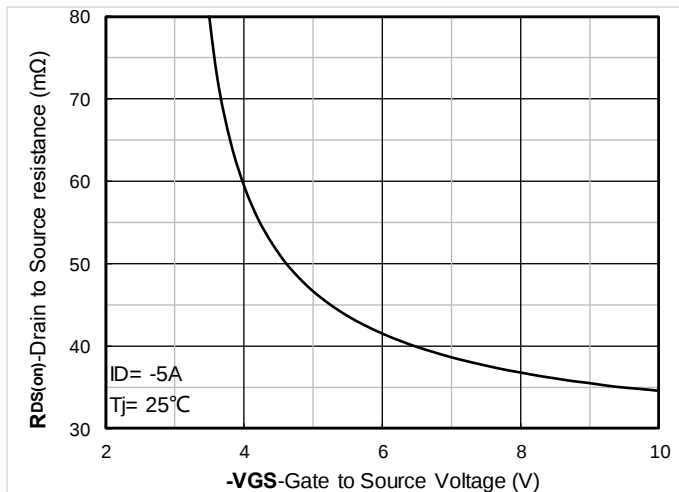


Figure 5. On-Resistance vs Gate to Source Voltage

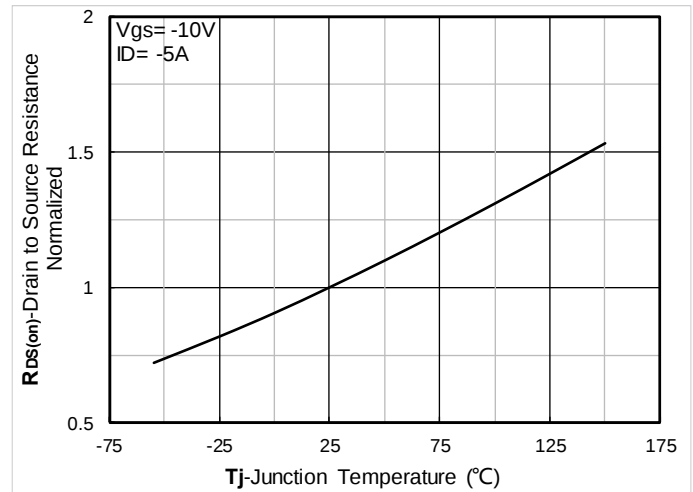


Figure 6. Normalized On-Resistance

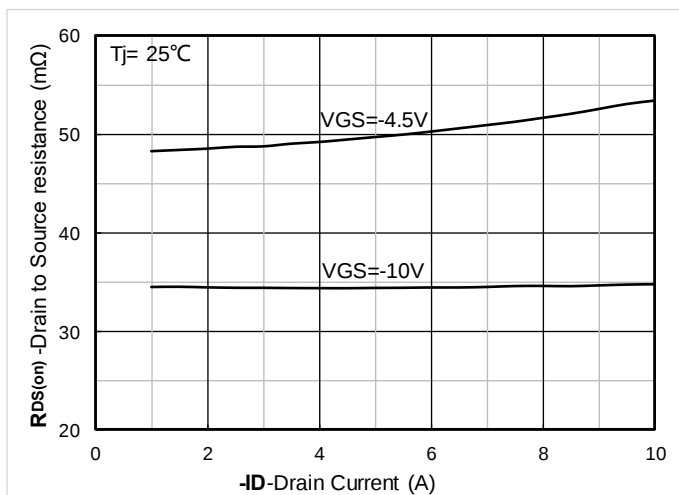


Figure 7. $R_{DS(on)}$ VS Drain Current

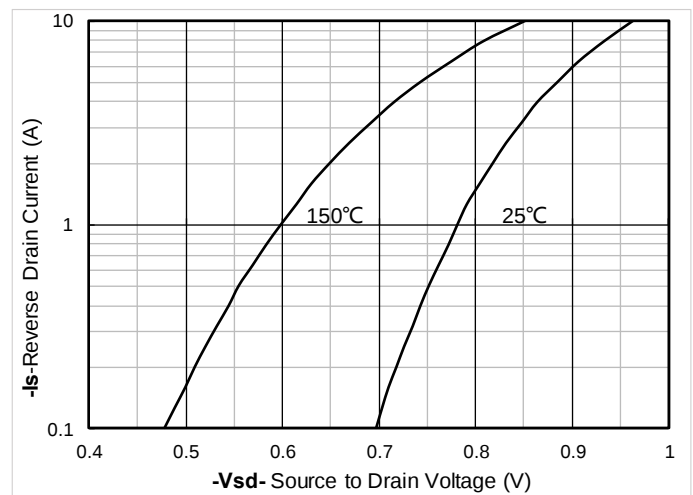


Figure 8. Forward characteristics of reverse diode

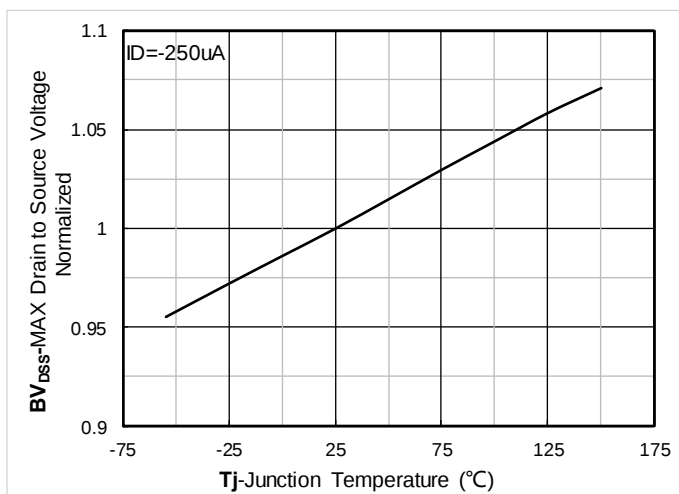


Figure 9. Normalized breakdown voltage

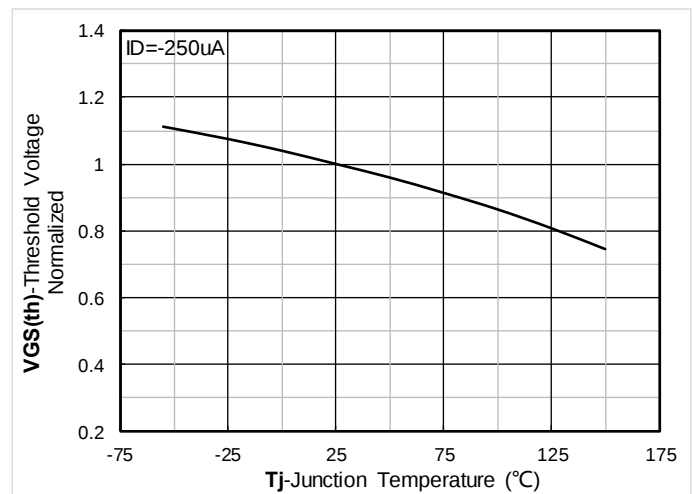


Figure 10. Normalized Threshold voltage

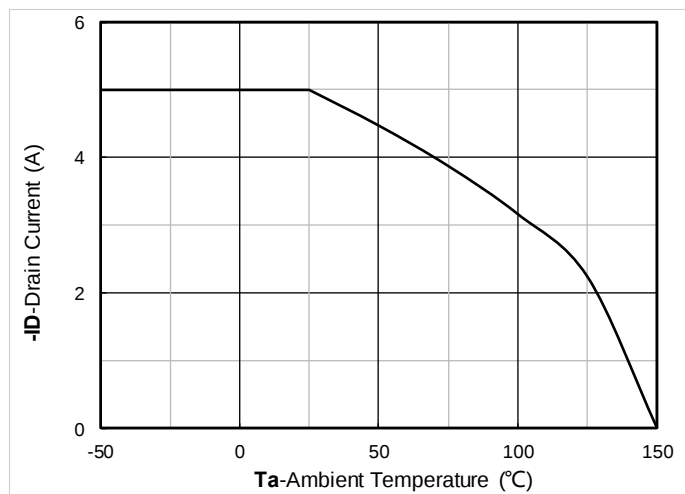


Figure 11. Current dissipation

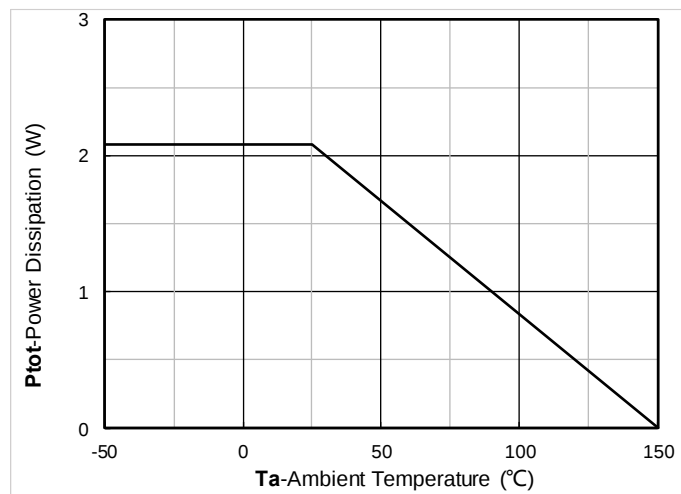


Figure 12. Power dissipation

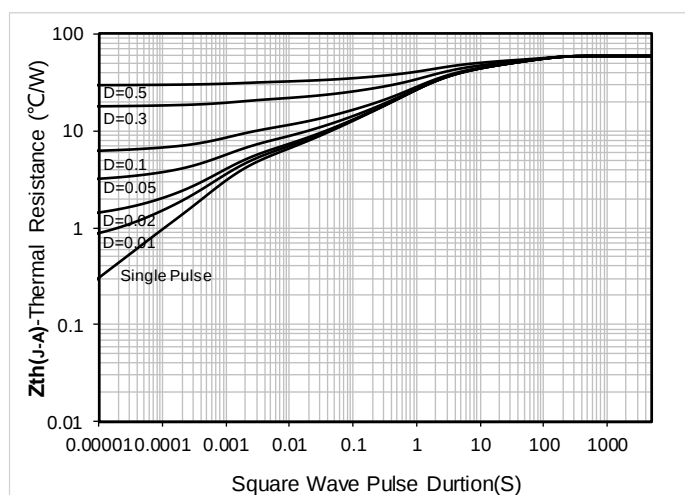


Figure 13. Maximum Transient Thermal Impedance

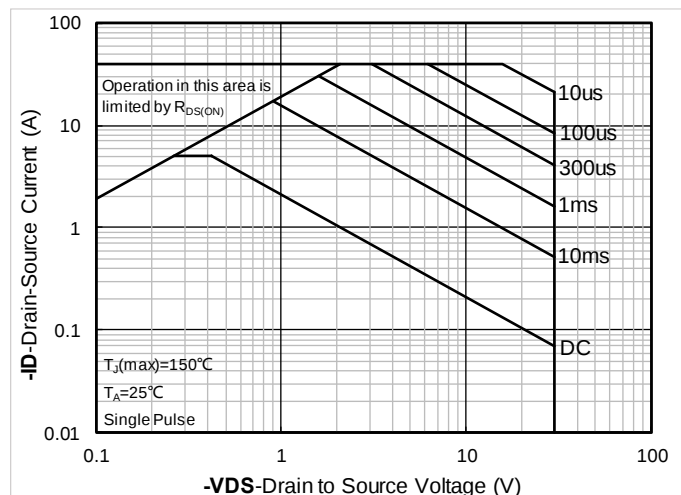


Figure 14. Safe Operation Area