STRUCTURE Silicon monolithic integrated circuit

PRODUCT NAME Data formatter LSI for IR remote control system for cellular phone

MODEL NAME BU7875GLS

EXTERNAL VIEW Figure 1 Package outline (VFLGA12-3)

BLOCK DIAGRAM Figure 2 Block diagram

MEASUREMENT CIRCUIT Figure 3 Test circuit

EXAMPLE OF APPLICATON Figure 4 Example of application circuit

FEATURES As to IR Remote Control
- Programmable Carrier Frequency
- Programmable Length of Header
- Programmable Length of Data hi
- Programmable Length of Data lo
- Programmable Length of End part
- Maximum Output Data Bit : 128bit
- Programmable Length of Output Data Bit
- Programmable Frame
- Continuous Data Transmission
- Interrupt Function
- I^2C-Bus-Interface (Fast-Mode)

◎This chip is not designed to protect itself against radioactive rays.

Application example
The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.
When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.
Note that ROHM cannot provide adequate confirmation of patents.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

ROHM assumes no responsibility for use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

● ABSOLUTE MAXIMUM RATINGS

Unless otherwise noted, Ta = 25℃

Parameter	Symbol	Min.	Max.	Unit
Supply voltage	VDD	−0.3	4.5	V
Input voltage	VIN	GND−0.3	VDD+0.3	V
Input current	IIN	-	±10	mA
Power dissipation	Pd	200※		mW
Operating temperature range	T_{OPR}	−30	+80	℃
Storage temperature range	T_{STG}	−55	+125	℃

※This is the power dissipation per IC unit. Reduce to 2.0 mW/℃ when Ta = 25℃ or above.

● OPERATION RANGE

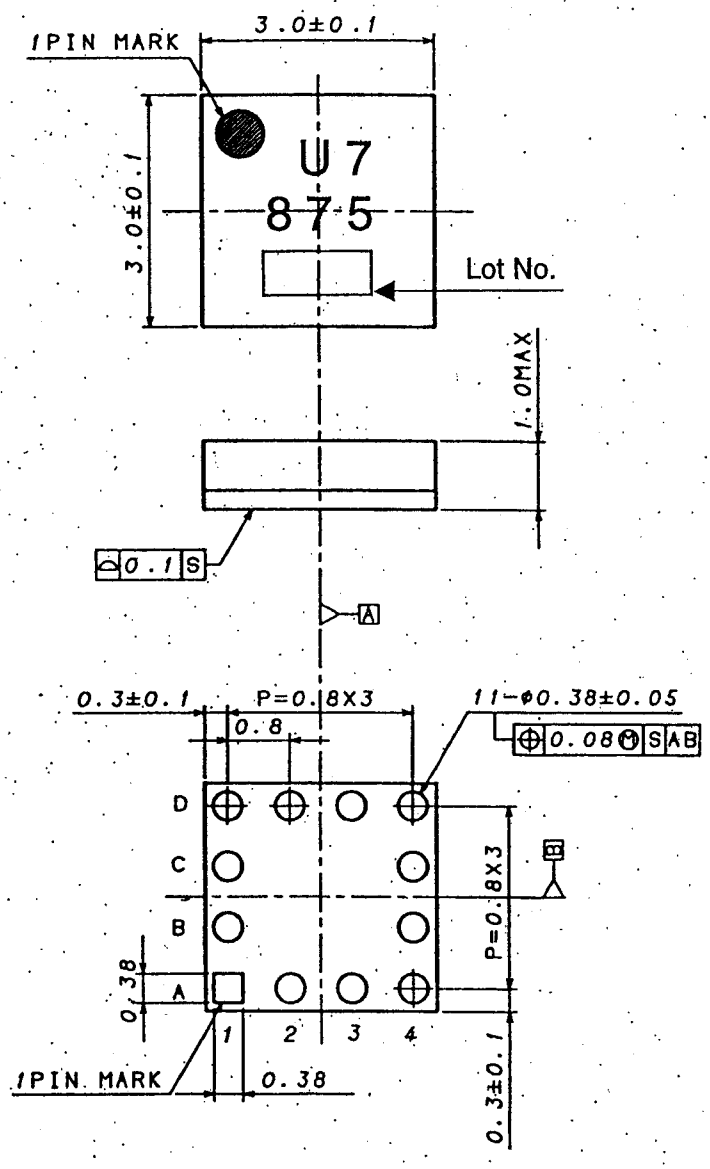
Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD	2.7	3.0	3.3	V
Reference clock frequency (VDD=3.0V)	fclki	-	16.128	20.0	MHz

● ELECTRICAL CHARACTERISTICS

Unless otherwise noted, Ta = 25℃, VDD=3.0V, GND=0V, CLKI=16.128MHz

Parameter	Symbol	Rating			Unit	Conditions
		MIN.	TYP.	MAX.		
Circuit Current 1	IDD1	-	0.1	3	μA	Pwr=0
Circuit Current 2	IDD2	-	1.0	2.0	mA	transmitting default format
Digital High-level input voltage	VIH	0.8× VDD	-	-	V	
Digital Low-level input voltage	VIL	-	-	0.2× VDD	V	
Digital High-level input current	IIH	-	-	10	μA	
Digital Low-level input current	IIL	-	-	10	μA	
Digital High-level output voltage 1	VOH1	VDD− 0.6	-	-	V	NIRQ pin IOH=−1mA
Digital Low-level output voltage 1	VOL1	-	-	0.6	V	NIRQ pin IOL=1mA
Digital High-level output voltage 2	VOH2	VDD− 0.6	-	-	V	DOUT pin IOH=−10mA
Digital Low-level output voltage 2	VOL2	-	-	0.6	V	DOUT pin IOL=10mA
Digital Low-level output voltage 3	VOL3	-	-	0.4	V	SDA pin IOL=3mA
CLKI input level	Vclki	0.5	-	VDD	V_{P-P}	
SCL clock frequency	f_{SCL}	-	-	400	kHz	
Bus free time	t_{BUF}	1.3	-	-	μs	
START condition setup time	$t_{SU;STA}$	0.6	-	-	μs	
START condition hold time	$t_{HD;STA}$	0.6	-	-	μs	
SCL LOW time	t_{LOW}	1.3	-	-	μs	
SCL HIGH time	t_{HIGH}	0.6	-	-	μs	
Data setup time	$t_{SU;DAT}$	100	-	-	ns	
Data hold time	tHD;DAT	0	-	-	ns	
STOP condition setup time	tSU;STO	0.6	-	-	μs	

● PACKAGE OUTLINE



(UNIT:mm)

Fig. 1 Package outline

● BLOCK DIAGRAM

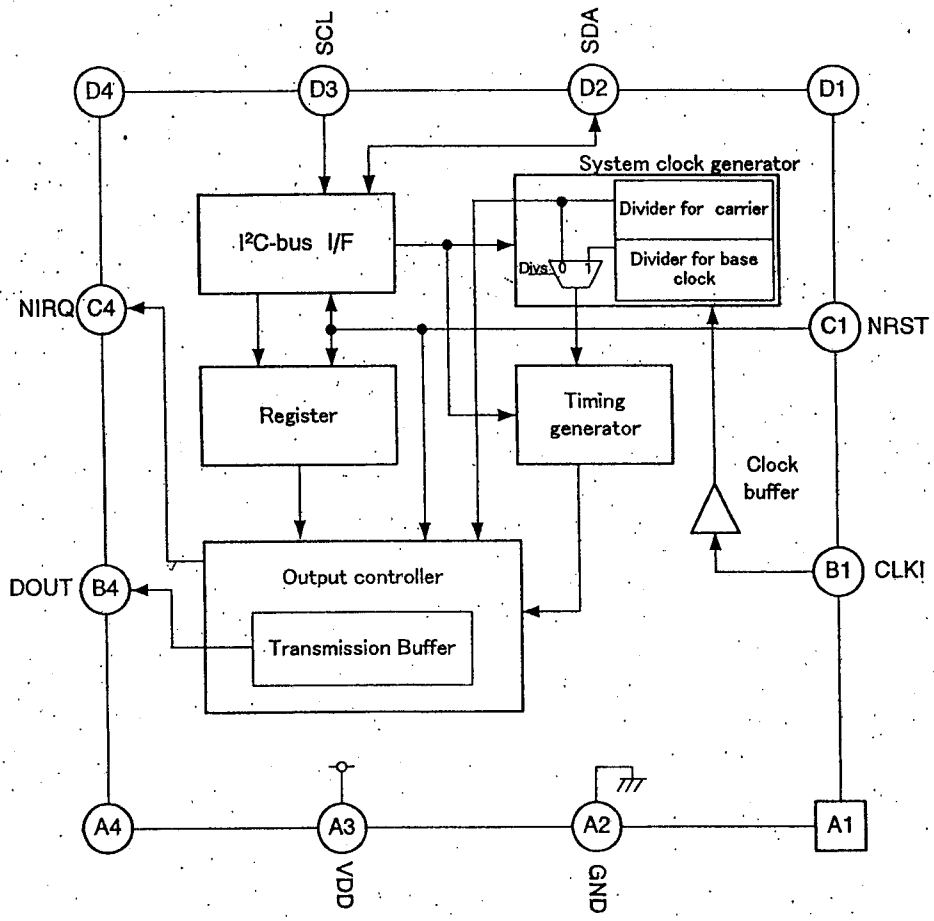


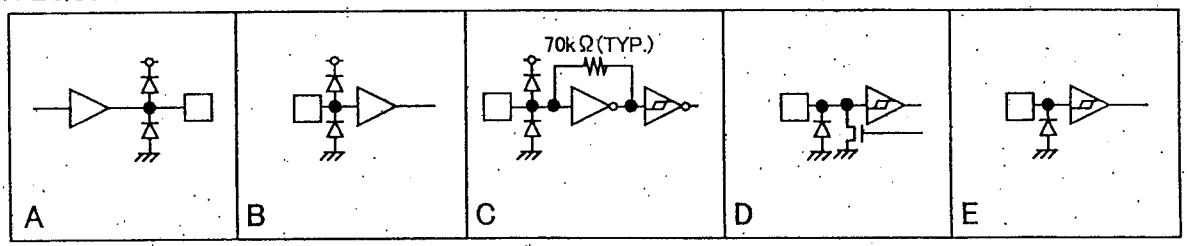
Fig. 2 Block diagram

● PIN DESCRIPTION

No	Pin name	I/O	Description	Pin equivalent circuit diagram
A2	GND	-	Ground	-
B1	CLKI	I	Reference clock input	C
C1	NRST	I	Reset pin (LOW : reset)	B
D2	SDA	I/O	Serial data input/output for I^2C-bus	D
D3	SCL	I	Serial clock input for I^2C-bus	E
C4	NIRQ	O	Interrupt output (LOW: Occurrence of interrupt)	A
B4	DOUT	O	Data output	A
A3	VDD	-	Supply voltage	-
A1	-	-	Pin for mount reinforcement※	-
A4	-	-	Pin for mount reinforcement※	-
D1	-	-	Pin for mount reinforcement※	-
D4	-	-	Pin for mount reinforcement※	-

※This pin doesn't connect to interval with electrical.

● PIN EQUIVALENT CIRCUIT DIAGRAM



● TEST CIRCUIT

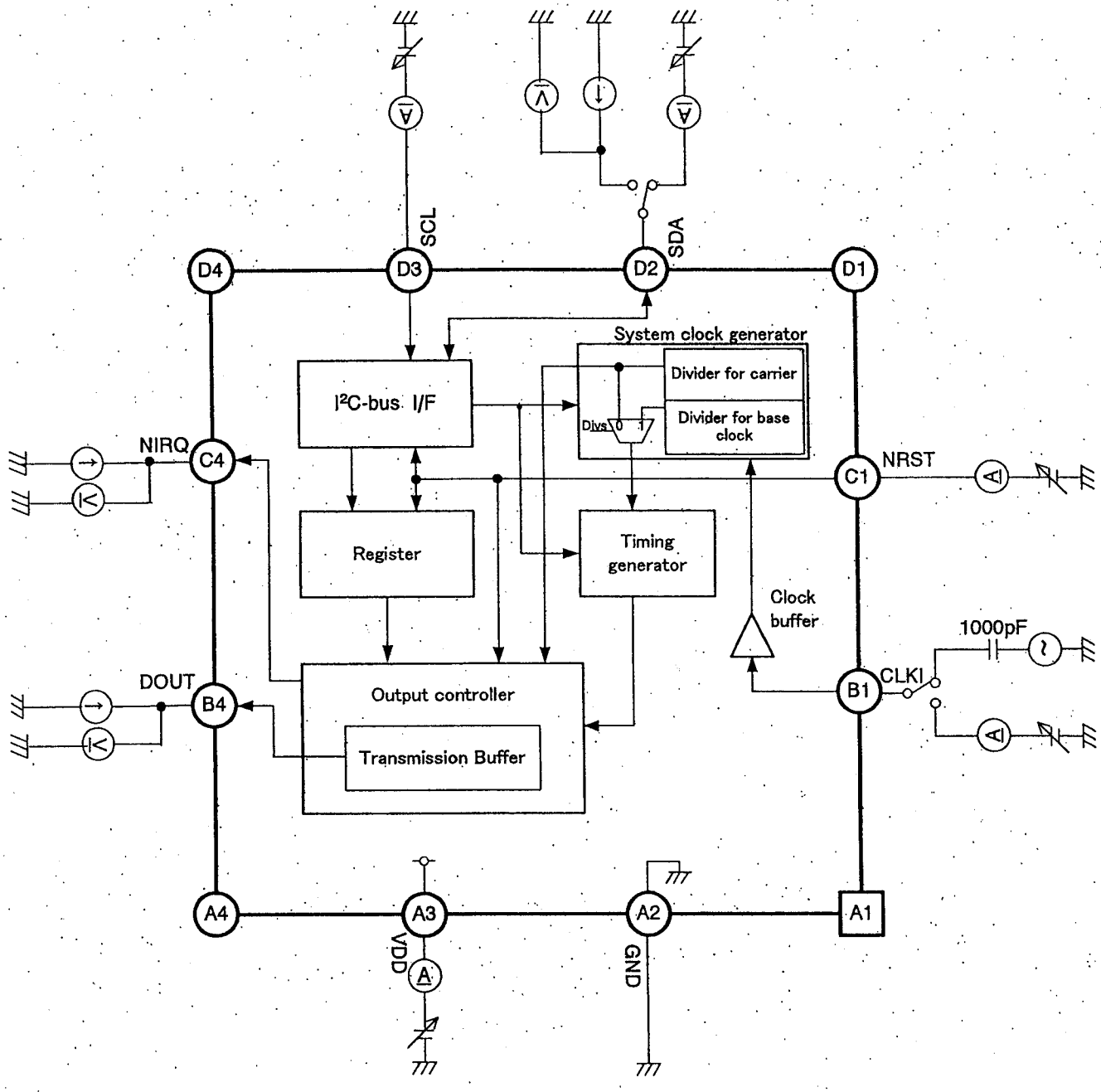


Fig. 3 Test circuit

● I²C-BUS INTERFACE

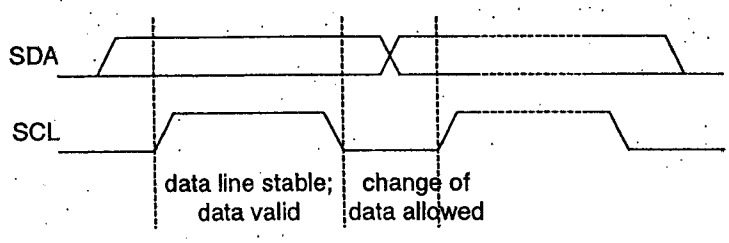
BU7875GLS is controlled by I²C slave interface. The address (slave address) is "1110111". Data on the I²C-bus can be transferred at rates of 400kbps maximum in the Fast-mode.

A7	A6	A5	A4	A3	A2	A1	W/R
1	1	1	0	1	1	1	0

I²C slave address

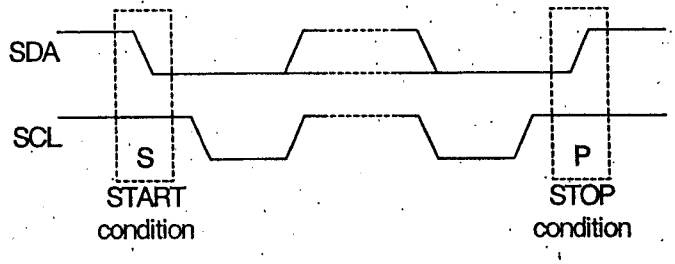
BIT TRANSFER

During "H" period of SCL, one data bit is transferred. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.



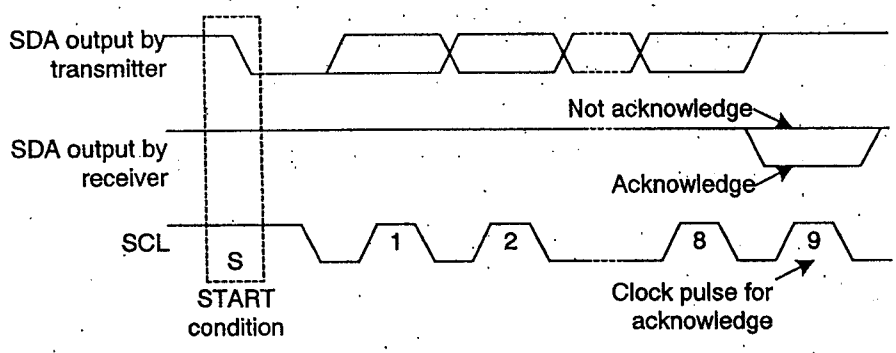
START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).



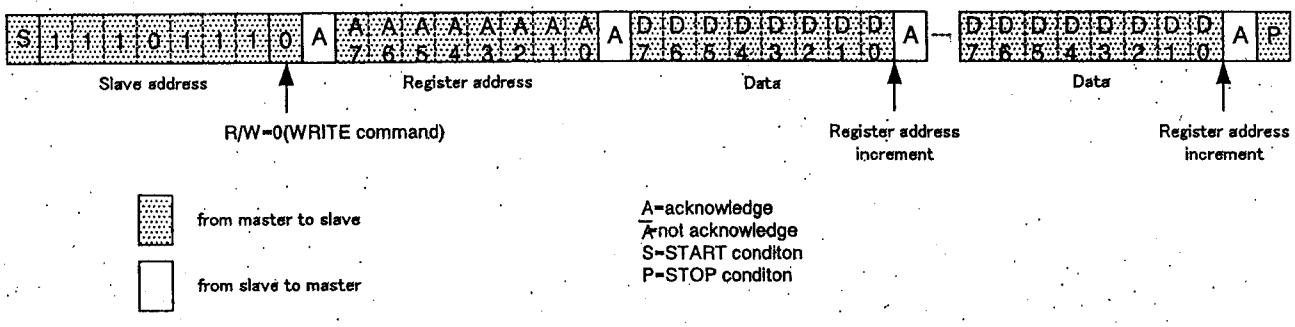
ACKNOWLEDGE

After the occurrence of START condition, each byte of eight bits is followed. A receiver must generate an acknowledge by pulling down the SDA line after the reception of each byte. In this event the transmitter leave the SDA line.

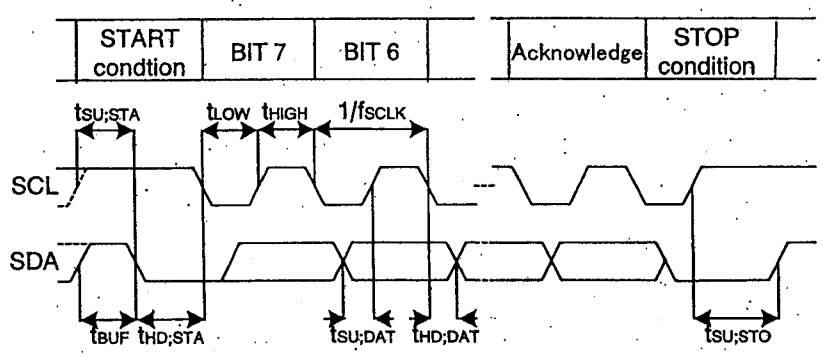


REGISTER WRITING PROTOCOL

The following sentence is about writing protocol. After transmitting the slave address and WRITE command (first byte), the register address of BU7875GLS is transferred (second byte). The third byte is the register data of this register address (second byte). After the register data (third byte), it is possible to send the register data consecutively. The address is automatically increased. But the next register address becomes 00h when the register address becomes final address (3Fh). After finishing the transmission, the register address is increased.



Timing diagram



● REGISTER MAP

Address	Initial Value	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	00h	W	-	-	-	Divs	Irqe	Inv1	Inv0	Pwr
01h	01h	W	-	-	-	Frme	Rpt			
02h	00h	W	Base							
03h	01h	W	-	-	-	-	-	-	-	Clo1
04h	19h	W	Clo0							
05h	00h	W	-	-	-	-	-	-	-	Chi1
06h	8Fh	W	Chi0							
07h	00h	W	-	-	Hlo1					
08h	ABh	W	Hlo0							
09h	01h	W	-	-	Hhi1					
0Ah	58h	W	Hhi0							
0Bh	00h	W	-	-	D0lo1					
0Ch	14h	W	D0lo0							
0Dh	00h	W	-	-	D0hi1					
0Eh	14h	W	D0hi0							
0Fh	00h	W	-	-	D1lo1					
10h	14h	W	D1lo0							
11h	00h	W	-	-	D1hi1					
12h	3Ch	W	D1hi0							
13h	00h	W	-	-	EndLen1					
14h	14h	W	EndLen0							
15h	20h	W	BitLen							
16h	00h	W	FrmLen1							
17h	00h	W	FrmLen0							
18h	00h	W	Out0							
19h	00h	W	Out1							
1Ah	00h	W	Out2							
1Bh	00h	W	Out3							
1Ch	00h	W	Out4							
1Dh	00h	W	Out5							
1Eh	00h	W	Out6							
1Fh	00h	W	Out7							
20h	00h	W	Out8							
21h	00h	W	Out9							
22h	00h	W	Out10							
23h	00h	W	Out11							
24h	00h	W	Out12							
25h	00h	W	Out13							
26h	00h	W	Out14							
27h	00h	W	Out15							
28h	00h	W	-	-	-	-	-	-	-	Irqc
29h	00h	W	-	-	-	-	-	-	-	Send
2Ah	00h	W	-	-	-	-	-	-	-	Rst
2Bh~3Fh	-	-	Reserved							
40h	-	-	Test Register							

※Don't access the 40h address.
This address is for test.

● DESCRIPTION OF REGISTER FUNCTION

Address 00h (Write)

	Description	Initial value	Operation
D4 (Divs)	Selection of divider	0	Divider in the system clock generator select 0: Carrier Divider 1: Base Clock Divider The system clock frequency is a reference of period setting for each part except carrier part (Clo, Chi) .
D3 (Irqe)	Permission of interrupt	0	Interrupt Mode Select 0: Mask Mode, NIRQ pin output "HIGH" 1: Permit Mode, NIRQ pin output "LOW" when this bit is "1" and the transmission buffer is null.
D2 (Inv1)	Data output period, Reversal of lo period (data1)	0	Data 1 Output Format Select 0: In "hi" part, outputting Carrier. 1: In "lo" part, outputting Carrier.
D1 (Inv0)	Data output period, Revered of lo period (data0)	0	Data 0 Output Format Select 0: In "hi" part, outputting Carrier. 1: In "lo" part, outputting Carrier.
D0 (Pwr)	Control of clock buffer	0	Clock Buffer (CLKI pin) Power Down Control 0: Power Down, The internal clock stop. DOUT pin outputs "LOW". NIRQ pin outputs "HIGH". 1: Power On

Address 01h (Write)

	Description	Initial value	Operation
D4 (Frme)	Control of frame interval	0	Frame Interval Control 0: Disable 1: Enable, It enable the time interval to set from the present transmission data to the next data.
D3~D0 (Rpt)	Setting of repetition times	1h	DOUT Output Times Control The setting value of this register is the repetition times (When Rpt =0h, the repetition times is 16). DOUT output is done setting times in this register. In case of setting this register, set Frme and FrmLen.

Address 02h (Write)

	Description	Initial value	Operation
D7~D0 (Base)	Setting of base clock frequency dividing	00h	Base Clock Frequency Control Base=00h, (Base clock cycle) = 1/ (CLKI input frequency) [sec] Exclude above, (Base clock cycle) = (2 × Base) / (CLKI input frequency) [sec]

Address 03h (Write)

	Description	Initial value	Operation
D0 (Clo1)	Setting the period of carrier lo (MSB)	1	Carrier "lo" (Clo) Period Control (the period of carrier lo)=(2^8xClo1+Clo0)/(CLKI input frequency) [sec]

Address 04h (Write)

	Description	Initial value	Operation
D7~D0 (Clo0)	Setting the period of carrier lo (the lower 8 bit)	19h	Carrier "lo" (Clo) Period Control (the period of carrier lo)=(2^8xClo1+Clo0)/(CLKI input frequency) [sec]

Address 05h (Write)

	Description	Initial value	Operation
D0 (Chi1)	Setting the period of carrier hi (MSB)	0	Carrier "hi" (Chi) Period Control (the period of carrier hi)=(2^8xChi1+Chi0)/(CLKI input frequency) [sec]

Address 06h (Write)

	Description	Initial value	Operation
D7~D0 (Chi0)	Setting the period of carrier hi (the lower 8 bit)	8Fh	Carrier "hi" (Chi) Period Control (the period of carrier hi)=(2^8xChi1+Chi0)/(CLKI input frequency) [sec]

・(System clock frequency) = 1 / (the period of carrier lo + the period of carrier hi) [Hz] (Divs = 0)
1 / (Base clock frequency) [Hz] (Divs = 1)

Address 07h (Write)

	Description	Initial value	Operation
D5~D0 (Hlo1)	Setting the period of header lo part (the upper 6bit)	00h	Header "lo" (Hlo) Period Control (the period of header lo)=(2^8x Hlo1+Hlo0)/(system clock frequency) [sec]

Address 08h (Write)

	Description	Initial value	Operation
D7~D0 (Hlo0)	Setting the period of header lo part (the lower 8 bit)	ABh	Header "lo" (Hlo) Period Control (the period of header lo)=(2^8x Hlo1+Hlo0)/(system clock frequency) [sec]

Address 09h (Write)

	Description	Initial value	Operation
D5~D0 (Hhi1)	Setting the period of header hi part (the upper 6bit)	01h	Header "hi" (Hhi) Period Control (the period of header hi)=(2^8x Hhi1+Hhi0)/(system clock frequency) [sec]

Address 0Ah (Write)

	Description	Initial value	Operation
D7~D0 (Hhi0)	Setting the period of header hi part (the lower 8 bit)	58h	Header "hi" (Hhi) Period Control (the period of header hi)=(2^8x Hhi1+Hhi0)/(system clock frequency) [sec]

Address 0Bh (Write)

	Description	Initial value	Operation
D5~D0 (D0lo1)	Setting the period of data 0 lo part (the upper 6bit)	00h	Data 0 "lo" (D0lo) Period Control (the period of data 0 lo)=(2^8x D0lo1+D0lo0)/(system clock frequency) [sec]

Address 0Ch (Write)

	Description	Initial value	Operation
D7~D0 (D0lo0)	Setting the period of data 0 lo part (the lower 8 bit)	14h	Data 0 "lo" (D0lo) Period Control (the period of data 0 lo)=(2^8x D0lo1+D0lo0)/(system clock frequency) [sec]

Address 0Dh (Write)

	Description	Initial value	Operation
D5~D0 (D0hi1)	Setting the period of data 0 hi part (the upper 6bit)	00h	Data 0 "hi" (D0hi) Period Control (the period of data 0 hi)=(2^8x D0hi1+D0hi0)/(system clock frequency) [sec]

Address 0Eh (Write)

	Description	Initial value	Operation
D7~D0 (D0hi0)	Setting the period of data 0 hi part (the lower 8 bit)	14h	Data 0 "hi" (D0hi) Period Control (the period of data 0 hi)=(2^8x D0hi1+D0hi0)/(system clock frequency) [sec]

Address 0Fh (Write)

	Description	Initial value	Operation
D5~D0 (D1lo1)	Setting the period of data 1 lo part (the upper 6bit)	00h	Data 1 "lo" (D1lo) Period Control (the period of data 1 lo)=(2^8x D1lo1+D1lo0)/(system clock frequency) [sec]

Address10h (Write)

	Description	Initial value	Operation
D7~D0 (D1lo0)	Setting the period of data 1 lo part (the lower 8 bit)	14h	Data 1 "lo" (D1lo) Period Control (the period of data 1 lo)=(2^8x D1lo1+D1lo0)/(system clock frequency) [sec]

Address 11h (Write)

	Description	Initial value	Operation
D5~D0 (D1hi1)	Setting the period of data 1 hi part (the upper 6bit)	00h	Data 1 "hi" (D1hi) Period Control (the period of data 1 hi)=(2^8x D1hi1+D1hi0)/(system clock frequency) [sec]

Address 12h (Write)

	Description	Initial value	Operation
D7~D0 (D1hi0)	Setting the period of data 1 hi part (the lower 8 bit)	3Ch	Data 1 "hi" (D1hi) Period Control (the period of data 1 hi)=(2^8x D1hi1+D1hi0)/(system clock frequency) [sec]

Address13h (Write)

	Description	Initial value	Operation
D5~D0 (EndLen1)	Setting output period of End part	00h	End Period Control (the period of End)=(2^8x EndLen1+EndLen0)/(system clock frequency) [sec]

Address 14h (Write)

	Description	Initial value	Operation
D7~D0 (EndLen0)	Setting output period of End part (the lower 8 bit)	14h	End Period Control (the period of End)=(2^8x EndLen1+EndLen0)/(system clock frequency) [sec]

Address 15h (Write)

	Description	Initial value	Operation
D7~D0 (BitLen)	Setting the output bit length of data part	20h	Output Bit Length of Data part Control The output data is transferred from Out0 with LSB first. When BitLen=00h, the output of Data part is not.

Address16h (Write)

	Description	Initial value	Operation
D7~D0 (FrmLen1)	Setting the frame interval (the upper 8bit)	00h	Frame Interval Control (the frame interval) = (2^8 x FrmLen1+FrmLen0) / (system clock frequency) [sec] When the frame interval is controlled, the frame interval must be set more than the following value. (Hhl+Hlo)+max{(D0hi+D0lo), (D1hi+D1ho)} × (BitLen)+(EndLen)+4 (The max(x) selects the greater one in the brace.)

Address 17h (Write)

	Description	Initial value	Operation
D7~D0 (FrmLen0)	Setting the frame interval (the lower 8 bit)	00h	Frame Interval Control (the frame interval) = (2^8 x FrmLen1+FrmLen0) / (system clock frequency) [sec] When the frame interval is controlled, the frame interval must be set more than the following value. (Hhl+Hlo)+max{(D0hi+D0lo), (D1hi+D1ho)} × (BitLen)+(EndLen)+4 (The max function selects the greater one in the brace.)

Address 18h (Write)

	Description	Initial value	Operation
D7~D0 (Out0)	Setting output data	00h	Setting Output Data of Out0 The output data is transferred from Out0 with LSB first. Setting data bit "1" : Output data "1" (from DOUT pin) Setting data bit "0" : Output data "0" (from DOUT pin)

Address 19h (Write)

	Description	Initial value	Operation
D7~D0 (Out1)	Setting output data	00h	Setting Output Data of Out1

Address 1Ah (Write)

	Description	Initial value	Operation
D7~D0 (Out2)	Setting output data	00h	Setting Output Data of Out2

Address 1Bh (Write)

	Description	Initial value	Operation
D7~D0 (Out3)	Setting output data	00h	Setting Output Data of Out3

Address 1Ch (Write)

	Description	Initial value	Operation
D7~D0 (Out4)	Setting output data	00h	Setting Output Data of Out4

Address 1Dh (Write)

	Description	Initial value	Operation
D7~D0 (Out5)	Setting output data	00h	Setting Output Data of Out5

Address 1Eh (Write)

	Description	Initial value	Operation
D7~D0 (Out6)	Setting output data	00h	Setting Output Data of Out6

Address 1Fh (Write)

	Description	Initial value	Operation
D7~D0 (Out7)	Setting output data	00h	Setting Output Data of Out7

Address 20h (Write)

	Description	Initial value	Operation
D7~D0 (Out8)	Setting output data	00h	Setting Output Data of Out8

Address 21h (Write)

	Description	Initial value	Operation
D7~D0 (Out9)	Setting output data	00h	Setting Output Data of Out9

Address 22h (Write)

	Description	Initial value	Operation
D7~D0 (Out10)	Setting output data	00h	Setting Output Data of Out10

Address 23h (Write)

	Description	Initial value	Operation
D7~D0 (Out11)	Setting output data	00h	Setting Output Data of Out11

Address 24h (Write)

	Description	Initial value	Operation
D7~D0 (Out12)	Setting output data	00h	Setting Output Data of Out12

Address 25h (Write)

	Description	Initial value	Operation
D7~D0 (Out13)	Setting output data	00h	Setting Output Data of Out13

Address 26h (Write)

	Description	Initial value	Operation
D7~D0 (Out14)	Setting output data	00h	Setting Output Data of Out14

Address 27h (Write)

	Description	Initial value	Operation
D7~D0 (Out15)	Setting output data	00h	Setting Output Data of Out15

Address 28h (Write)

	Description	Initial value	Operation
D0 (Irqc)	Clearing the internal interrupt factor	0	1: The internal interrupt factor is cleared.

Address 29h (Write)

	Description	Initial value	Operation
D0 (Send)	Starting the transmission	0	0: Not Send 1: Send The contents of the register setting are forwarded to the transmission buffer, and the transmission starts in the DOUT pin. After forwarding to the transmission buffer, this bit is set "0". At the same time, the internal input factor is cleared.

Address 2Ah (Write)

	Description	Initial value	Operation
D0 (Rst)	Reset	0	0: Not Reset 1: Reset When the condition of I^2C –bus is STOP, this bit is set "0" . The operation of this bit must not do with the operation of another address. This operation must be realized by accessing only this address on a sequence of the data transmission of I^2C bus (from STPRT condition to STOP condition).

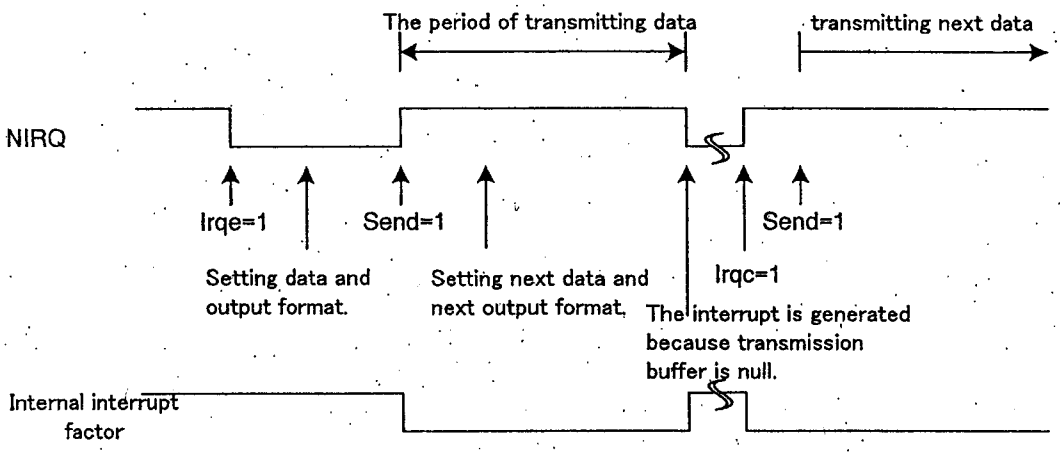
Address 2Bh~3Fh

Reserved

Address 40h

Don't access this address.
This address is for test.

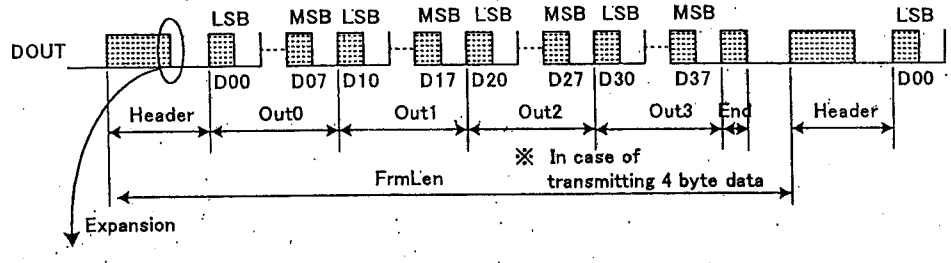
● INTERRUPT FUNCTION



When transmission buffer is null, internal interrupt factor is generated.
After the reset is released, transmission buffer becomes null.
When Send bit is set "1", the setting data is forwarded to the transmission buffer, and the transmission starts in the DOUT pin.
When the setting data is forward to the transmission buffer, the interrupt factor is cleared.
Also, when Irqc bit is set "1", the interrupt factor is cleared.
When Irqe bit is set "1", NIRQ pin outputs the interrupt factor condition because the internal interrupt factor is permitted.
When Irqe bit is set "0", NIRQ pin outputs "HIGH" because the internal interrupt factor is masked.

● OUTPUT FORMAT

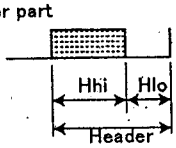
※ The whole format



※ Carrier part

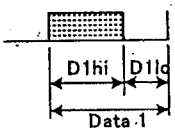
The rectangle part with net represent the pulse wave that like this.

※ Header part

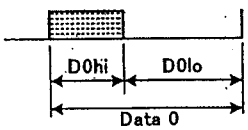


※ Data part

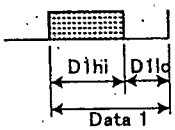
Data 1 (Inv1=0, Inv0=0)



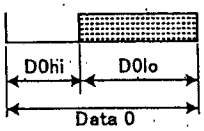
Data 0 (Inv1=0, Inv0=0)



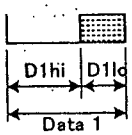
Data 1 (Inv1=0, Inv0=1)



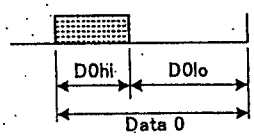
Data 0 (Inv1=0, Inv0=1)



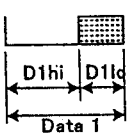
Data 1 (Inv1=1, Inv0=0)



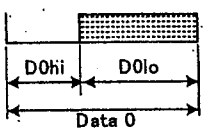
Data 0 (Inv1=1, Inv0=0)



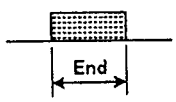
Data 1 (Inv1=1, Inv0=1)



Data 0 (Inv1=1, Inv0=1)



※ End part



● INITIAL VALUE OF REGISTER

Register name	Register setting	Time		Condition
	Initial value	Initial value	unit	
Base	00h	0.062	μs	CLKI=16.128MHz
Clo1, Clo0	1h, 19h	17.42	μs	CLKI=16.128MHz
Chi1, Chi0	0h, 8Fh	8.87	μs	CLKI=16.128MHz
Hlo1, Hlo0	00h, ABh	4.5	ms	carrier frequency=38kHz, Divs=0
Hhi1, Hhi0	01h, 58h	9.0	ms	carrier frequency=38kHz, Divs=0
D0lo1, D0lo0	00h, 14h	525.7	μs	carrier frequency=38kHz, Divs=0
D0hi1, D0hi0	00h, 14h	525.7	μs	carrier frequency=38kHz, Divs=0
D1lo1, D1lo0	00h, 14h	525.7	μs	carrier frequency=38kHz, Divs=0
D1hi1, D1hi0	00h, 3Ch	1577.4	μs	carrier frequency=38kHz, Divs=0
EndLen1, EndLen0	00h, 14h	525.7	μs	carrier frequency=38kHz, Divs=0
BitLen	20h	32	bit	
FrmLen1, FrmLen0	00h, 00h	0	μs	carrier frequency=38kHz, Divs=0

● RANGE OF REGISTER SETTING (Divs=0)

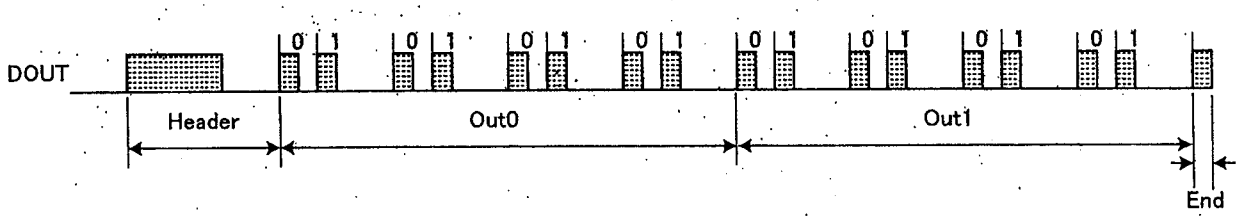
Register name	The enable range of register setting		Time (CLKI=16.128MHz)		unit
	min.	max.	min.	max.	
Base	00h	FFh	0.062	31.622	μs
Clo1, Clo0	0h, 01h	1h, FFh	0.062	31.684	μs
Chi1, Chi0	0h, 01h	1h, FFh	0.062	31.684	μs
Hlo1, Hlo0	00h, 00h	3Fh, FFh	0	16383	carrier cycle
Hhi1, Hhi0	00h, 00h	3Fh, FFh	0	16383	carrier cycle
D0lo1, D0lo0	00h, 01h	3Fh, FFh	1	16383	carrier cycle
D0hi1, D0hi0	00h, 01h	3Fh, FFh	1	16383	carrier cycle
D1lo1, D1lo0	00h, 01h	3Fh, FFh	1	16383	carrier cycle
D1hi1, D1hi0	00h, 01h	3Fh, FFh	1	16383	carrier cycle
EndLen1, EndLen0	00h, 00h	3Fh, FFh	0	16383	carrier cycle
BitLen	00h	80h	0	128	bit
FrmLen1, FrmLen0	①	FFh, FFh	①	65535	carrier cycle

※ Don't set the data that is out of the enable range in these register, because it is impossible to guarantee the operation.

① applies (Hhi+Hlo)+max{(D0hi+D0lo), (D1hi+D1ho)} × (Bit Len)+(End Len)+4 .

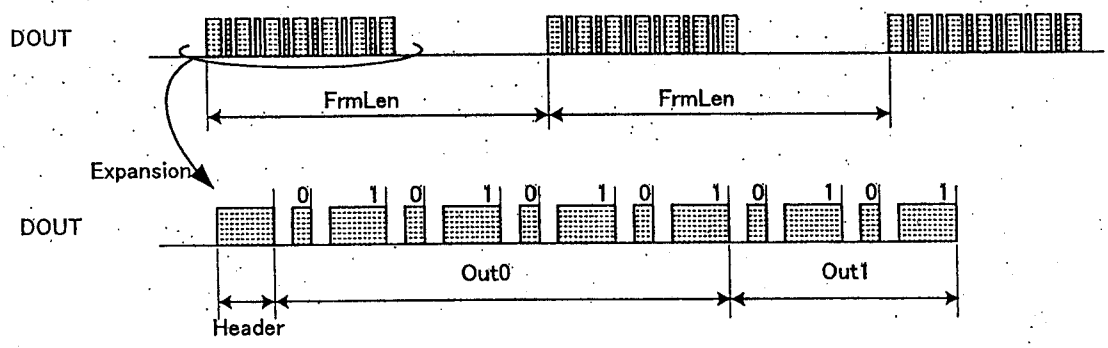
● EXAMPLE 1 OF REGISTER SETTING

Address	Register value	D7	D6	D5	D4	D3	D2	D1	D0
00h	01h	-	-	-	Divs	Irqe	Inv1	Inv0	Pwr
01h	01h	-	-	-	Frme	Rpt			
02h	00h	Base							
03h	01h	-	-	-	-	-	-	-	Clo1
04h	19h	Clo0							
05h	00h	-	-	-	-	-	-	-	Chi1
06h	8Fh	Chi0							
07h	00h	-	-	Hlo1					
08h	ABh	Hlo0							
09h	01h	-	-	Hhi1					
0Ah	58h	Hhi0							
0Bh	00h	-	-	D0lo1					
0Ch	14h	D0lo0							
0Dh	00h	-	-	D0hi1					
0Eh	14h	D0hi0							
0Fh	00h	-	-	D1lo1					
10h	3Ch	D1lo0							
11h	00h	-	-	D1hi1					
12h	14h	D1hi0							
13h	00h	-	-	EndLen1					
14h	14h	EndLen0							
15h	10h	BitLen							
16h	00h	FrmLen1							
17h	00h	FrmLen0							
18h	AAh	Out0							
19h	AAh	Out1							
:									
28h	00h	-	-	-	-	-	-	-	Irqc
29h	01h	-	-	-	-	-	-	-	Send



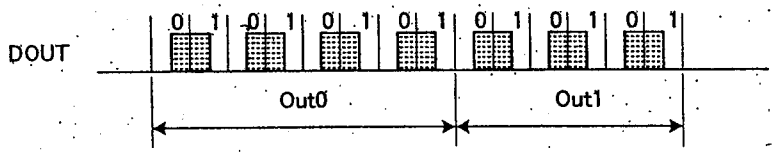
● EXAMPLE 2 OF REGISTER SETTING

Address	Register value	D7	D6	D5	D4	D3	D2	D1	D0
00h	07h	-	-	-	Divs	Irqe	Inv1	Inv0	Pwr
01h	13h	-	-	-	Frme	Rpt			
02h	00h	Base							
03h	01h	-	-	-	-	-	-	-	Clo1
04h	13h	Clo0							
05h	00h	-	-	-	-	-	-	-	Chi1
06h	81h	Chi0							
07h	00h	-	-	Hlo1					
08h	00h	Hlo0							
09h	00h	-	-	Hhi1					
0Ah	60h	Hhi0							
0Bh	00h	-	-	D0lo1					
0Ch	18h	D0lo0							
0Dh	00h	-	-	D0hi1					
0Eh	18h	D0hi0							
0Fh	00h	-	-	D1lo1					
10h	30h	D1lo0							
11h	00h	-	-	D1hi1					
12h	18h	D1hi0							
13h	00h	-	-	EndLen1					
14h	00h	EndLen0							
15h	0Ch	BitLen							
16h	08h	FrmLen1							
17h	34h	FrmLen0							
18h	AAh	Out0							
19h	AAh	Out1							
:									
28h	00h	-	-	-	-	-	-	-	Irqc
29h	01h	-	-	-	-	-	-	-	Send

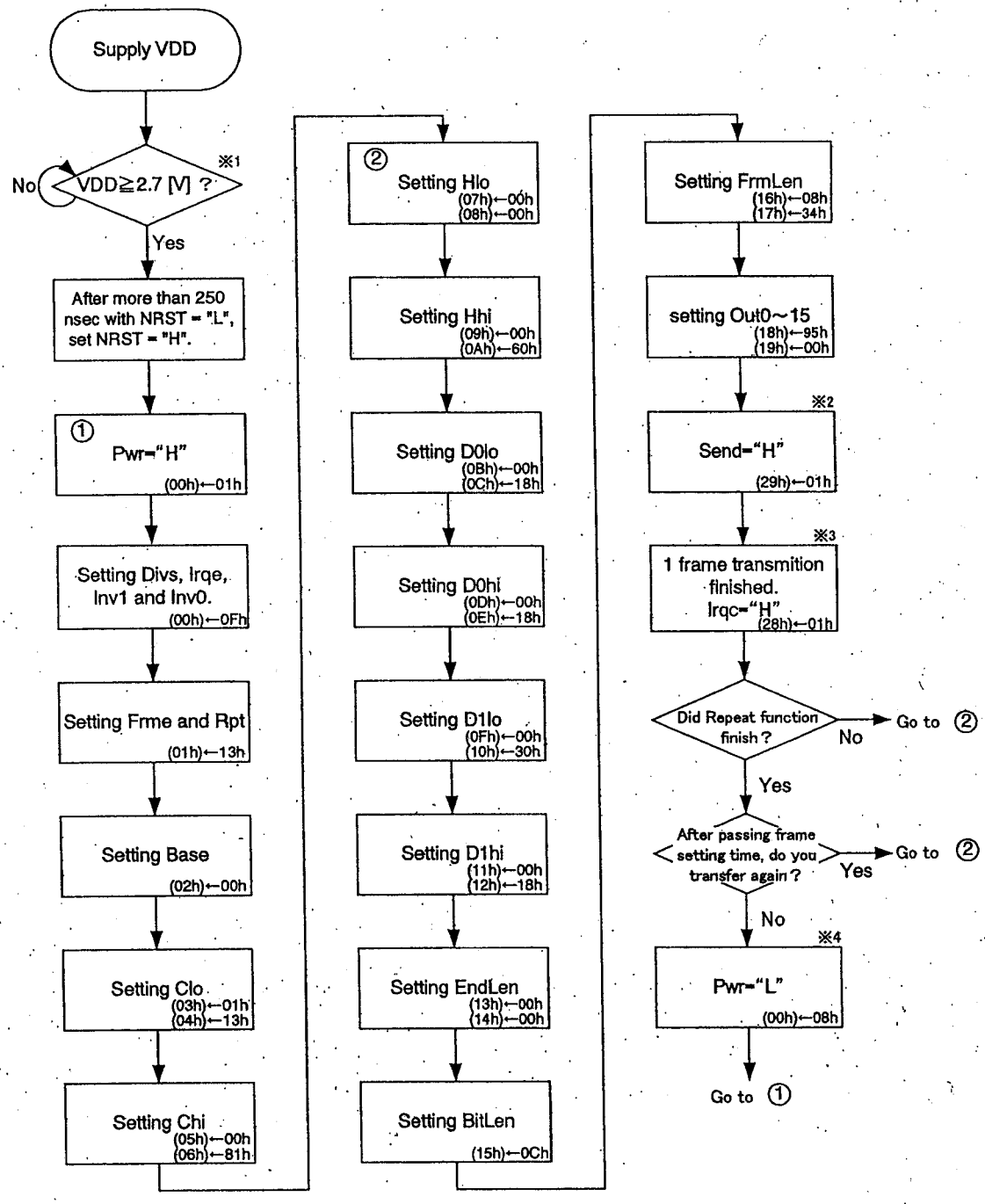


● EXAMPLE 3 OF REGISTER SETTING

Address	Register value	D7	D6	D5	D4	D3	D2	D1	D0
00h	03h	-	-	-	Divs	Irqe	Inv1	Inv0	Pwr
01h	01h	-	-	-	Frme	Rpt			
02h	00h	Base							
03h	01h	-	-	-	-	-	-	-	Clo1
04h	2Ah	Clo0							
05h	00h	-	-	-	-	-	-	-	Chi1
06h	98h	Chi0							
07h	00h	-	-	Hlo1					
08h	00h	Hlo0							
09h	00h	-	-	Hhi1					
0Ah	00h	Hhi0							
0Bh	00h	-	-	D0lo1					
0Ch	20h	D0lo0							
0Dh	00h	-	-	D0hi1					
0Eh	20h	D0hi0							
0Fh	00h	-	-	D1lo1					
10h	20h	D1lo0							
11h	00h	-	-	D1hi1					
12h	20h	D1hi0							
13h	00h	-	-	EndLen1					
14h	00h	EndLen0							
15h	0Eh	BitLen							
16h	00h	FrmLen1							
17h	00h	FrmLen0							
18h	AAh	Out0							
19h	AAh	Out1							
⋮									
28h	00h	-	-	-	-	-	-	-	Irqc
29h	01h	-	-	-	-	-	-	-	Send



● SETTING FLOW CHART



In this flow, the needless register setting can be omitted.
In the each process, the lower right-hand value is the example of the register setting. (AAh) ←DDh stands for writing data DDh at address AAh.
These setting values are the examples of register setting when the basis clock frequency is "16.128MHz".

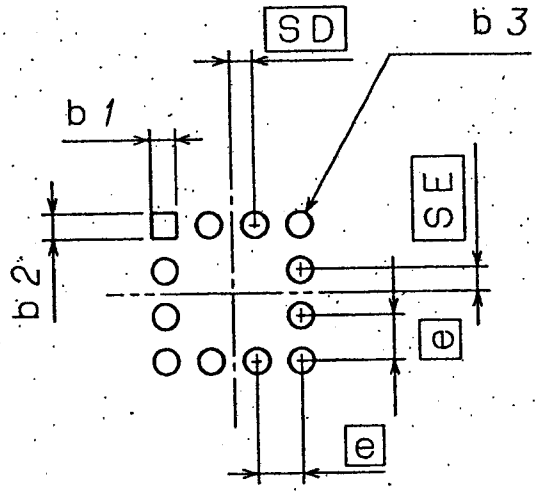
※1 After Supply VDD, it is possible to go to the next process when VDD ≧2.7 [V] constantly.

※2 When setting Send="H" again during outputting DOUT, DOUT output restart after the setting of repetition and frame interval.
The setting of Send command during outputting DOUT can set only once.
Also, in case of setting Send bit during outputting DOUT, wait more than 1/(system clock frequency) from the positive edge of acknowledge clock pulse for Send command to the finish of outputting DOUT.

※3 In case of setting Pwr ="L" after setting Irqc="H", wait more than 3/(system clock frequency) from the positive edge of acknowledge clock pulse for Irqc command to setting Pwr="L".

※4 In case of setting Pwr="L" after transferring 1 frame, wait more than 4/(system clock frequency) from the positive edge of NIRQ to setting Pwr="L".

● REFERENCE TERMINAL LAND AREA



(TOP VIEW)

Unit mm

Reference symbol	Reference value
e	0.80
b1	0.38
b2	0.38
b3	0.38
SD	0.40
SE	0.40

(Notes) Please set pattern design, taking into consideration flux cleaning conditions, solder joint strength, screen mask tolerance, bridge, heat dissipation and the others.

● EXAMPLE OF APPLICATION CIRCUIT

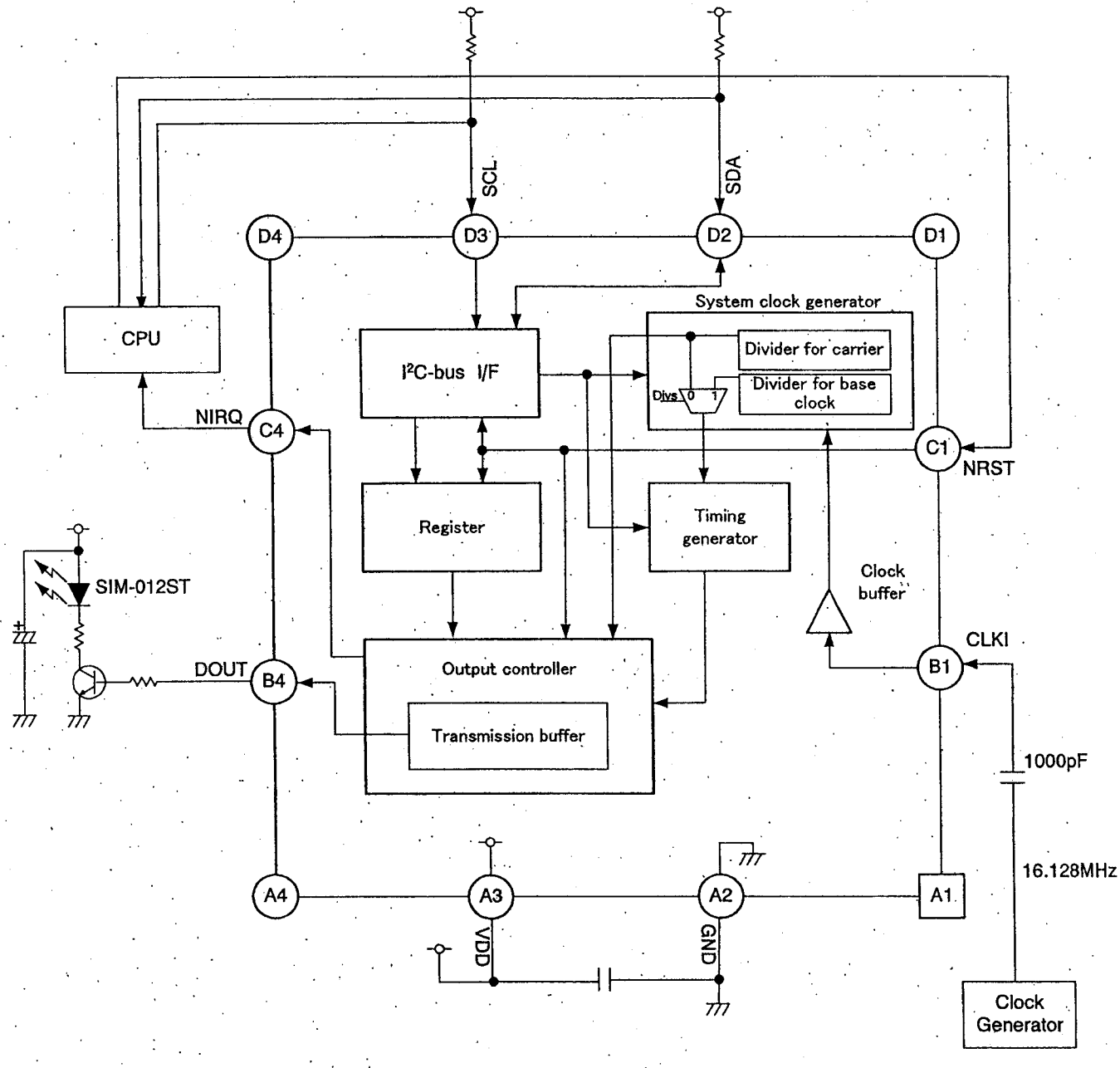


Fig. 4 Example of application circuit

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