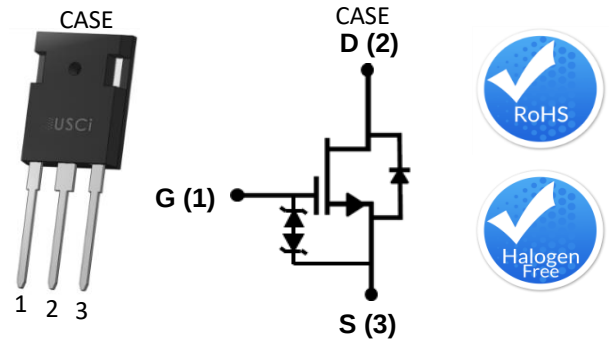


Description

United Silicon Carbide's cascode products co-package its high-performance G3 SiC JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. This series exhibits ultra-low gate charge, but also the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads, and any application requiring standard gate drive.



Part Number	Package	Marking
UF3C065040K3S	TO-247-3L	UF3C065040K3S

Features

- ♦ Typical on-resistance $R_{DS(on),typ}$ of 42mΩ
- ♦ Maximum operating temperature of 175°C
- ♦ Excellent reverse recovery
- ♦ Low gate charge
- ♦ Low intrinsic capacitance
- ♦ ESD protected, HBM class 2

Typical Applications

- ♦ EV charging
- ♦ PV inverters
- ♦ Switch mode power supplies
- ♦ Power factor correction modules
- ♦ Motor drives
- ♦ Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current ¹	I_D	$T_C=25^\circ\text{C}$	54	A
		$T_C=100^\circ\text{C}$	40	A
Pulsed drain current ²	I_{DM}	$T_C=25^\circ\text{C}$	125	A
Single pulsed avalanche energy ³	E_{AS}	$L=15\text{mH}$, $I_{AS}=3.19\text{A}$	76	mJ
Power dissipation	P_{tot}	$T_C=25^\circ\text{C}$	326	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J , T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	°C

1 Limited by $T_{J,max}$

2 Pulse width t_p limited by $T_{J,max}$

3 Starting $T_J = 25^\circ\text{C}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=0V, I_D=1mA$	650			V
Total drain leakage current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V, T_J=25^\circ\text{C}$		0.7	150	μA
		$V_{DS}=650V, V_{GS}=0V, T_J=175^\circ\text{C}$		10		
Total gate leakage current	I_{GSS}	$V_{DS}=0V, T_J=25^\circ\text{C}, V_{GS}=-20V / +20V$		6	± 20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=40A, T_J=25^\circ\text{C}$		42	52	mΩ
		$V_{GS}=12V, I_D=40A, T_J=175^\circ\text{C}$		78		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	4	5	6	V
Gate resistance	R_G	$f=1MHz, \text{open drain}$		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C=25^\circ\text{C}$			54	A
Diode pulse current ²	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			125	A
Forward voltage	V_{FSD}	$V_{GS}=0V, I_F=20A, T_J=25^\circ\text{C}$		1.5	1.75	V
		$V_{GS}=0V, I_F=20A, T_J=175^\circ\text{C}$		1.8		
Reverse recovery charge	Q_{rr}	$V_R=400V, I_F=40A, V_{GS}=-5V, R_{G_EXT}=20\Omega$		138		nC
Reverse recovery time	t_{rr}	$di/dt=1100A/\mu s, T_J=25^\circ\text{C}$		38		ns
Reverse recovery charge	Q_{rr}	$V_R=400V, I_F=40A, V_{GS}=-5V, R_{G_EXT}=20\Omega$		137		nC
Reverse recovery time	t_{rr}	$di/dt=1100A/\mu s, T_J=150^\circ\text{C}$		38		ns

Typical Performance - Dynamic

Parameter	symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS}=100V$, $V_{GS}=0V$, $f=100kHz$		1500		pF
Output capacitance	C_{oss}			200		
Reverse transfer capacitance	C_{rss}			2.2		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		146		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		325		pF
C_{oss} stored energy	E_{oss}	$V_{DS}=400V$, $V_{GS}=0V$		11.7		μJ
Total gate charge	Q_G	$V_{DS}=400V$, $I_D=40A$, $V_{GS}=-5V$ to 12V		43		nC
Gate-drain charge	Q_{GD}			11		
Gate-source charge	Q_{GS}			19		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=400V$, $I_D=40A$, Gate Driver=-5V to +12V, Turn-on $R_{G,EXT}=8.5\Omega$, Turn-off $R_{G,EXT}=20\Omega$ Inductive Load, FWD: same device with $V_{GS} = -5V$ and $R_G = 20\Omega$ RC snubber: $R_S=5\Omega$ and $C_S=330pF$ $T_J=25^\circ C$		73		ns
Rise time	t_r			24		
Turn-off delay time	$t_{d(off)}$			44		
Fall time	t_f			17		
Turn-on energy including R_S energy ⁴	E_{ON}			678		μJ
Turn-off energy including R_S energy ⁴	E_{OFF}			131		
Total switching energy including R_S energy ⁴	E_{TOTAL}			809		
Snubber R_S energy during turn-on	E_{RS_ON}			2.9		
Snubber R_S energy during turn-off	E_{RS_OFF}			9.7		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=400V$, $I_D=40A$, Gate Driver=-5V to +12V, Turn-on $R_{G,EXT}=8.5\Omega$, Turn-off $R_{G,EXT}=20\Omega$ Inductive Load, FWD: same device with $V_{GS} = -5V$ and $R_G = 20\Omega$ RC snubber: $R_S=5\Omega$ and $C_S=330pF$ $T_J=150^\circ C$		72		ns
Rise time	t_r			22		
Turn-off delay time	$t_{d(off)}$			45		
Fall time	t_f			17		
Turn-on energy including R_S energy ⁴	E_{ON}			679		μJ
Turn-off energy including R_S energy ⁴	E_{OFF}			138		
Total switching energy including R_S energy ⁴	E_{TOTAL}			817		
Snubber R_S energy during turn-on	E_{RS_ON}			2.8		
Snubber R_S energy during turn-off	E_{RS_OFF}			9.9		

⁴ The switching performance are evaluated with a RC snubber circuit as shown in Figure 1.

Thermal Characteristics

Parameter	symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.35	0.46	°C/W

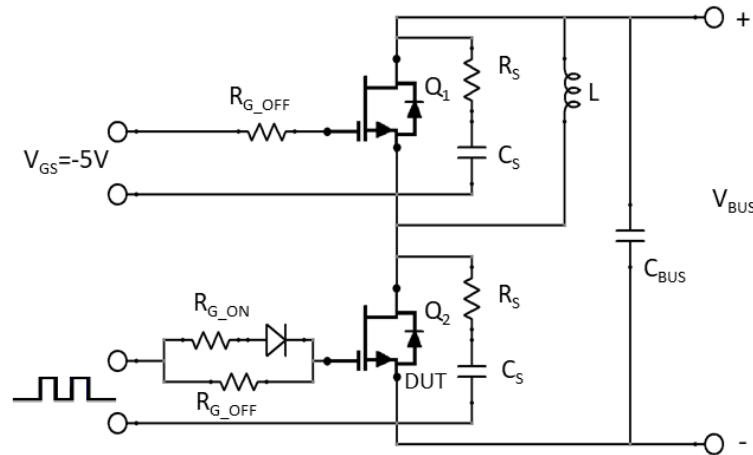


Figure 1 Inductive load switching test circuit

An RC snubber ($R_S=5\ \Omega$, $C_S=330\text{pF}$) is required to improve the turn-off waveforms.

Applications Information

SiC cascodes are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_g), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC cascodes also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the cascode is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on cascode operation, see www.unitedsic.com.

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