

N-Channel Super Junction Power MOSFET III

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

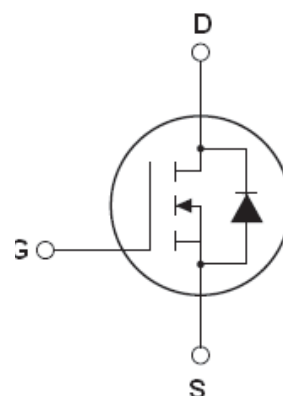
Features

- New technology for high voltage device
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)

V_{DS}	650	V
$R_{DS(ON)TYP}$	290	mΩ
I_D	11.5	A



Schematic diagram

Package Marking And Ordering Information

Device	Device Package	Marking
RM12N650LD	TO-252	12N650
RM12N650IP	TO-251	12N650



TO -252



TO -251

Table 1. Absolute Maximum Ratings ($T_C=25^\circ\text{C}$)

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS}=0V$)	V_{DS}	650	V
Gate-Source Voltage ($V_{DS}=0V$) AC ($f>1\text{ Hz}$)	V_{GS}	± 30	V
Continuous Drain Current at $T_C=25^\circ\text{C}$	$I_{D(DC)}$	11.5	A
Continuous Drain Current at $T_C=100^\circ\text{C}$	$I_{D(DC)}$	7	A
Pulsed drain current (Note 1)	I_{DM} (pulse)	46	A
Maximum Power Dissipation ($T_C=25^\circ\text{C}$)	P_D	101	W
Derate above 25°C		0.97	W/ $^\circ\text{C}$
Single pulse avalanche energy (Note2)	E_{AS}	144	mJ
Avalanche current (Note 1)	I_{AR}	6	A
Repetitive Avalanche energy, t_{AR} limited by T_{jmax} (Note 1)	E_{AR}	0.5	mJ

Parameter	Symbol	Value	Unit
Drain Source voltage slope, $V_{DS} \leq 480\text{ V}$,	dv/dt	50	V/ns
Reverse diode dv/dt , $V_{DS} \leq 480\text{ V}$, $I_{SD} < I_D$	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55...+150	°C

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R_{thJC}	1.24	°C /W
Thermal Resistance, Junction-to-Ambient (Maximum)	R_{thJA}	62	°C /W

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	650			V
Zero Gate Voltage Drain Current(Tc=25℃)	I _{DSS}	V _{DS} =650V, V _{GS} =0V			1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I _{DSS}	V _{DS} =650V, V _{GS} =0V			100	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	3	3.5	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =7A		290	360	mΩ
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz		870		pF
Output Capacitance	C _{oss}			54		pF
Reverse Transfer Capacitance	C _{rss}			1.8		pF
Total Gate Charge	Q _g	V _{DS} =480V, I _D =11.5A, V _{GS} =10V		19		nC
Gate-Source Charge	Q _{gs}			6		nC
Gate-Drain Charge	Q _{gd}			6.5		nC
Switching times						
Turn-on Delay Time	t _{d(on)}	V _{DD} =380V, I _D =5.8A, R _G =3Ω, V _{GS} =10V		11		nS
Turn-on Rise Time	t _r			8		nS
Turn-Off Delay Time	t _{d(off)}			58	70	nS
Turn-Off Fall Time	t _f			9	14	nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I _{SD}	T _c =25℃			11.5	A
Pulsed Source-drain current(Body Diode)	I _{SDM}				46	A
Forward on voltage	V _{SD}	T _j =25℃, I _{SD} =11.5A, V _{GS} =0V		0.9	1.2	V
Reverse Recovery Time	t _{rr}	T _j =25℃, I _F =5.8A, di/dt=100A/μs		220		nS
Reverse Recovery Charge	Q _{rr}			2.2		uC
Peak Reverse Recovery Current	I _{rrm}			19		A

Notes: 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2. $T_J=25^\circ C, V_{DD}=50V, V_G=10V, R_G=25\Omega$

RATING AND CHARACTERISTICS CURVES (RM12N650LD(IP))

Figure1. Safe operating area

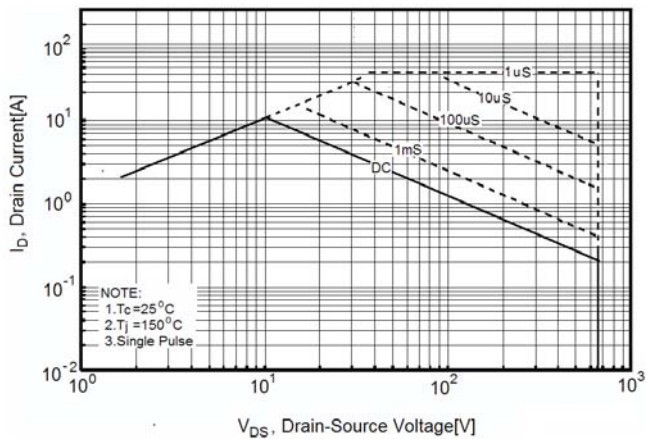


Figure2. Transient Thermal Impedance

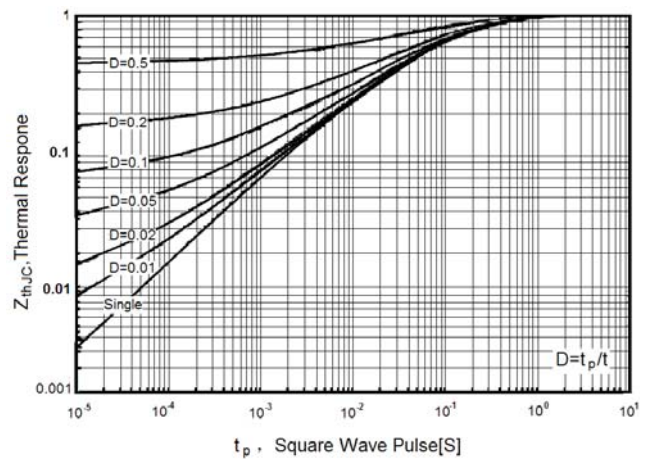


Figure3. Source-Drain Diode Forward Voltage

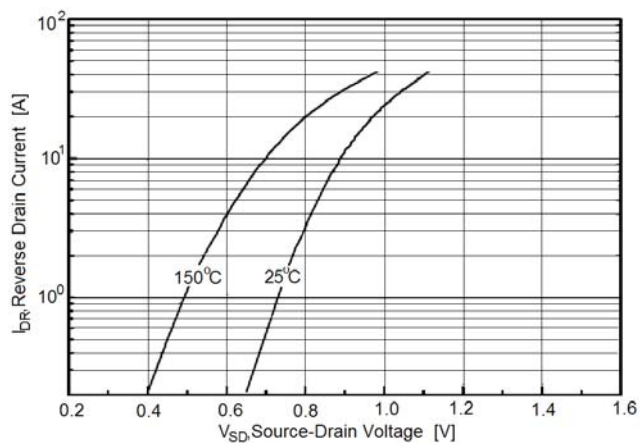


Figure4. Output characteristics

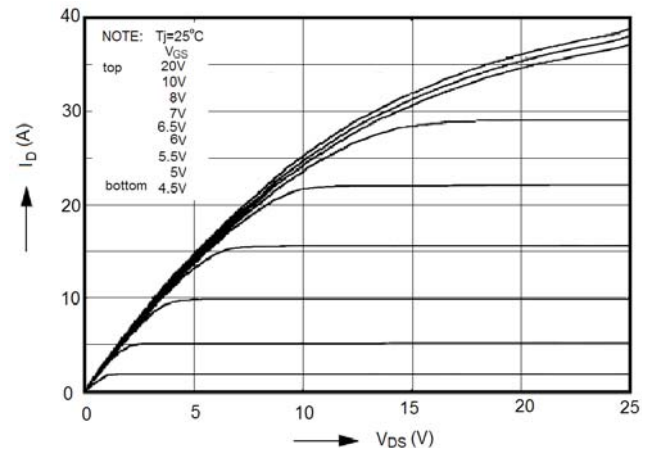


Figure5. Transfer characteristics

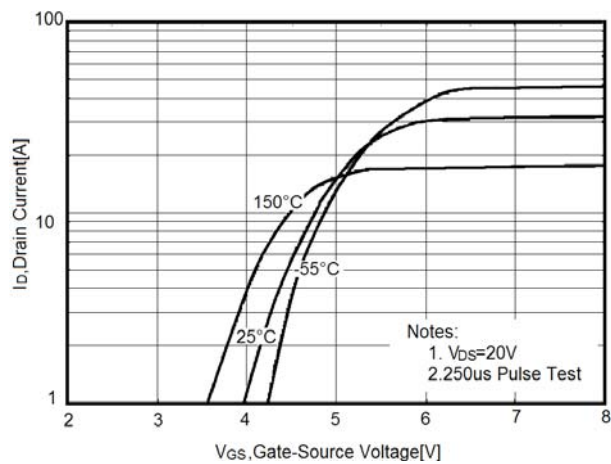
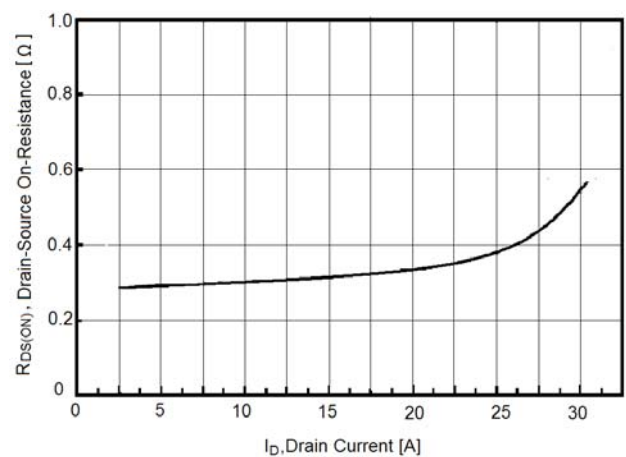


Figure6. Static drain-source on resistance



RATING AND CHARACTERISTICS CURVES (RM12N650LD(IP))

Figure7. $R_{DS(ON)}$ vs Junction Temperature

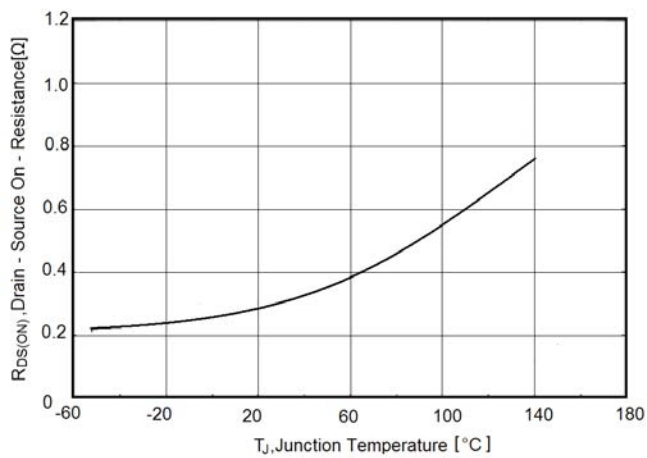


Figure8. BV_{DSS} vs Junction Temperature

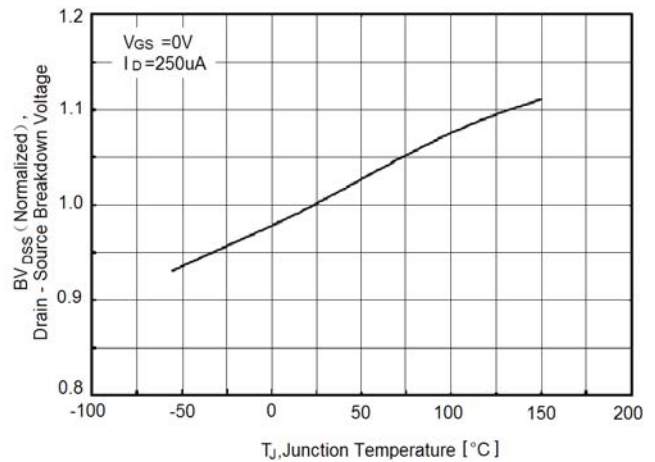


Figure9. Maximum I_D vs Junction Temperature

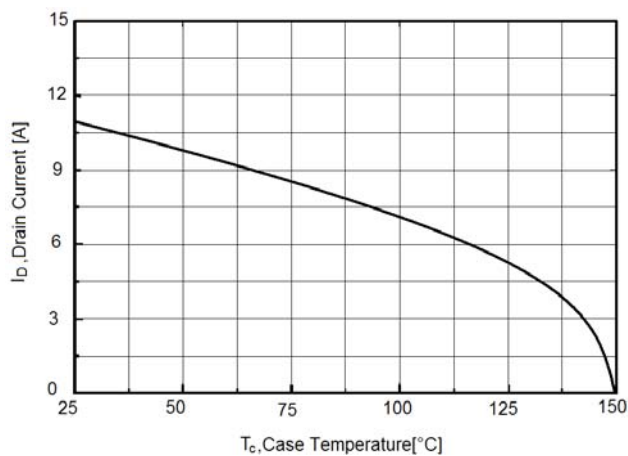


Figure10. Gate charge waveforms

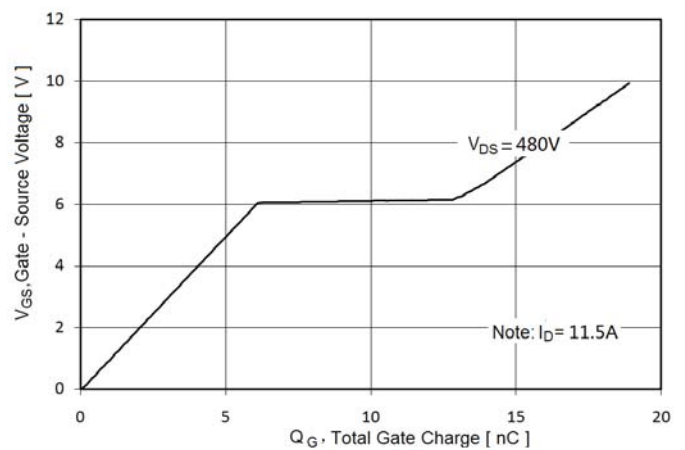
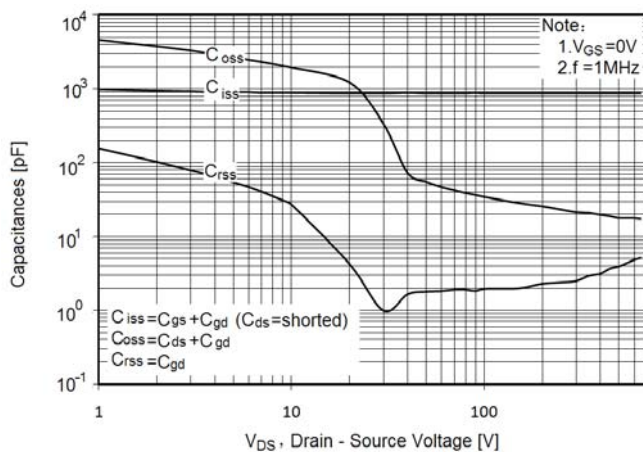
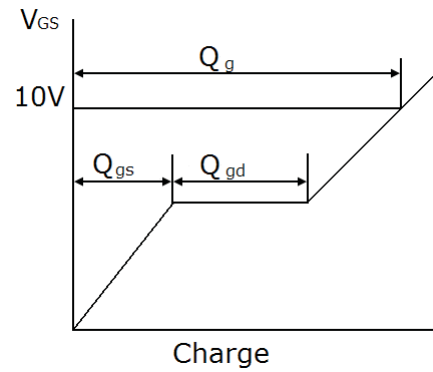
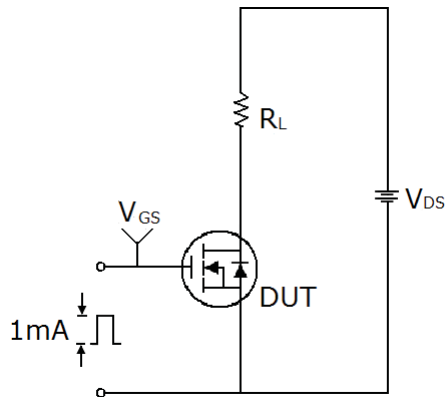


Figure11. Capacitance

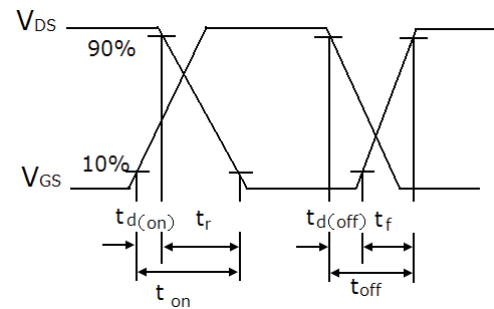
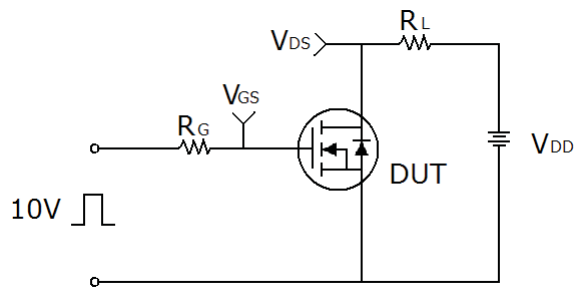


Test circuit

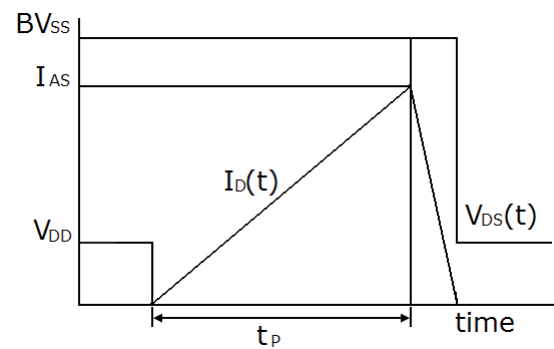
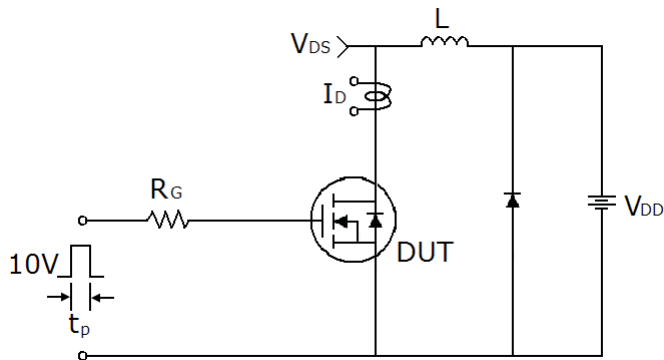
1) Gate charge test circuit & Waveform



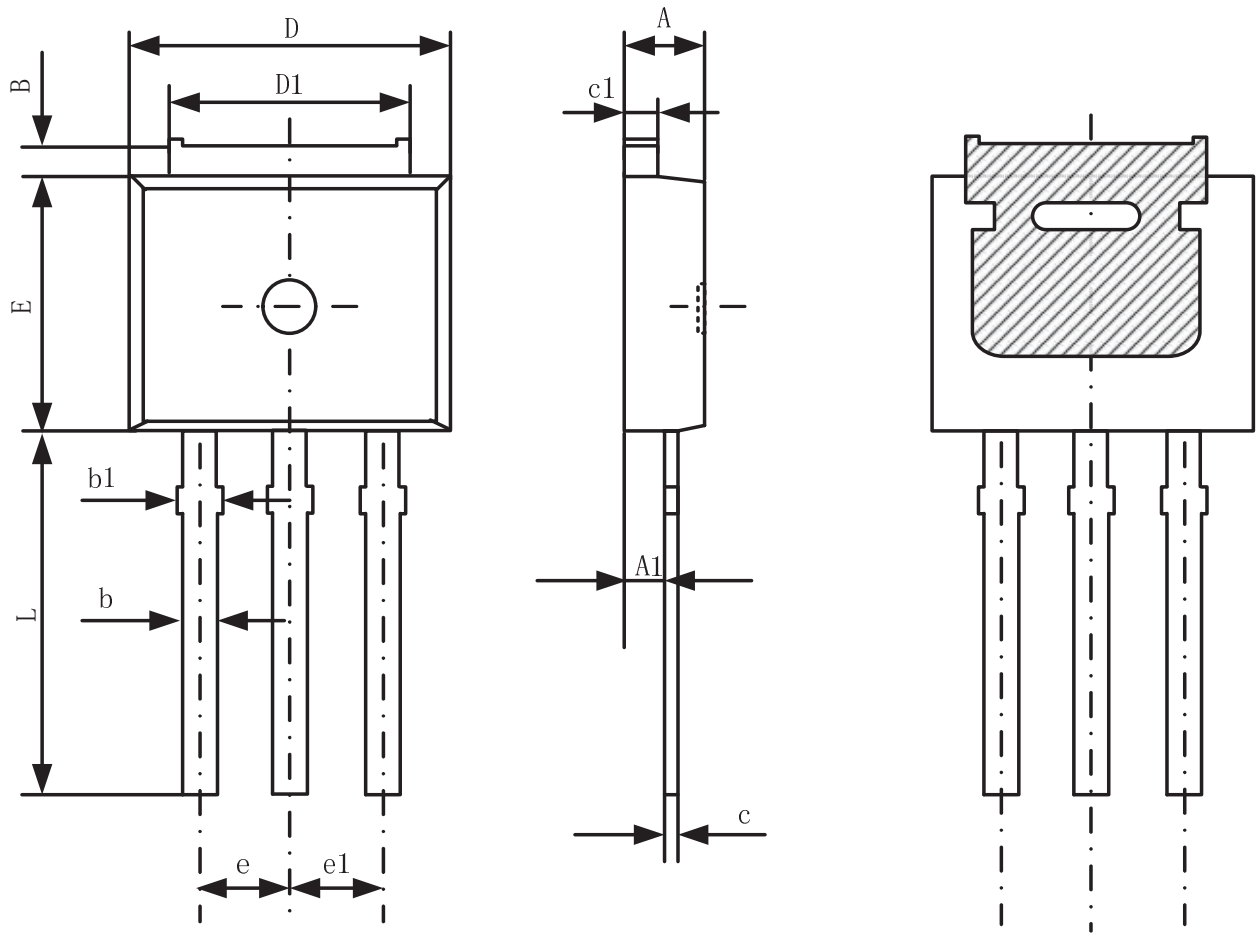
2) Switch Time Test Circuit:



3) Unclamped Inductive Switching Test Circuit & Waveforms

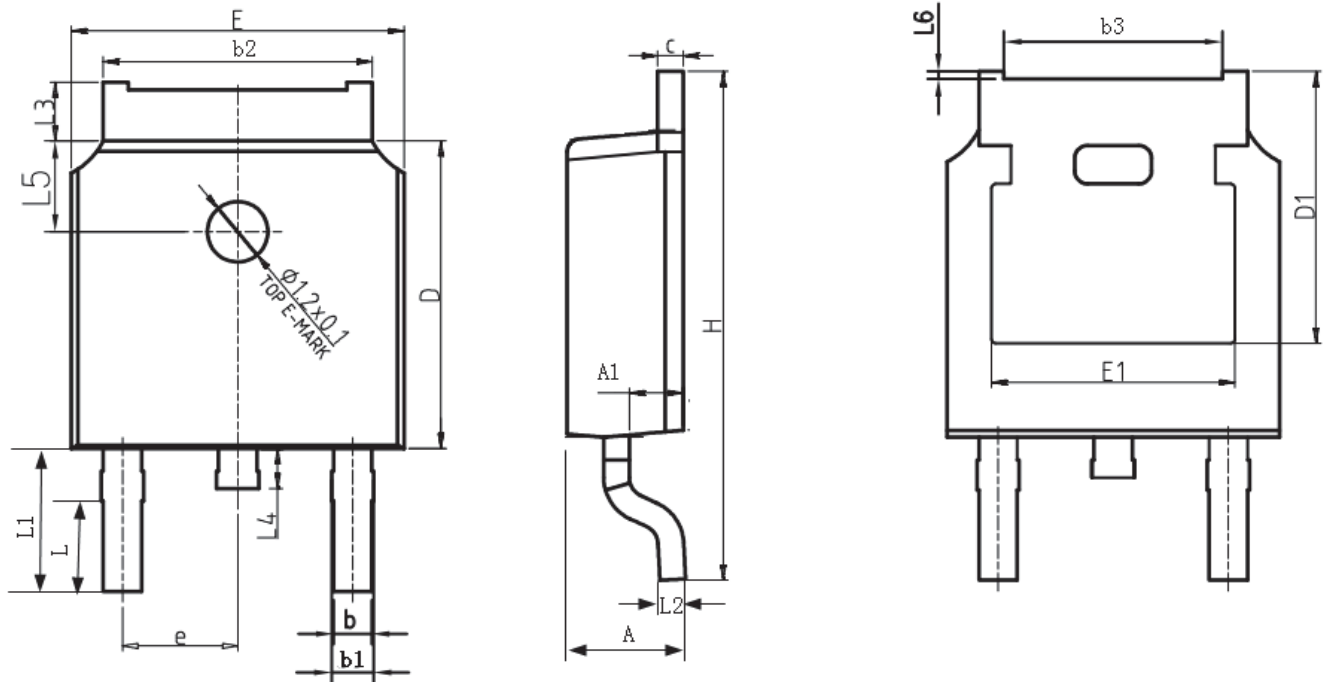


TO-251 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.100	2.500	0.083	0.099
A1	0.850	1.150	0.034	0.045
B	0.718	1.018	0.028	0.040
b	0.700	0.900	0.028	0.036
b1	0.700	1.000	0.028	0.040
c	0.408	0.608	0.016	0.024
c1	0.408	0.508	0.016	0.020
D	6.400	6.800	0.253	0.269
D1	5.180	5.480	0.205	0.217
E	5.950	6.350	0.235	0.251
e	2.286		0.090	
e1	2.286		0.090	
L	6.700	7.300	0.265	0.289

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.056	0.061
A1	0.970	1.17	0.025	0.030
b	0.720	0.850	0.018	0.022
b1	0.720	0.930	0.018	0.024
b2	5.230	5.460	0.133	0.139
b3	4.270	4.370	0.108	0.111
c	0.470	0.580	0.012	0.015
D	6.000	6.200	0.152	0.157
D1	5.300 TYP.		0.135	
E	6.500	6.700	0.165	0.170
E1	4.700	4.920	0.119	0.125
e	2.286 TYP		0.058	
L	1.400	1.700	0.036	0.043
L1	2.900 TYP.		0.074	
L2	0.510 TYP.		0.013	
L3	0.900	1.250	0.023	0.032
L4	0.600	1.000	0.015	0.025
L5	1.700	1.900	0.043	0.048
L6	0	0.1223	0.000	0.003



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Marking on the body



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