Description

The SX1N65D is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

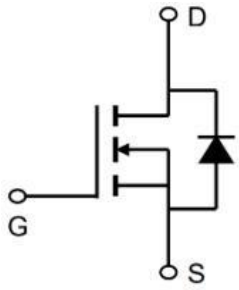
General Features

V_{DS} = 650V I_D =1.1A

$R_{DS(ON)}$ < 12Ω @ V_{GS}=10V

Application

LED



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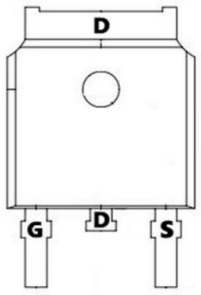


Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage (V_{GS} = 0V)	650	V
ID	Continuous Drain Current	1.2	A
IDM	Pulsed Drain Current (note1)	6.0	A
VGS	Gate-Source Voltage	±30	V
EAS	Single Pulse Avalanche Energy (note2)	25	mJ
P_D	Power Dissipation (T_C = 25ºC)	3	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	ºC
RthJC	Thermal Resistance, Junction-to-Case	5	ºC/W
RthJA	Thermal Resistance, Junction-to-Ambient	62.5	ºC/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	650	700	--	V
VGS(th)	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	3.0	4.0	V
RDS(on)	Drain-Source On-Resistance	V_{GS} = 10V, I_D = 0.5A	--	9	12	Ω
IDSS	Zero Gate Voltage Drain Current	V_{DS}=650V, V_{GS} = 0V, T_J = 25ºC	--	--	1	μA
		V_{DS}=520V, V_{GS} = 0V, T_J = 125ºC	--	--	100	
IGSS	Gate-Source Leakage	V_{GS} = ±30V	--	--	±100	nA
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS}=25V, f=1.0MHz	--	139	--	pF
C_{oss}	Output Capacitance		--	17	--	
C_{rss}	Reverse Transfer Capacitance		--	2	--	
Q_g	Total Gate Charge	V_{DD}=350V, I_D=0.8A, V_{GS}=10V	--	5.3	--	nC
Q_{gs}	Gate-Source Charge		--	0.7	--	
Q_{gd}	Gate-Drain Charge		--	2.6	--	
td(on)	Turn-on Delay Time	V_{DD}=350V, I_D=0.8A, R_G=25Ω	--	6	--	ns
t_r	Turn-on Rise Time		--	4.5	--	
td(off)	Turn-off Delay Time		--	27	--	
t_f	Turn-off Fall Time		--	16	--	
I_S	Continuous Body Diode Current	T_C=25ºC	--	--	1.2	A
ISM	Pulsed Diode Forward Current		--	--	6.0	
t_{rr}	Reverse Recovery Time	V_{GS} = 0V,I_S=0.8A, di_F/dt =100A /μs	--	65	--	ns
Q_{rr}	Reverse Recovery Charge		--	101	--	μC
V_{SD}	Body Diode Voltage	T_J = 25ºC, I_{SD} =0.8A, V_{GS} = 0V	--	--	1.5	V

Note：

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

3、The power dissipation is limited by 150℃junction temperature

4、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

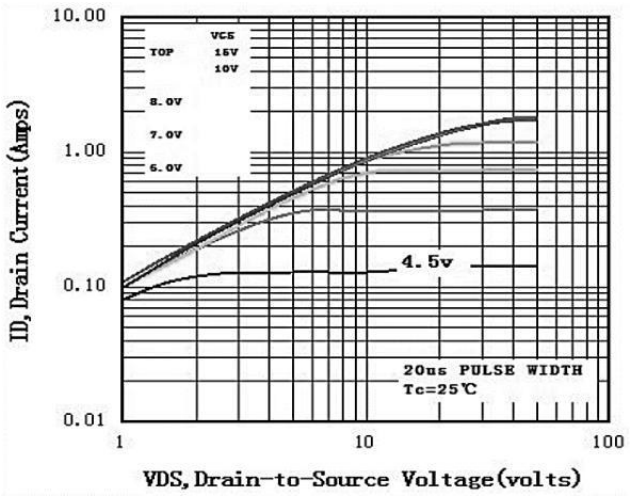


Figure1:Typical Output Characteristics（Tc=25℃）

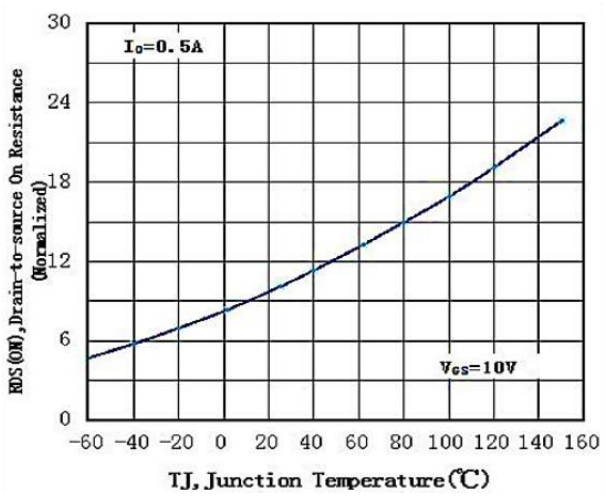


Figure2:On-Resistance Vs.Temperature

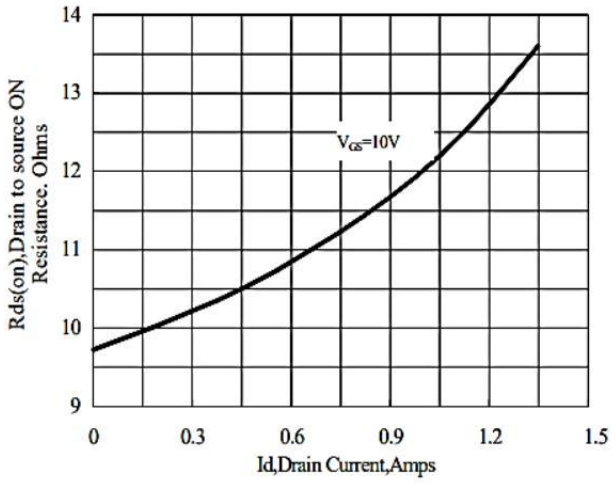


Figure3: Drain to Source ON Resistance vs Drain Current

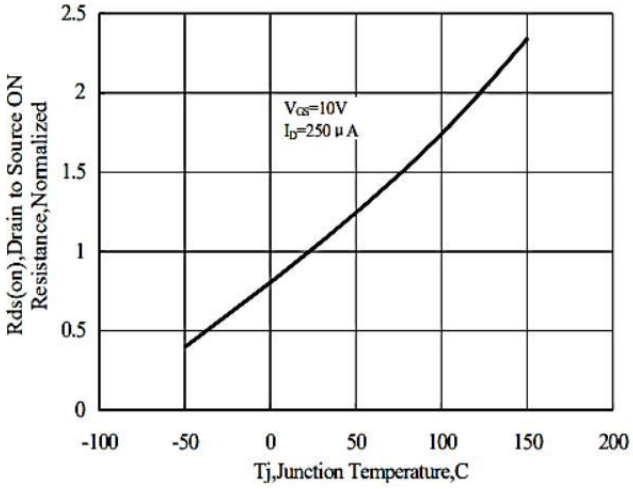


Figure4: Drianto Source on Resistance vs Junction Temperature

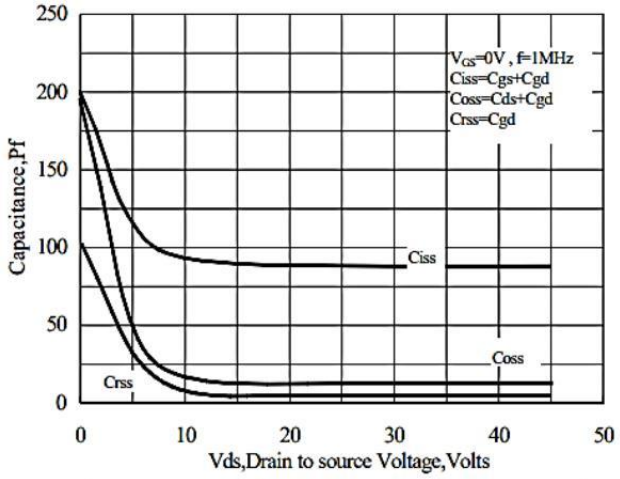


Figure5: Capacitance vs Drain to Source Voltage

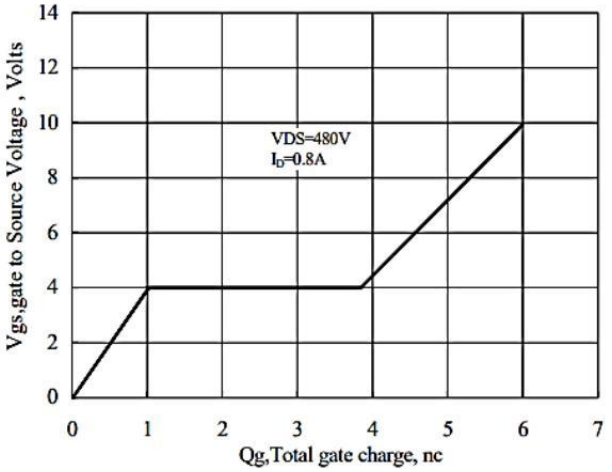


Figure6: Gate Charge vs Gate to Source Voltage

Typical Characteristics

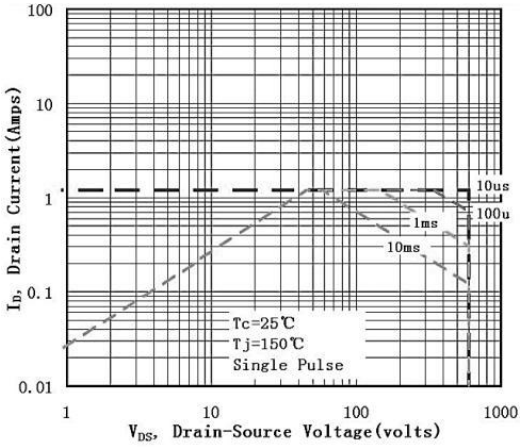


Figure5: Safe Operating Area

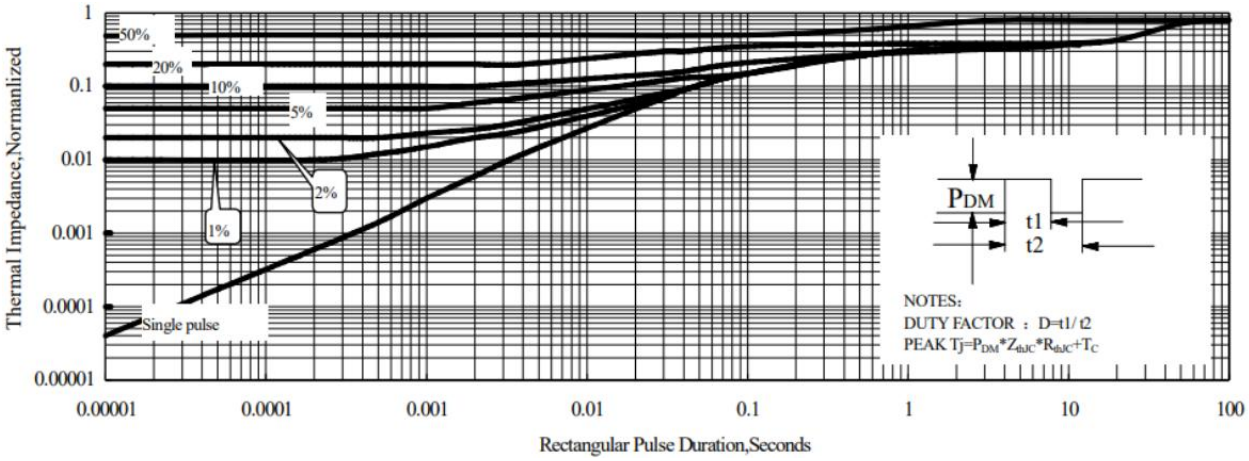
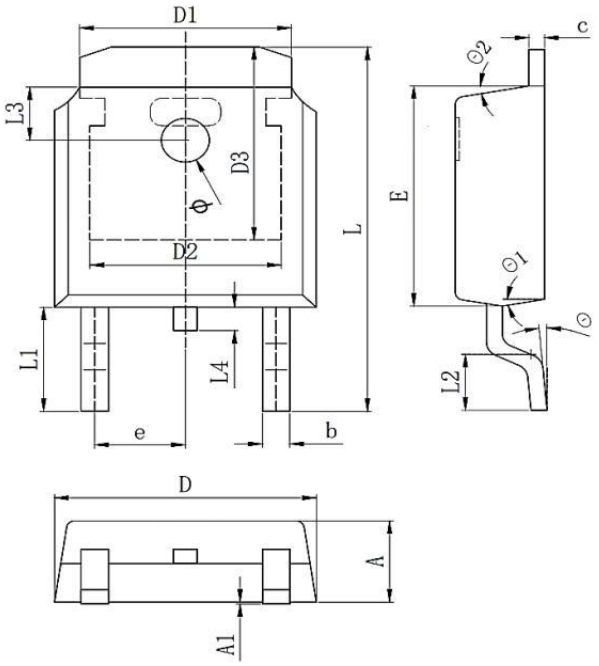


Figure6:Maximum Effective Thermal Impedance , Junction to Ambient

Package Mechanical Data-TO-252-3L



Symbol	Dim in mm		
	Min	Typ	Max
A	2.1	2.3	2.5
A1	0	0.064	0.128
b	0.64	0.75	0.86
c	0.45	0.52	0.6
D	6.4	6.6	6.8
D1		5.33REF	
D2		4.83REF	
D3		5.25REF	
E	5.9	6.1	6.3
e		2.286TYP	
L	9.8	10.1	10.4
L1		2.888REF	
L2	1.4	1.5	1.7
L3		1.65REF	
L4	0.6	0.8	1
ϕ	1.1	1.2	1.3
θ	0°		10°
θ1	5°		10°
θ2	5°		10°

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	TO-252-3L		2500