



PRODUCT DATA SHEET

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Datasheet



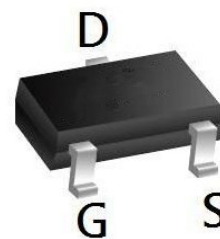
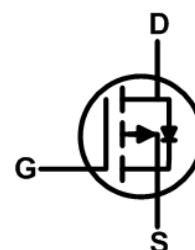
Resources



Samples

Please note: Please check the JINGAO Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.jg-semi.cn. Please email any questions regarding the system integration to JINGAO_questions@jgsemi.com.

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology


SOT23-3L


Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_A=25^{\circ}\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}^1$	-3	A
$I_D@T_A=70^{\circ}\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}^1$	-2.4	A
I_{DM}	Pulsed Drain Current ²	-6	A
EAS	Single Pulse Avalanche Energy ³	20	mJ
I_{AS}	Avalanche Current	-20	A
$P_D@T_A=25^{\circ}\text{C}$	Total Power Dissipation ⁴	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	85	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	50	$^{\circ}\text{C/W}$

Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=-250\mu A$	-60	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1mA$	---	-0.049	---	V/ $^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V$, $I_D=-3A$	---	115	140	$m\Omega$
		$V_{GS}=-4.5V$, $I_D=-2A$	---	---	190	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=-250\mu A$	-1.0	---	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	5.42	---	mV/ $^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-48V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=-48V$, $V_{GS}=0V$, $T_J=150^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V$, $I_D=-3A$	---	5.8	---	S
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-20V$, $V_{GS}=-4.5V$, $I_D=-3A$	---	5.9	---	nC
Q_{gs}	Gate-Source Charge		---	2.9	---	
Q_{gd}	Gate-Drain Charge		---	1.8	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-12V$, $V_{GS}=-10V$, $R_G=3.3\Omega$, $I_D=-3A$	---	10	---	ns
T_r	Rise Time		---	17	---	
$T_{d(off)}$	Turn-Off Delay Time		---	22	---	
T_f	Fall Time		---	21	---	
C_{iss}	Input Capacitance	$V_{DS}=-15V$, $V_{GS}=0V$, $F=1MHz$	---	715	---	pF
C_{oss}	Output Capacitance		---	51	---	
C_{rss}	Reverse Transfer Capacitance		---	34	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	---	---	-3	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	-6	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=-1A$, $T_J=25^{\circ}\text{C}$	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=-25V$, $V_{GS}=-10V$, $L=0.1mH$, $I_{AS}=-20A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Channel Typical Characteristics

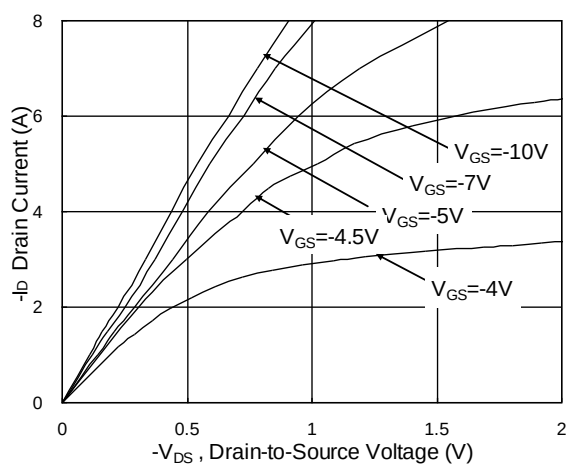


Fig.1 Typical Output Characteristics

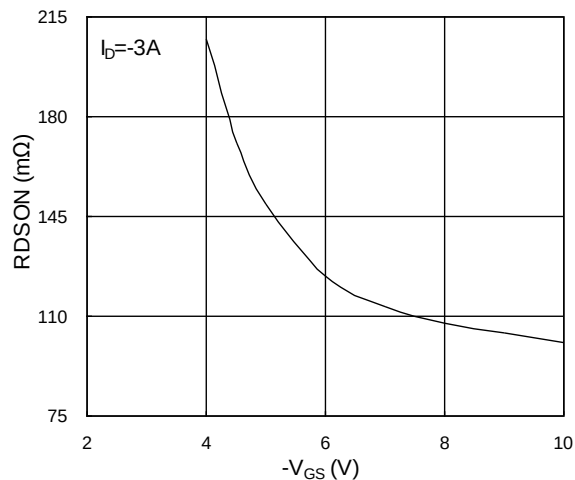


Fig.2 On-Resistance vs. G-S Voltage

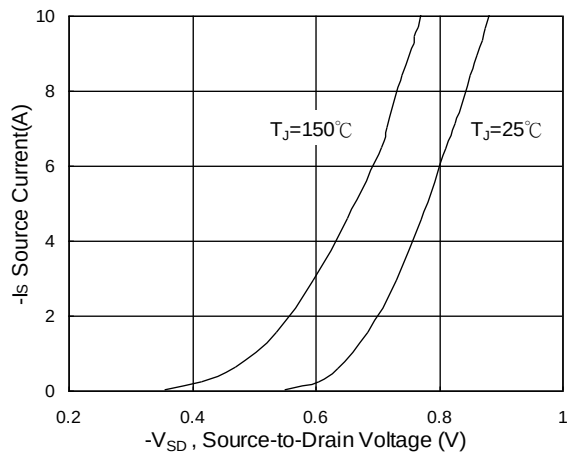


Fig.3 Forward Characteristics Of Reverse

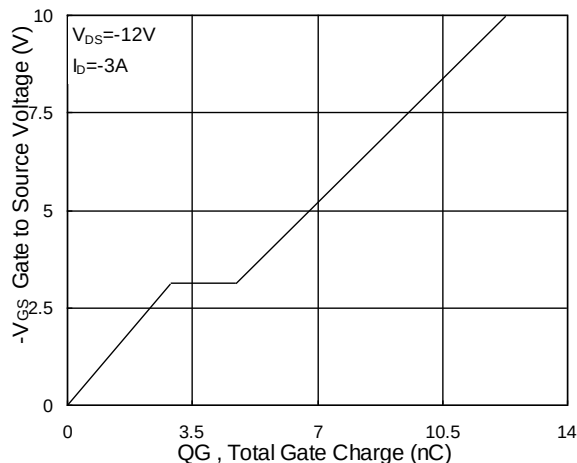


Fig.4 Gate-Charge Characteristics

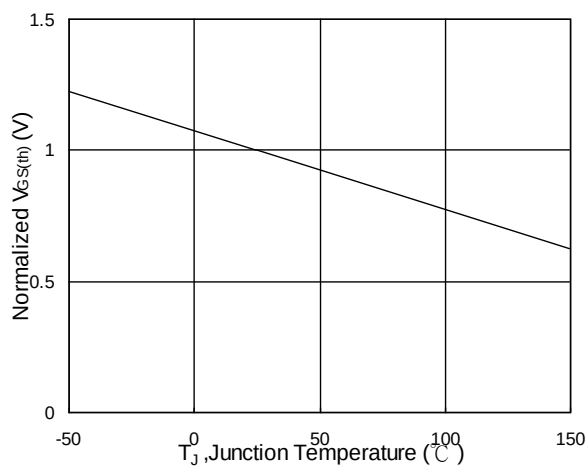


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

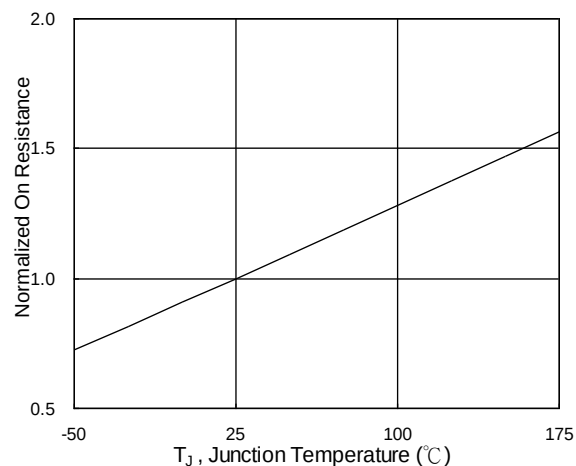
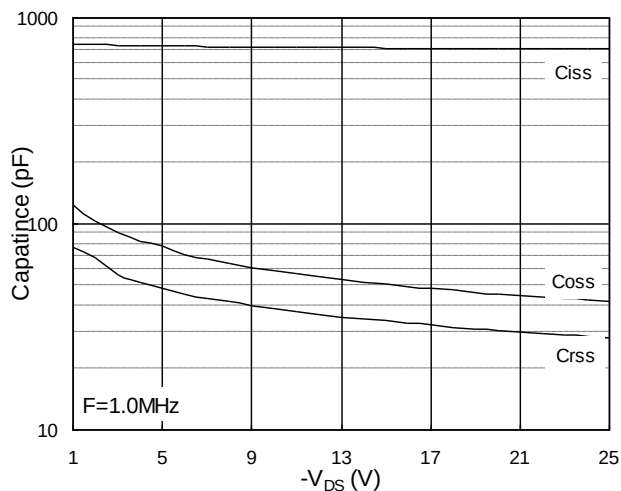
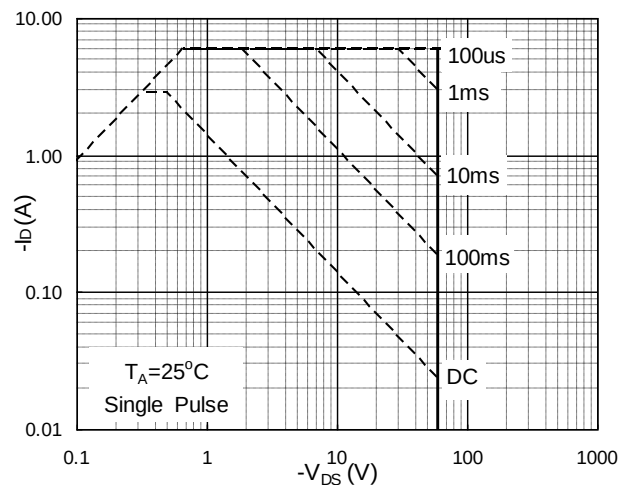
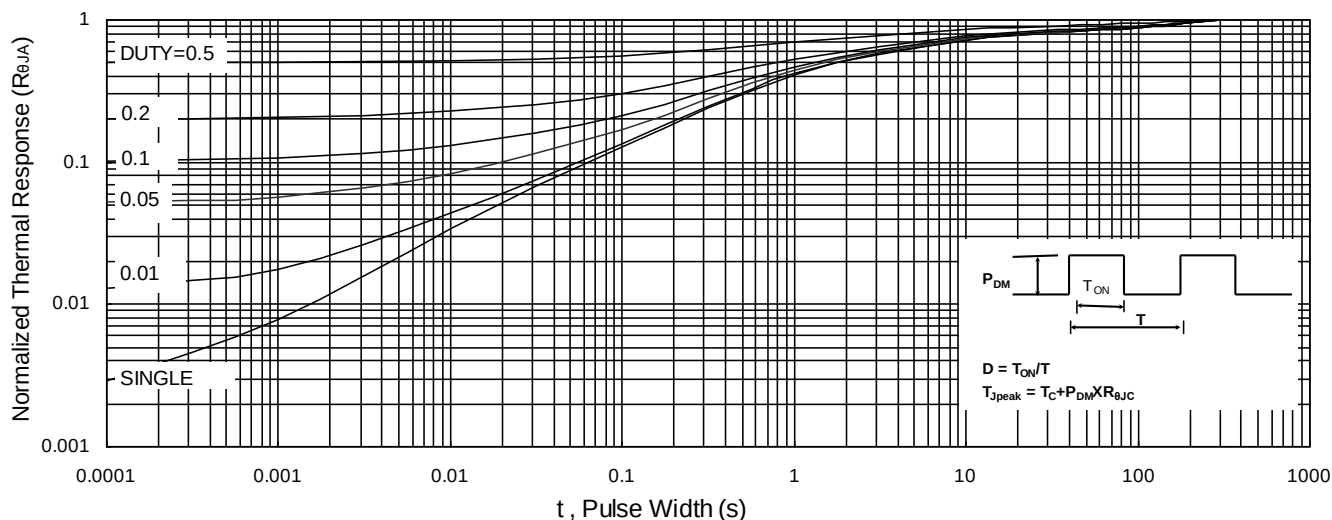
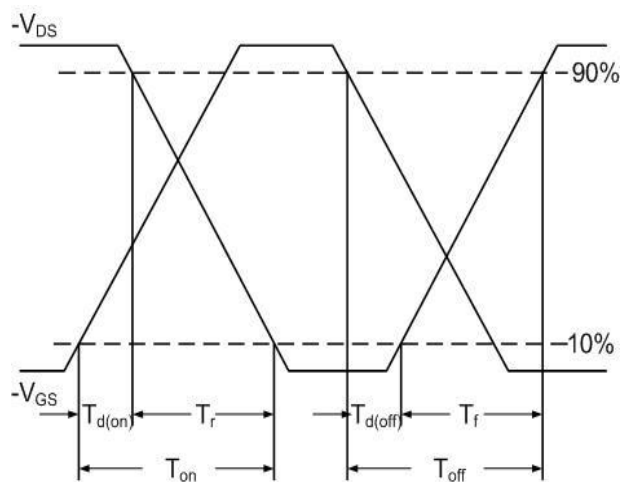
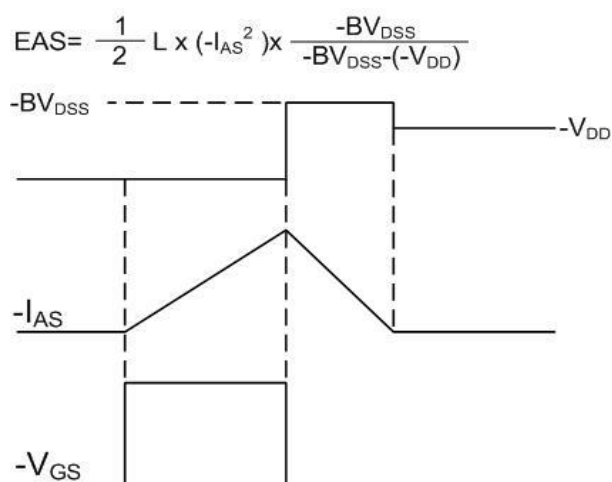
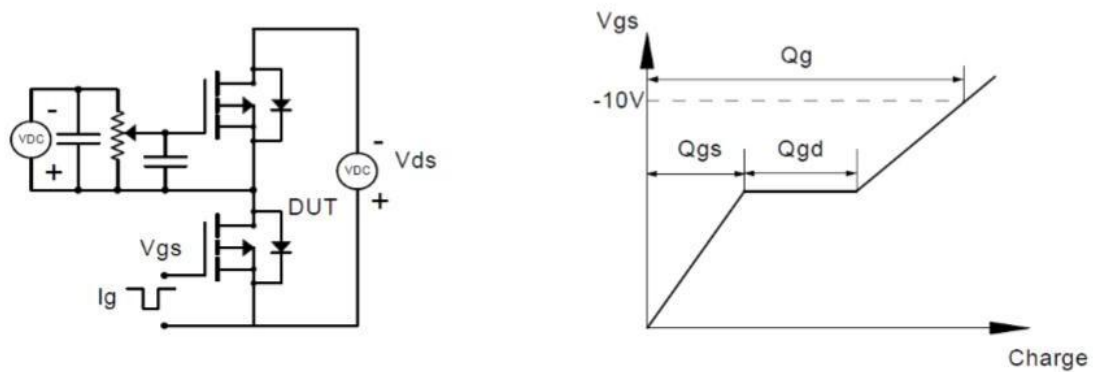


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

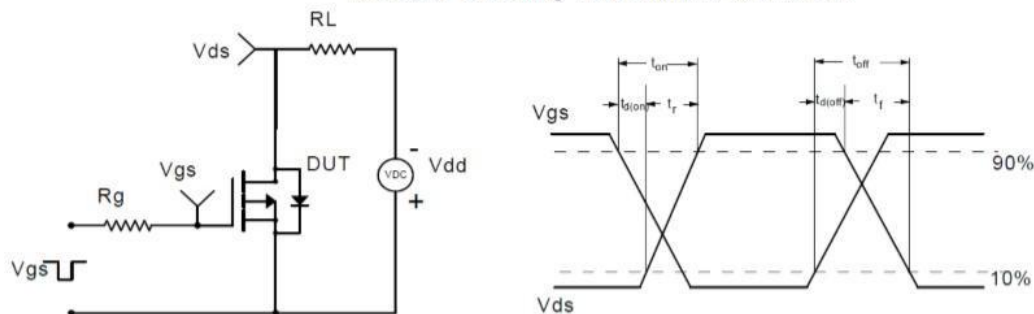

Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Fig.10 Switching Time Waveform

Fig.11 Unclamped Inductive Waveform

Test Circuit

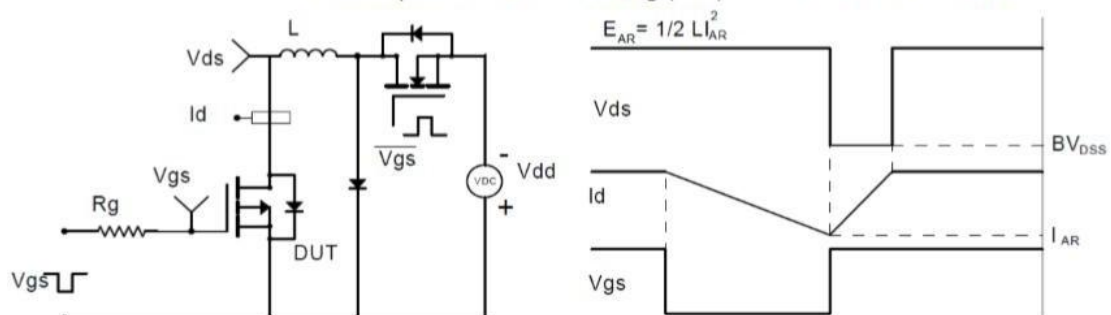
Gate Charge Test Circuit & Waveform



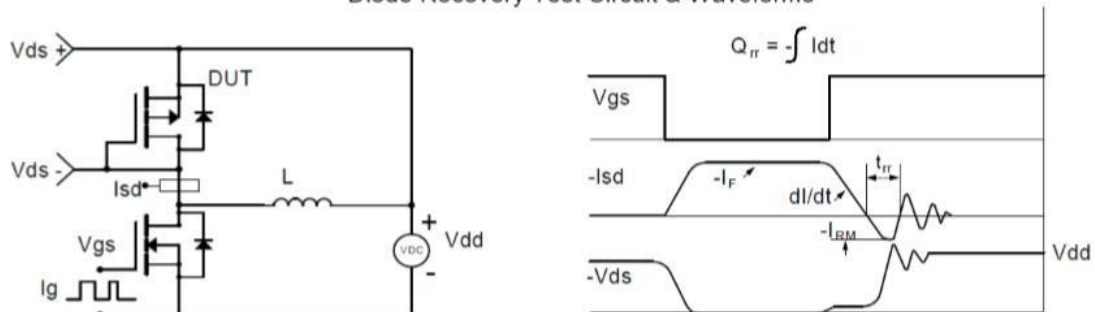
Resistive Switching Test Circuit & Waveforms



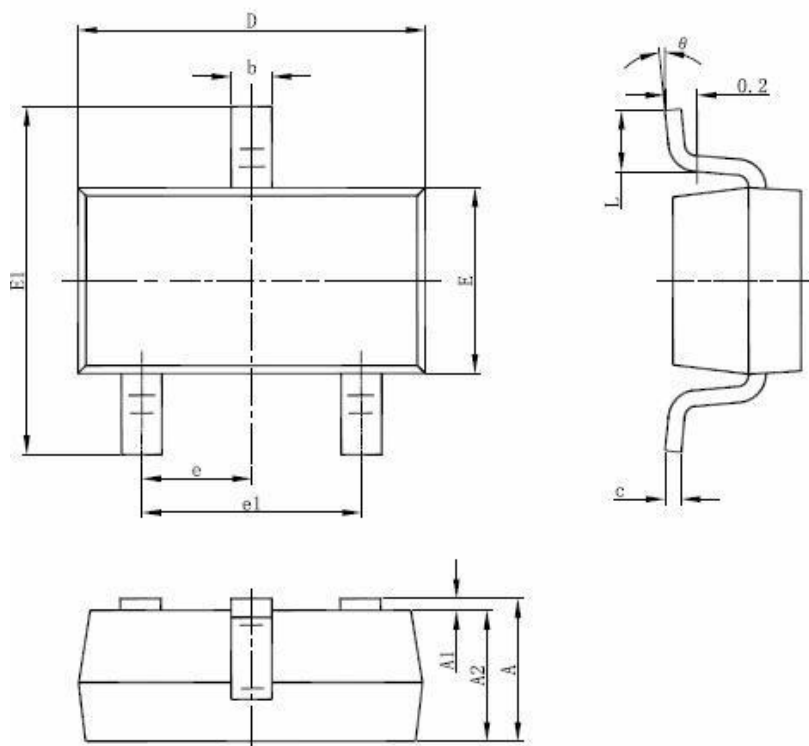
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



SOT-23-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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