



Data Sheet Addendum: LPDDR2 SDRAM

EDB8132B4PB-8D-F-R, EDB8132B4PB-8D-F-D

Features

This addendum documents features of the Micron® 4Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) device.

This addendum does not provide detailed device information. The standard density-specific device data sheet provides a complete description of device functionality, operating modes, and specifications unless specified herein.

Information provided here is in addition to or supersedes information in the device data sheet.

- Ultra-low-voltage core and I/O power supplies
- Frequency range
 - 400 MHz (data rate: 800 Mb/s/pin)
- 4n prefetch DDR architecture
- 8 internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on each CK/CK edge
- Bidirectional/differential data strobe per byte of data (DQS/DQS)
- Programmable READ and WRITE latencies (RL/WL)
- Burst length: 4, 8, and 16
- Per-bank refresh for concurrent operation
- Auto temperature-compensated self refresh (ATCSR) by built-in temperature sensor
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock-stop capability
- Lead-free (RoHS-compliant) and halogen-free packaging

Options

- $V_{DD1}/V_{DD2}/V_{DDCA}/V_{DDQ}$: 1.8V/1.2V/1.2V/1.2V
- Array configuration
 - 256 Meg x 32 (DDP)
 - 384 Meg x 32 (3DP)
 - 512 Meg x 32 (QDP)
- Packaging
 - 12mm x 12mm, 168-ball PoP FBGA package
- Operating temperature range
 - From -30°C to +85°C

Table 1: Configuration Addressing – Single-Channel Package

Architecture		256 Meg x 32
Density per package		8Gb
Die per package		2
Ranks (CS_n) per channel		1
Die per rank	CS0_n	2
	CS1_n	N/A
Configuration per rank (CS_n)	CS0_n	16 Meg x 32 x 8 banks
	CS1_n	N/A



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Table 1: Configuration Addressing – Single-Channel Package (Continued)

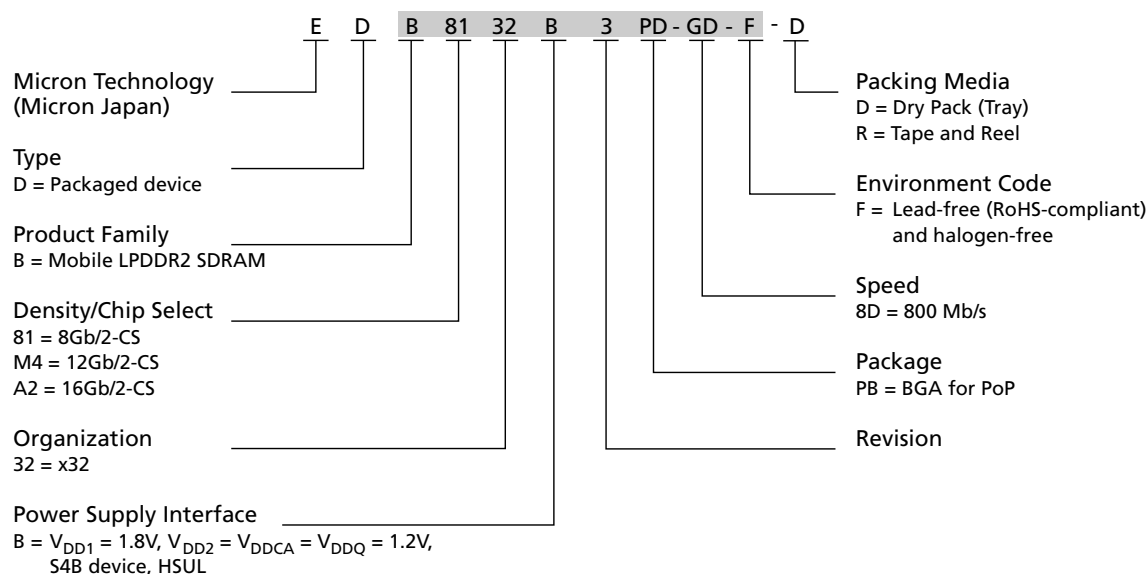
Architecture		256 Meg x 32
Row addressing		16K A[13:0]
Column addressing/CS_n	CS0_n	2K A[10:0]
	CS1_n	N/A

Table 2: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency (Set A/B)	READ Latency
8D	400	800	6/9	12

Table 3: Part Number Description

Part Number	Total Density	Configuration	Ranks	Channels	Package Size	Ball Pitch
EDB8132B4PB-8D-F-R, EDB8132B4PB-8D-F-D	8Gb	256 Meg x 32	1	1	12mm x 12mm (0.80mm MAX height)	0.50mm

Figure 1: Marketing Part Number Chart


Note: 1. The characters highlighted in gray indicate the physical part marking found on the device.



168-Ball LPDDR2 SDRAM Addendum General Description

General Description

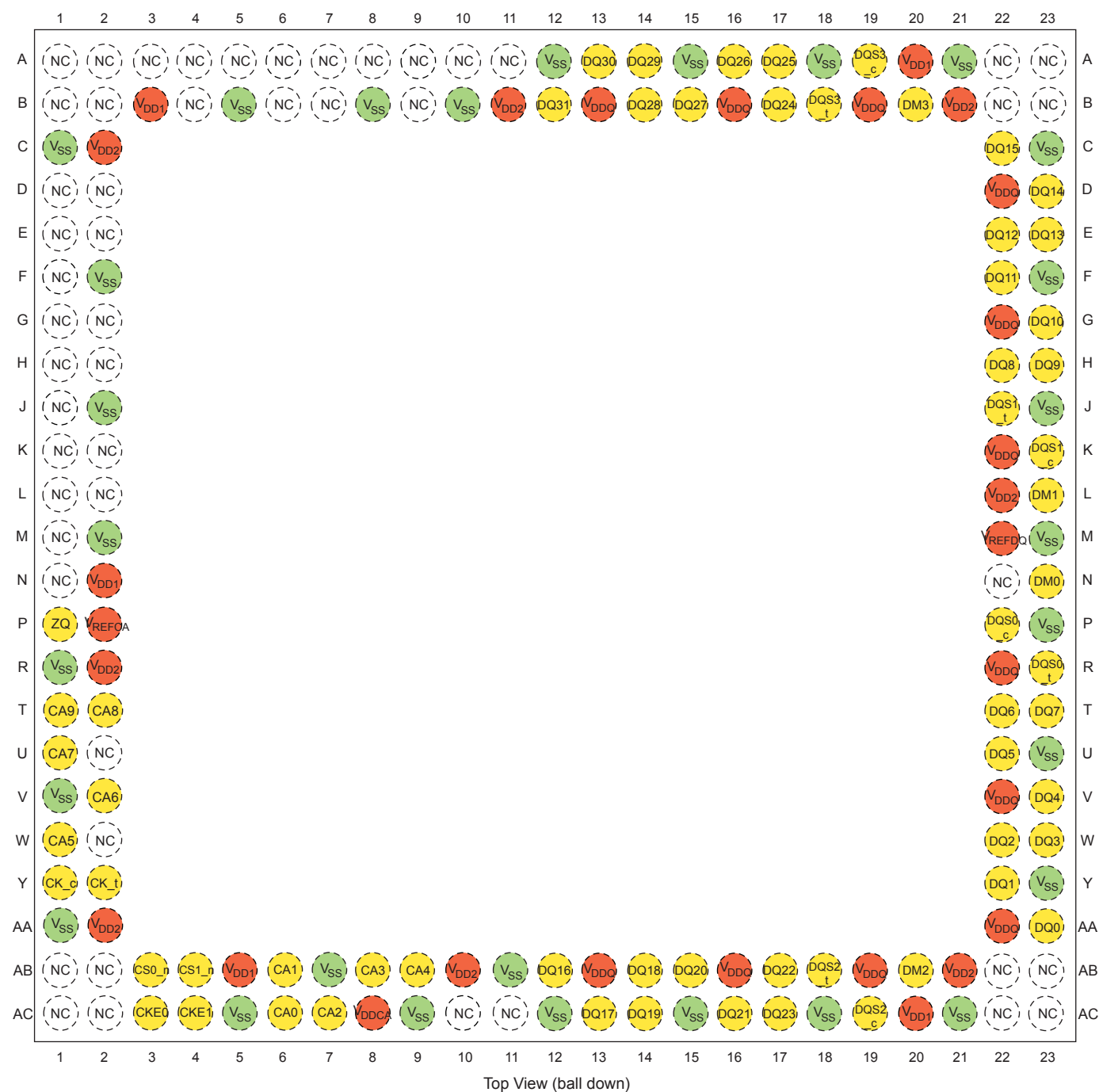
The 168-ball PoP FBGA package is available in a 2-die DDP configuration. This configuration is based on a Mobile Low-Power DDR2 SDRAM (LPDDR2) high-speed CMOS, dynamic random-access memory, containing 4,294,967,296-bits (4Gb). The device is internally configured as an eight-bank DRAM.



168-Ball LPDDR2 SDRAM Addendum Ball Assignments

Ball Assignments

Figure 2: 168-Ball PoP Single-Channel FBGA – 2 x 4Gb Die, 12mm x 12mm





168-Ball LPDDR2 SDRAM Addendum Ball Descriptions

Ball Descriptions

The ball/pad description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See Ball Assignments for information specific to this device.

Table 4: Ball/Pad Descriptions

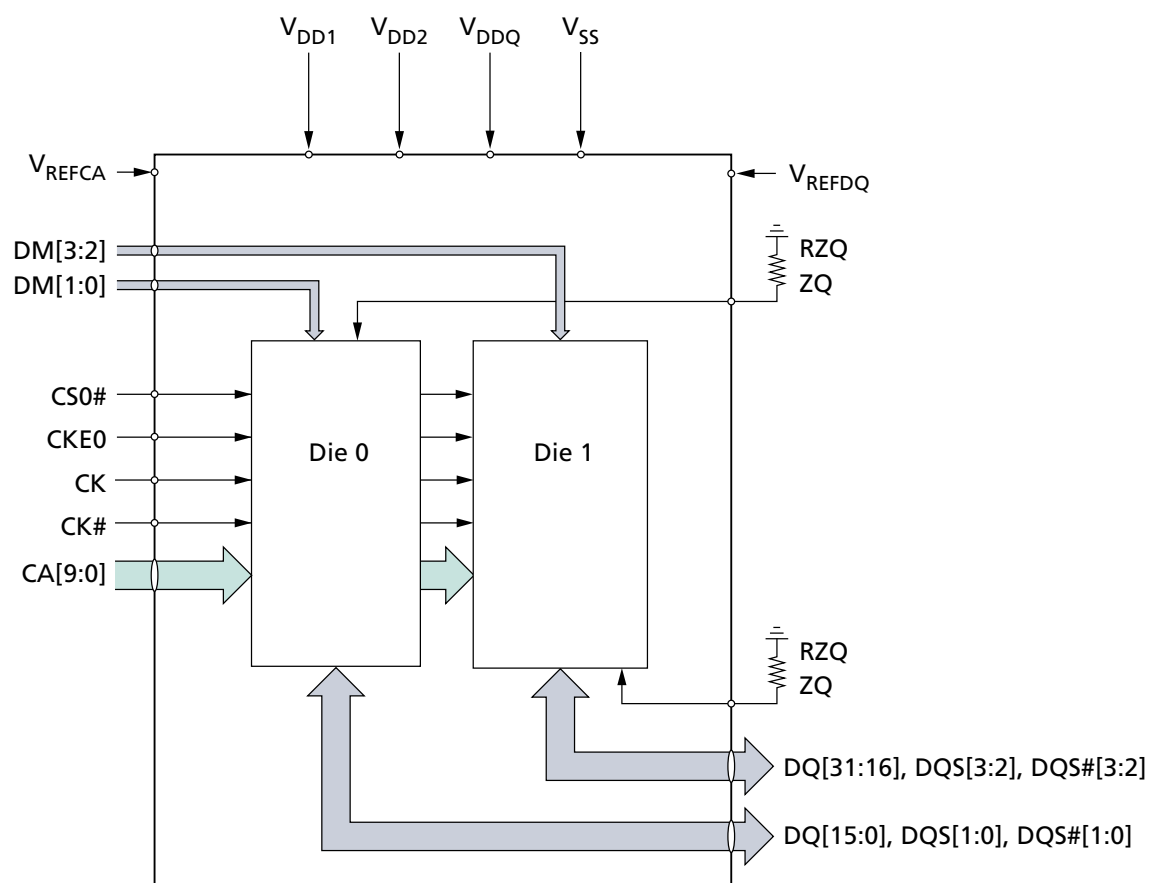
Symbol	Type	Description
CA[9:0]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
CK_t, CK_c	Input	Clock: Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE[1:0]	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled on the rising edge of CK.
CS[1:0]_n	Input	Chip select: Considered part of the command code and is sampled on the rising edge of CK.
DM[3:0]	Input	Input data mask: Input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ[31:0]	I/O	Data input/output: Bidirectional data bus.
DQS[3:0]_t, DQS[3:0]_c	I/O	Data strobe: Bidirectional (used for read and write data) and complementary (DQS_t and DQS_c). It is edge-aligned output with read data and centered input with write data. DQS[3:0]_t/DQS[3:0]_c is DQS for each of the four data bytes, respectively.
V _{DDQ}	Supply	DQ power supply: Isolated on the die for improved noise immunity.
V _{SSQ}	Supply	DQ ground: Isolated on the die for improved noise immunity.
V _{DD1}	Supply	Core power: Supply 1.
V _{DD2}	Supply	Core power: Supply 2.
V _{SS}	Supply	Common ground.
V _{REFCA} , V _{REFDQ}	Supply	Reference voltage: V _{REFCA} is reference for command/address input buffers, V _{REFDQ} is reference for DQ input buffers.
ZQ[1:0]	Reference	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (RZQ), which is tied to V _{SSQ} .
NU	–	Not usable: Do not connect.
NC	–	No connect: Not internally connected.
(NC)	–	No connect: Balls indicated as (NC) are no connects; however, they could be connected together internally.

Package Block Diagrams

Figure 3: Single-Rank, Dual-Die, Single-Channel Package Block Diagram



168-Ball LPDDR2 SDRAM Addendum Package Block Diagrams

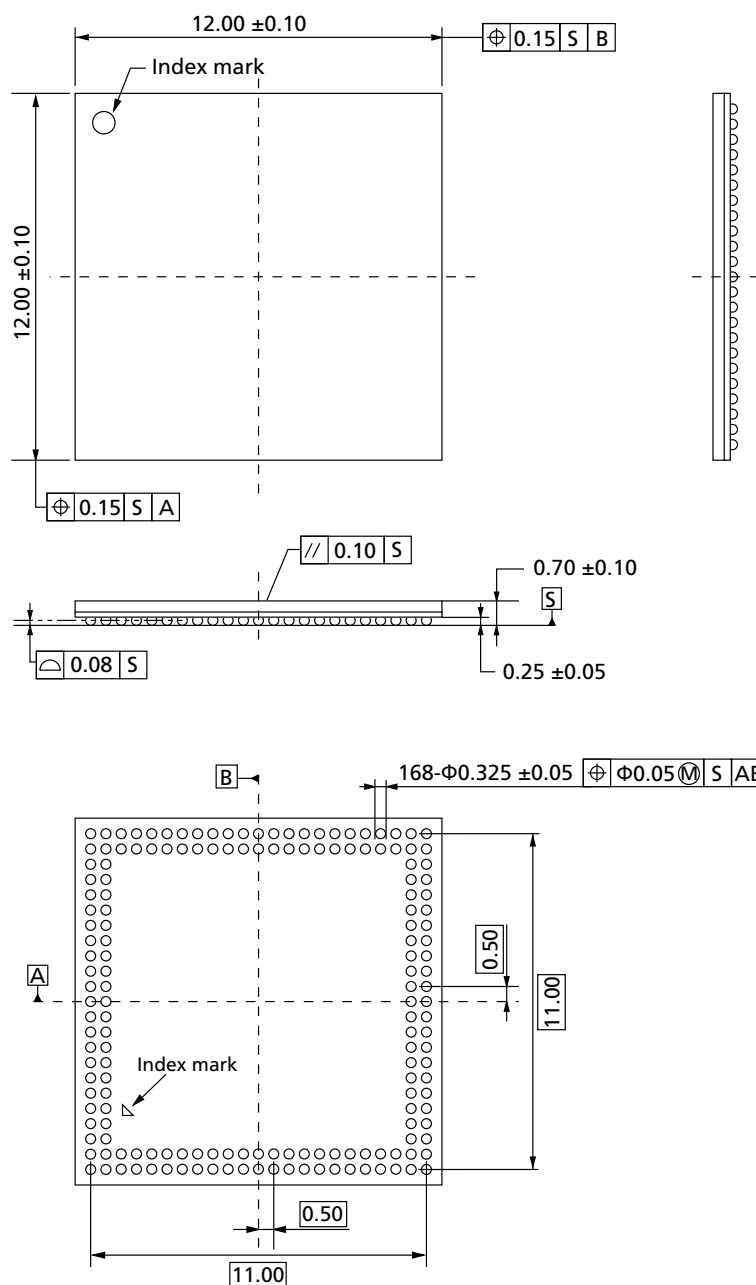




168-Ball LPDDR2 SDRAM Addendum Package Dimensions

Package Dimensions

Figure 4: 168-Ball PoP FBGA (12mm x 12mm) – EDB8132B4PB-8D-F-D/R



- Notes: 1. Package drawing: ECA-TS2-0515-02.
2. All dimensions are in millimeters.



168-Ball LPDDR2 SDRAM Addendum Revision History

Revision History

Rev. A – 04/14

- Initial release

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This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.